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A 21.2 μA $\Delta\Sigma$-Based Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer

Matti Paavola[1], *Mika Kämäräinen*[1], *Erkka Laulainen*[1], *Mikko Saukoski*[1,2], *Lauri Koskinen*[1], *Marko Kosunen*[1], *and Kari Halonen*[1]

[1]SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, Espoo, Finland
Email: mhpaavol@ecdl.tkk.fi

***Abstract*—In this paper, a micropower interface IC for a capacitive 3-axis micro-accelerometer implemented in a 0.25 -μm CMOS process is presented. The fully-integrated sensor interface consists of a $\Delta\Sigma$ sensor front-end that converts the acceleration signal into the digital domain, a decimator, a frequency reference, a clock generator for the front-end, a voltage and current reference, the required reference buffers, and low-dropout regulators (LDOs) needed for system-on-chip power management. The interface IC provides operating modes for 1 and 25 Hz signal bandwidths. The chip with a $1.72\,\mathrm{mm}^2$ active area draws $21.2\,\mu$A in 1 Hz mode, and $97.6\,\mu$A in 25 Hz mode, from a $1.2 - 2.75$ V supply. In 1 Hz mode with a ± 2 -g capacitive 3-axis accelerometer, the measured noise floors in the x-, y-, and z-directions are 1080, 1165 and $930\,\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$, respectively.**

I. Introduction

Micro-accelerometers have a wide range of different applications, such as automotive safety and stability control systems, navigation, and movement detection and user interfaces in hand-held mobile terminals and in game controllers. The use of microsensors in battery-powered equipment requires the sensor interface to exhibit low power dissipation and to be able to operate from supply voltages varying over a wide range. In order to realize a low-power, high-performance accelerometer with a small silicon area, the readout electronics has to be integrated together with the sensor element at chip or packaging level, forming a microelectromechanical system (MEMS).

The advantages of capacitive accelerometers [1], such as zero static bias current, the capability of achieving high sensitivity, and excellent thermal stability, are emphasized in ultra-low-power applications. In this paper, a fully-integrated low-voltage low-power sensor interface IC for a capacitive 3-axis micro-accelerometer will be presented. The system is based on the front-end circuit presented earlier by the authors in [2], and includes additionally a decimator, all the required reference circuits, and on-chip power management circuitry. The 2nd-order $\Delta\Sigma$ sensor front-end operates in open-loop configuration and performs inherent capacitance-to-digital conversion and charge balancing. The reasons for using an open-loop configuration are simple implementation that reduces both silicon area and power dissipation, and a limited voltage range available for electrostatic feedback.

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[2]Starting from the year 2008, M. Saukoski has been with ELMOS Semiconductor AG, Dortmund, Germany.

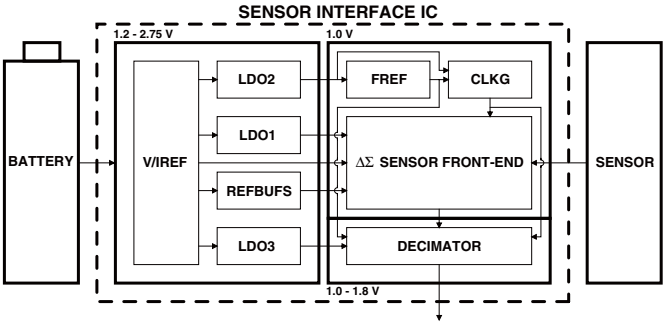

Fig. 1. Block diagram of the implemented interface IC for a capacitive 3-axis micro-accelerometer.

To make an operation over wide range of supply voltages $(1.2 - 2.75\,V)$ required by the battery-powered system possible, low-dropout regulators (LDOs) were implemented for system-on-chip power management. LDOs have significant advantages, such as fast transient response, low-noise characteristic, low complexity, and no need for inductors. The implemented sensor interface provides operating modes for 1 and 25 Hz signal bandwidths. The former makes it possible to detect accelerations while maintaining low power dissipation, and the latter can be used to measure accelerations over a wider bandwidth.

The paper is organized as follows. The system architecture of the implemented sensor interface is briefly described in Section II. Different circuit blocks are presented in Section III and the measurement results of the implemented prototype are presented in Section IV. Finally, conclusions are drawn in Section V.

II. System Description

A block diagram of the implemented sensor interface system is shown in Fig. 1. The $\Delta\Sigma$-type sensor front-end [2] converts the capacitive acceleration information from each of the three proof masses first to charge and then subsequently to a bit stream. The decimator, based on the implementation presented in [3], filters and decimates the single-bit outputs to the final desired bandwidth and accuracy. The frequency reference circuit (FREF) [4] provides the master clock signal for both the clock generator of the front-end (CLKG) and for the decimator. The CLKG then generates all the clock signals required by the front-end.

The voltage and current reference circuit (V/IREF) provides the main reference voltage and current, together with the bias voltages and currents required by the other circuit blocks. The

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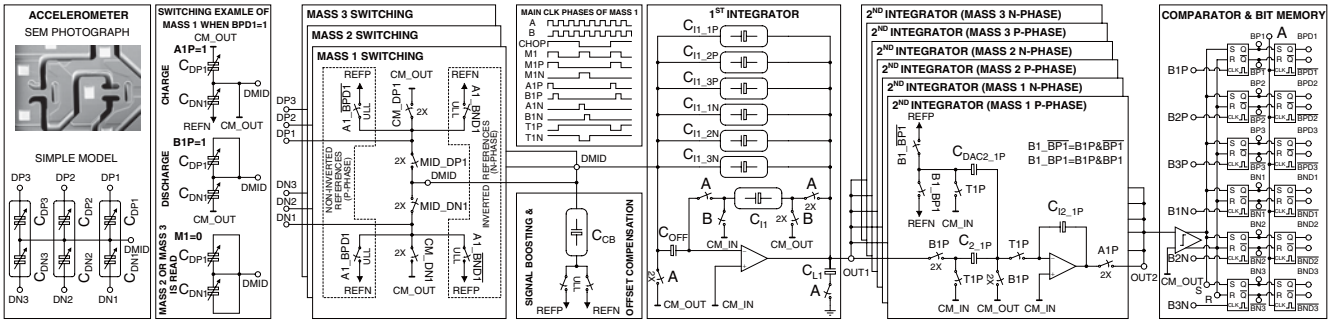

Fig. 2. Schematic of the $\Delta\Sigma$ sensor front-end with an SEM photograph of a capacitive 3-axis micro-accelerometer. (SEM image courtesy of VTI Technologies, Vantaa, Finland).

reference voltage buffers (REFBUFs) are used to scale and buffer the reference voltage, and they provide the positive reference (REFP) and the common-mode output (CM_OUT) and input (CM_IN) voltages required by the front-end circuit. Two separate buffers were designed to optimize power dissipation in both 1 and $25\,Hz$ operating modes.

Two LDOs were implemented to provide separate $1.0\,V$ regulated supply voltages for the $\Delta\Sigma$ sensor front-end and for the FREF and the CLKG. Additionally, the decimator had to be provided with an LDO of its own with programmable output voltage from 1.0 to $1.8\,V$, as the standard cell library used in the design was specified only for supply voltages down to $1.8\,V$. To avoid the use of impractical off-chip load capacitors and to guarantee the maximum tolerable output voltage drop of $0.1\,V$, the LDOs were equipped with programmable on-chip load capacitors up to $1\,nF$. Because of the low-power characteristic of the sensor interface, the LDOs must remain stable with zero load currents.

In order to reach a sufficient ($> 20\,dB$) mechanical attenuation of folding out-of-band interferers and low enough noise level for 12-bit resolution for a ± 2-g dc acceleration signal in $1\,Hz$ mode, a sampling frequency of $4.096\,kHz$ per mass was chosen. With a full-scale input signal, the maximum signal-to-noise ratio of the sensor front-end would then be limited by thermal noise to 16 bits. However, the limited signal available from the ± 2-g accelerometer limits the achievable dynamic range to 12 bits. In the $25\,Hz$ mode, a sampling frequency of $51.2\,kHz$ is required for the same resolution. The 16-bit accuracy is demanded also from the reference buffers. This has an adverse effect on the current consumption of the REFBUFs.

The attenuation of the used sinc^3 decimation filters is not allowed to be greater than $3\,dB$ at the edge of the passband. Thus, the output data rate of the decimator was chosen to be 4 and $100\,Hz$ in the 1 and $25\,Hz$ modes, respectively. Because of the absence of analog gain control before the A/D conversion, the decimator is equipped with shifters for gain control and 16-bit wide serial outputs to maintain the resolution even at the presence of uncompensated offsets.

III. Circuit Description

A. $\Delta\Sigma$ Sensor Front-End

The schematic of the $\Delta\Sigma$ sensor front-end with the sensor element is shown in Fig. 2. The front-end balances charge,

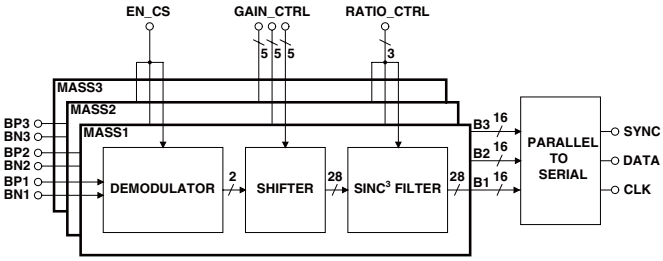

Fig. 3. Simplified block diagram of the decimator.

in other words it ensures an equal average charge in both positive and negative detection capacitances, and thus reduces the distorting effects of the nonlinear electrostatic forces. The resulting transfer function from acceleration to bit stream is of the form $(C_{DP} - C_{DN})/(C_{DP} + C_{DN})$, which cancels the nonlinearity of the displacement-to-capacitance transducer to the first order. Chopper stabilization (CS) and correlated double sampling (CDS) are implemented in order to reduce the offset voltage and noise of the front-end.

The operation principle of the front-end is described in detail in [2]. The positive and negative reference voltages are equal to the supply and ground. Because of the low supply voltage of $1.0\,V$, the input and output common-mode levels of the operational amplifiers are separated to 0.1 and $0.5\,V$, respectively. To minimize power dissipation, a tail-current-boosted Class-AB operational amplifier [5] with enhanced dc gain [2] is used in the 1st integrator. The operational amplifier used in the 2nd integrators is a basic current mirror OTA, whose dc gain is enhanced with the same technique. The simulated dc gains of the two amplifiers are approximately 50 and $45\,dB$, respectively. A dynamic latch with zero static power dissipation is used as a comparator.

The programmable capacitor matrix C_{CB} can be used to sink charge from the sensor middle electrode DMID. It makes possible both boosting the available signal and compensating the offsets of the sensor capacitors [2]. Because of the low supply voltage, the gate voltage of an NMOS device in a floating transmission gate is increased to $2 \cdot V_{DD}$ using charge pumps [2]. The symbol 2x is used to indicate the gate-voltage-boosted switches in Fig. 2. As the node DMID is especially sensitive to leakage currents, a special ultra-low-leakage switch [2] denoted by ULL in Fig. 2 was developed.

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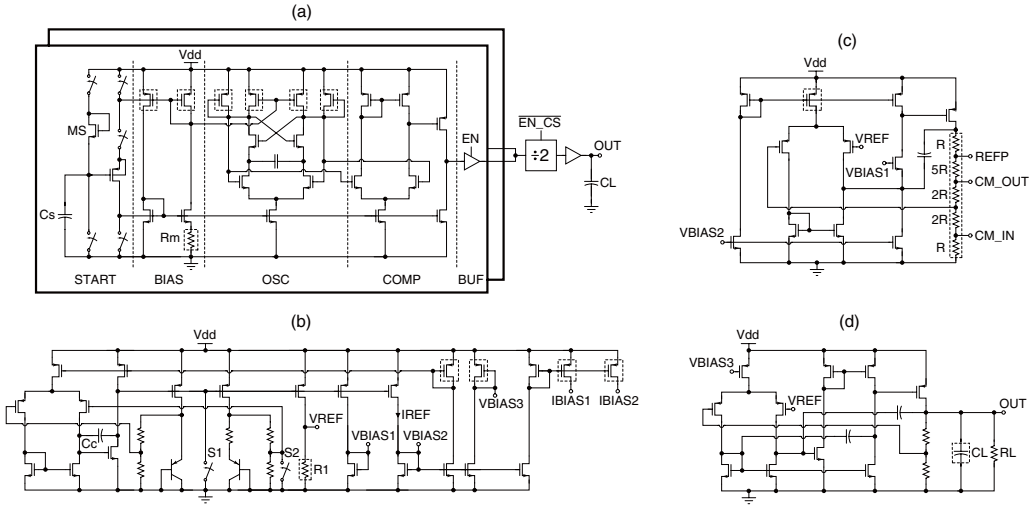

Fig. 4. Schematics of: (a) a frequency reference; (b) a voltage and current reference; (c) a reference voltage buffer, and (d) an LDO.

B. Decimator

The simplified block diagram of the designed decimator based on three parallel sinc^3 filters [3], one for each proof mass, is shown in Fig. 3. Three-stage cascaded integrator-comb (CIC) filters with one sample delays and selectable rate change factor are used. Each of the filters has two 1-bit inputs and a 16-bit wide output. When CS is not used, the filters use only one input. In the case of CS enabled, the demodulation is performed by subtracting the two input bits. After possible demodulations the signals can be scaled with shifters. The decimation ratio can be selected between 16 and 512, with each control step doubling the ratio. The outputs from the three filters are fed to a parallel-to-serial converter that outputs the 48 (3×16) bits. Based on the measurement results [3], the decimator operates nominally from a $1.0\,V$ supply in $1\,Hz$ mode, and from a $1.8\,V$ supply in $25\,Hz$ mode. The decimation ratios used are 512 and 256, respectively.

C. Reference Circuits and LDOs

The master clock frequency is $24.576\,kHz$ in $1\,Hz$ mode and $307.2\,kHz$ in $25\,Hz$ mode. The frequency reference that provides the master clock signal and which consists of two parallel source-coupled CMOS multivibrator-based structures is shown in Fig. 4 (a) [4]. Both modes require an independent frequency reference circuit because, due to the low supply voltage of $1.0\,V$, floating switches cannot be used, and therefore a sufficient frequency tuning range cannot be achieved by using capacitor matrices. Coarse tuning is implemented by using PMOS transistor matrices in the biasing circuits and in the multivibrators, while fine tuning is implemented with resistor matrix Rm (matrices marked with dashed boxes in Fig. 4). The devices Rm, MS, and Cs are common for the two frequency references. The used biasing circuits are proportional-to-absolute-temperature (PTAT) current generators. Two-stage differential comparators are used to magnify the oscillation amplitudes rail-to-rail, and tri-state buffers are used to interface the parallel frequency references to the divider consisting of two cascaded gated SR latches. The divide-by-two operation is enabled when CS is disabled.

The designed V/IREF shown in Fig. 4 (b) is based on the bandgap reference topology presented in [6], and it is suitable to be implemented with a standard CMOS process. A Miller-compensated operational amplifier with a PMOS input pair is used as the feedback amplifier. To allow the use of supply voltages down to $1.2\,V$, the input voltage levels of the operational amplifier are lowered with resistive voltage dividers. The effects of process variations on the output voltage level (VREF nominally $0.3\,V$) can be eliminated by trimming R1. To achieve a sufficient noise performance, the bandwidth of the bandgap reference is limited aggressively by using the compensation capacitor Cc of $50\,pF$. As a result, the bandwidths of the negative feedback loop and the closed loop are nominally 1.6 and $11.0\,kHz$, respectively. The NMOS switches S1 and S2 were included to provide a power-on-reset that can be used to force the bandgap reference to the right operating point, if needed. Programmable biasing currents IBIAS1 and IBIAS2 are used to bias the amplifiers of the $\Delta\Sigma$ sensor front-end.

The two REFBUFs have identical schematics shown in Fig. 4 (c), but different device parameters. Time constants formed by the resistances of the resistive networks and the load capacitances from the front-end and the sensor element determine the settling accuracies.

The LDO shown in Fig. 4 (d) is based on the structure presented in [7]. It uses a Q-reduction technique to minimize both the required on-chip capacitance and the minimum output current. Nominally, the current of $2.0\,\mu A$ flows through the feedback resistive network. The requirement for stability at zero load current ($RL \rightarrow \infty$) results in a small bandwidth of $18.5\,kHz$ for the loop response. To minimize the silicon area required by the programmable $1\,nF$ load capacitors metal-insulator-metal (MIM) capacitors were stacked above standard MOS capacitors.

IV. Measurement Results

The prototype chip with a $1.72\,mm^2$ active core area shown in Fig. 5 was fabricated in a 0.25-μm CMOS technology.

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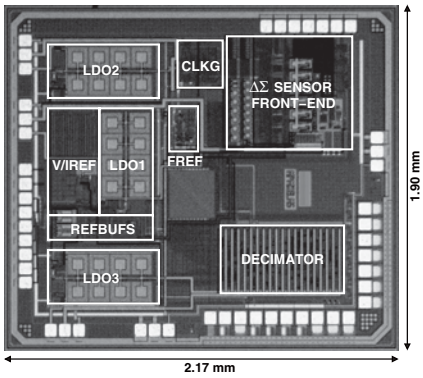

Fig. 5. Microphotograph of the implemented chip.

TABLE I
SUMMARY OF MEASURED PERFORMANCE.

Process	0.25-μm CMOS with MIM capacitors and high-resistivity polysilicon resistors		
Supply	$1.2 - 2.75\,V$ Two $1.0\,V$ and one $1.0 - 1.8\,V$ regulated on chip		
Configuration	With CS and CDS Without signal boosting and offset compensation		
Active area	$1.72\,mm^2$		
Mode	**1 Hz**	**25 Hz**	
f_s per mass	4.096	51.2	kHz
Current consumption			
I_{LDO1}[a]	14.5	84.3	μA
I_{LDO2}[b]	3.5	5.2	μA
I_{LDO3}[c]	3.2	8.1	μA
Total	21.2	97.6	μA
Noise floor			
x-axis	1080	340	$\mu g/\sqrt{Hz}$
y-axis	1165	325	$\mu g/\sqrt{Hz}$
z-axis	930	275	$\mu g/\sqrt{Hz}$

[a] LDO1, V/IREF, REFBUFs, and $\Delta\Sigma$ sensor front-end
[b] LDO2, FREF, and CLKG
[c] LDO3 and decimator

For the measurements, the chip was encapsulated into a plastic quad flat package (QFP) with 64 pins and soldered onto a printed circuit board (PCB). The chip was combined with an external ± 2-g capacitive 3-axis accelerometer on the PCB. The results presented below were measured for the complete system shown in Fig. 1, while the prior results of the $\Delta\Sigma$ sensor front-end published in [2] were obtained using both off-chip decimator, and off-chip references and power management.

The performance measured for both modes using a $2.5\,V$ supply voltage and $0.5\,nF$ load capacitors at the outputs of the LDOs is summarized in Table I. All the results were measured by using both CS and CDS, but without using signal boosting or offset compensation. The core circuit consumes $21.2\,\mu A$ in $1\,Hz$ mode and $97.6\,\mu A$ in $25\,Hz$ mode. The noise results yield dynamic ranges of 70 and $67\,dB$ for dc input signals in 1 and $25\,Hz$ modes, respectively. FFTs measured from the output of the sensor front-end, for the x-directional data in $1\,Hz$ mode and the z-directional data in $25\,Hz$ mode, are shown in Figs. 6 (a)-(b). The root Allan variance for the y-directional data and the ± 2-g acceleration ramps, both measured from the decimator output in $1\,Hz$ mode, are shown in Figs. 6 (c)-(d). The ramps were measured using a rotating rate table. The results are expected to improve when the interface IC is bonded directly to the sensor.

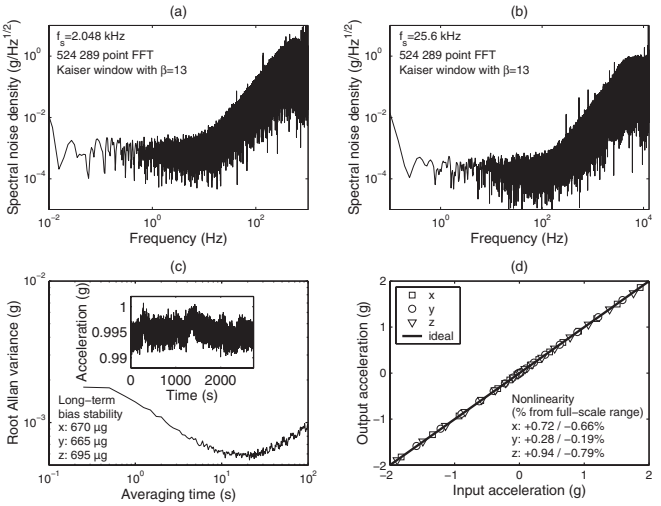

Fig. 6. FFTs of measured (a) x-directional data in $1\,Hz$ mode and (b) z-directional data in $25\,Hz$ mode, and measured (c) root Allan variance for y-directional data and (d) ± 2-g acceleration ramps in $1\,Hz$ mode.

V. CONCLUSION

In this paper, a micropower $\Delta\Sigma$-based interface IC for a capacitive 3-axis micro-accelerometer implemented in a 0.25-μm CMOS process was presented. In $1\,Hz$ mode, the chip with a $1.72\,mm^2$ active area draws $21.2\,\mu A$ from a $1.2 - 2.75\,V$ supply while sampling three proof masses, each at $4.096\,kHz$. With a ± 2-g capacitive 3-axis accelerometer, the measured noise floors in the x-, y-, and z-directions are 1080, 1165 and $930\,\mu g/\sqrt{Hz}$, respectively. Compared to the open-loop sensor interface of [1] which includes separate capacitance-to-voltage and voltage-to-digital conversions, the presented measurement results prove that by using both open-loop configuration and inherent capacitance-to-digital conversion, an alternative low-voltage low-power sensor interface can be implemented.

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