Publication P6

Matti Paavola, Mika Kämäräinen, Erkka Laulainen, Mikko Saukoski, Lauri Koskinen, Marko Kosunen, and Kari A. I. Halonen. 2009. A micropower ΔΣ-based interface ASIC for a capacitive 3-axis micro-accelerometer. IEEE Journal of Solid-State Circuits, volume 44, number 11, pages 3193-3210.

A Micropower $\Delta\Sigma$-Based Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer

Matti Paavola, *Student Member, IEEE*, Mika Kämäräinen, *Student Member, IEEE*, Erkka Laulainen, *Student Member, IEEE*, Mikko Saukoski, *Member, IEEE*, Lauri Koskinen, *Member, IEEE*, Marko Kosunen, *Member, IEEE*, and Kari A. I. Halonen, *Member, IEEE*

***Abstract*—In this paper, a micropower interface IC for a capacitive 3-axis micro-accelerometer is presented. The IC is implemented in a 0.25-μm CMOS process. The fully-integrated sensor interface is based on a $\Delta\Sigma$ sensor front-end that operates mechanically in an open-loop configuration and converts the acceleration signals directly into the digital domain, thus avoiding the use of separate analog-to-digital converters. A detailed analysis with transfer functions is presented for the front-end circuit. Furthermore, the interface IC includes a decimator, a frequency reference, a clock generator for the front-end, a voltage and current reference, the required reference buffers, and low-dropout regulators (LDOs) needed for system-on-chip power management. The interface IC provides operating modes with 12-bit resolution for 1 and 25 Hz signal bandwidths. The former is optimized for very low power dissipation at the cost of reduced bandwidth, and is intended for example for activity monitoring in otherwise powered-off devices. The chip, with a 1.73 mm^2 active area, draws typically 21.2 μA in the 1 Hz mode, and 97.6 μA in the 25 Hz mode, from a 1.2–2.75 V supply. In the 1 and 25 Hz modes with a $\pm$4-g capacitive 3-axis accelerometer, the measured noise floors in the x-, y-, and z-directions are 1080, 1100 and 930 $\mu g/\sqrt{Hz}$, and 360, 320 and 275 $\mu g/\sqrt{Hz}$, respectively. The implemented prototype achieves competitive Figures of Merit (FOMs) compared to the other published or commercially available, low-g, low-power accelerometers.**

***Index Terms*—Low-power circuit, low-voltage circuit, microelectromechanical system (MEMS), sensor interface, switched-capacitor circuit, three-axis accelerometer, $\Delta\Sigma$ front-end.**

I. Introduction

MICRO-SENSORS have three main application fields: information technology (IT) peripherals, automotive, and consumer electronics. According to the market analysis presented in [1], IT peripherals will remain as the leading application field of the microelectromechanical systems/microsystems technology (MEMS/MST) products in 2009, mainly thanks to the hard drive read/write heads and inkjet printing heads. Automotive applications, such as safety and stability control and various comfort systems, will also remain an important application field. Nevertheless, the widespread use of micro-sensors, mainly accelerometers and pressure sensors, in the automotive industry has pushed their unit prices down dramatically. Micro-sensor applications in consumer electronics are experiencing the strongest market growth. Consumer electronics is expected to increase its share in the MEMS/MST market to 22% in 2009, and it is already overtaking the automotive [1].

Accelerometers are widely used in inertial and tilting sensing. Typically, the design focus is then set to dc accuracy, null drift with time and temperature, and resolution. When considering consumer electronics, like portable terminals and game controllers, additional design criteria, such as micropower dissipation, a wide supply voltage range, and a small silicon area must be taken into account. A single 3-axis accelerometer makes the sensing of all three linear acceleration vector components in a three-dimensional space possible. The fully-integrated sensor interface with a digital output, proposed in this paper, is capable of reading a capacitive 3-axis accelerometer and it is suitable for the aforementioned low-power, low-cost consumer electronics applications [2].

Many high-performance micro-accelerometers based on the electromechanical force-balancing $\Delta\Sigma$ loop, an idea that was first reported in 1990 [3], have been published during the last ten years [4]–[6]. However, due to the additional complexity and power dissipation resulting from the mechanical force balancing, i.e. the mechanical closed-loop operation, low-power and low-cost accelerometers typically operate mechanically in open-loop configuration [7]–[9]. Only a few complete, low-g, low-power, 3-axis accelerometers have been published [9], while there are numerous commercial products of that kind available with both analog [10]–[13] and digital outputs [14]–[20].

The application area of accelerometers is often expanded by providing several active operating modes with various functionalities. The interface IC presented in this paper provides two operating modes with relatively low signal bandwidths of 1 and 25 Hz. The modes have an equal resolution of 12 bits, but the 1 Hz mode is optimized for very low power dissipation at the cost of reduced signal bandwidth. The 25 Hz mode can be used in applications such as motion and tilting sensing in handheld devices, digital cameras, and antitheft systems. The 1 Hz mode, on the other hand, is applicable for example for activity monitoring in otherwise powered-off devices. The implemented interface IC stands out from the available products by enabling the use of lower supply voltages. The on-chip power management, realized using low-dropout regulators (LDOs), provides supply voltages down to 1.0 V from a 1.2–2.75 V battery. In

Manuscript received December 01, 2008; revised July 06, 2009. Current version published October 23, 2009. This paper was approved by Associate Editor Michael P. Flynn. This work was supported by VTI Technologies and the Finnish Funding Agency for Technology and Innovation (TEKES).

M. Paavola, M. Kämäräinen, E. Laulainen, L. Koskinen, M. Kosunen, and K. A. I. Halonen are with the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, 02150 Espoo, Finland (e-mail: mhpaavol@ecdl.tkk.fi; mpkamara@ecdl.tkk.fi; elaulain@ecdl.tkk.fi; lauri.koskinen@ecdl.tkk.fi; mak@ecdl.tkk.fi; karih@ecdl.tkk.fi).

M. Saukoski was with the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology. He is now with ELMOS Semiconductor AG, 44227 Dortmund, Germany (e-mail: mikko.saukoski@elmos.eu).

Digital Object Identifier 10.1109/JSSC.2009.2031059

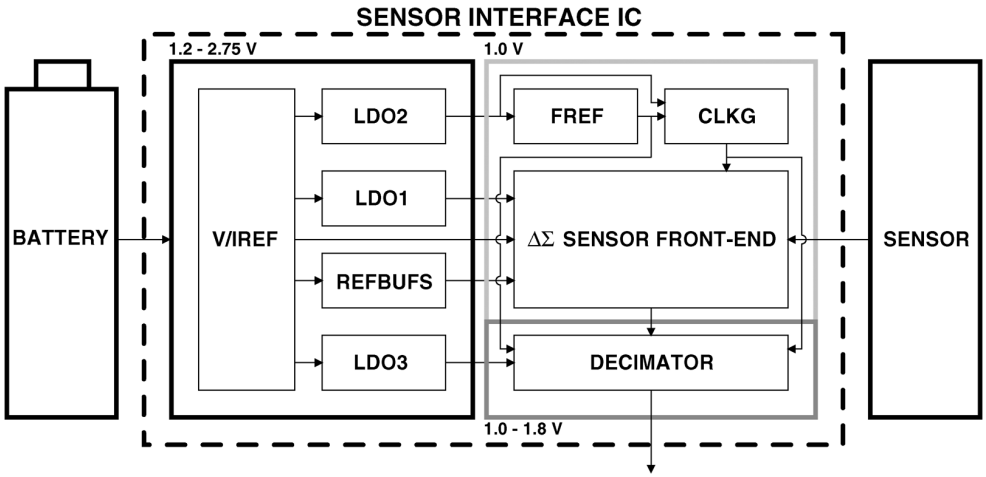

Fig. 1. Block diagram of the implemented interface IC for a capacitive 3-axis micro-accelerometer.

order to reduce both power dissipation and the silicon area, the accelerometer is read by an innovative $\Delta\Sigma$ sensor front-end [21] that provides a direct capacitance-to-digital conversion and operates mechanically in open-loop configuration. The charge balancing behavior of the implemented front-end reduces the distorting effects of the nonlinear electrostatic forces. In addition to the front-end and the LDOs, the proposed sensor interface consists of a decimator and reference circuits required for the generation of clock signals and reference voltages and currents.

Parts of this system have already been published in [2] and [21]. This paper extends and deepens the presentation in comparison to those publications by providing a more detailed analysis of the $\Delta\Sigma$ sensor front-end, extensive measurement results of both the individual building blocks and the system, and a performance comparison with other recently published or commercially available, low-g, low-power accelerometers. The system measurements presented in this paper prove good noise performance, and excellent current consumption and linearity.

The rest of the paper is organized as follows. The system architecture and the specifications are presented in Section II. Designed circuit blocks are described in detail in Section III and the measurement results of the implemented prototype together with the performance comparison are presented in Section IV. Conclusions are drawn in Section V.

II. System Description

A block diagram of the implemented sensor interface system is shown in Fig. 1. The interface IC addressed in this paper is outlined with the dashed line. The sensor interface is used to read a capacitive 3-axis accelerometer that consists of three proof masses. The masses form differential capacitor pairs, which have a common middle electrode, but separate top and bottom electrodes. These capacitances change as a result of the movements of the masses induced by the accelerations. The IC is powered using a single 1.2–2.75 V battery. This varying supply voltage must be taken into account in the power management design. Another limiting factor to the power management design is the fact that the available standard digital cell library has been characterized only for supply voltages down to 1.8 V. In addition to the normal operating mode with 25 Hz signal bandwidth and 12-bit resolution, the implemented sensor interface is provided with another mode, which has the same resolution but is optimized for very low power dissipation at the cost of the reduced signal bandwidth of 1 Hz. This mode is intended mainly for activity monitoring purposes. The doubling of the active operating modes enables power saving at the cost of larger silicon area.

Next, each building block of the sensor interface IC is briefly introduced. The $\Delta\Sigma$-type sensor front-end [21] converts the capacitive acceleration information from each of the three proof masses first to charge and then subsequently to a bit stream. The decimator, based on the implementation presented in [22], filters and decimates the single-bit outputs to the final desired bandwidth and accuracy. The frequency reference circuit (FREF) [23] provides the master clock signal for both the clock generator of the front-end (CLKG) and for the decimator. The CLKG generates all the clock signals required in the front-end. The reference voltage buffers (REFBUFs) are used to scale and buffer the reference voltage provided by the voltage and current reference (V/IREF). Two separate buffers were designed to optimize power dissipation in both the 1 and 25 Hz operating modes.

To make the battery-powered operation possible, the system-on-chip power management is provided by using LDOs that have significant advantages, such as fast transient response, low-noise characteristic, low complexity, and no need for inductors. Two LDOs (LDO1 and LDO2), that are based on the prototype LDO presented in [24], provide separate analog and digital regulated supply voltages of 1.0 V, for the $\Delta\Sigma$ sensor front-end and for the FREF and the CLKG, respectively. Additionally, the decimator requires an LDO of its own (LDO3) with a programmable output voltage level ranging from 1.0 to 1.8 V, as the standard digital cell library used in the design has been characterized by the vendor only for supply voltages down to 1.8 V. By tailoring the digital library cells for low-voltage operation, the need for the third LDO could be avoided. This is possible, as the speed requirements of this application are very moderate. Then, the LDO2 would also drive the decimator, and the quiescent current consumption of the LDO3 could be eliminated.

In this design, the V/IREF, the REFBUFs, and the LDOs operate directly from the battery voltage. This is evident for the

TABLE I
SENSOR ELEMENT PARAMETERS

Parameter	Symbol	Min	Typ	Max
Full-scale range		$-4\,g$		$+4\,g$
Static capacitance	C_0	$1.5\,pF$		$2.5\,pF$
Capacitance sensitivity	$\Delta C/\Delta a$	$50\,fF/g$		$150\,fF/g$
Bandwidth	BW		$100\,Hz$	
Die size			$2\,mm \times 2\,mm$	

LDOs, and is also necessary for the V/IREF, because the reference voltage created by the V/IREF is required for the proper operation of the LDOs. Furthermore, the REFBUFs are forced to use a supply voltage above 1 V, since they must be able to buffer a reference voltage of 1.0 V for the front-end. In order to guarantee the proper operation of the aforementioned circuit blocks over the process, supply voltage, and temperature variations, the lower end of the battery voltage range is limited to 1.2 V.

The sensor parameters used in the front-end design are given in Table I. The static capacitance C_0 and the single-ended capacitance sensitivity $\Delta C/\Delta a$ (i.e. per one half of the differential detection capacitance pair) of the detection capacitances in each direction vary between 1.5–2.5 pF and 50–150 fF/g, respectively. The -3 dB bandwidth of the sensor element is typically 100 Hz in each direction. Because of the high mass of the bulk-micromachined sensor element (of the order of micrograms), it can be safely assumed that the Brownian noise does not limit the noise performance of the system.

According to the worst case sensor parameters, $C_0 = 2.5$ pF and $\Delta C/\Delta a = 50$ fF/g, the maximum capacitive signal available from this $\pm$4-g accelerometer does not cover the whole input range of the $\Delta\Sigma$ sensor front-end, but is limited roughly to the level of the 12th part of the full-scale range. Therefore, the front-end has to be designed so that the available capacitive signal is sufficient for 12-bit resolution. If it would be possible to utilize the whole input range of the front-end, the signal-to-noise ratio of the front-end would then be limited to almost 16 bits. In order to reach a sufficient, >20 dB, mechanical attenuation of folding out-of-band interferers with a typical mechanical bandwidth of 100 Hz, together with a low enough noise level for 12-bit resolution for a $\pm$4-g dc acceleration signal in the 1 Hz mode, a sampling frequency of 4.096 kHz per mass was chosen. In the 25 Hz mode, a sampling frequency of 51.2 kHz is required for the same resolution.

From the reference voltage generation point of view, the original input voltage range of 1.0 V is effectively shrunk to 80 mV, due to the limited input signal range available for the front-end. In other words, the 16-bit accuracy is also demanded from the reference circuits. This has an adverse effect on the current consumption of the REFBUFs. A half least significant bit (LSB) step size of 9.77 μV can be calculated from the 80 mV full-scale range, when the resolution of 12 bits is required. By taking the signal bandwidths into account, the maximum allowed noise spectral densities of 9.77 and 1.954 $\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ can then be calculated for the 1 and 25 Hz modes, respectively. When assuming the noise to be white and allocating half of the noise budget for the reference voltage generation, the maximum allowed rms noise in the reference voltages can be evaluated by integrating over the Nyquist bandwidths of 1.024 kHz for the 1 Hz mode and 12.8 kHz for the 25 Hz mode. This results in 220 and 156 μV for each of the two modes, respectively. The halving of the sampling frequencies per mass is caused by the chosen implementation of the chopper stabilization (CS) in the front-end.

The attenuation of the used sinc^3 decimation filters is not allowed to be greater than 3 dB at the edge of the passband. Thus, the output data rate of the decimator was chosen to be 4 and 100 Hz in the 1 and 25 Hz modes, respectively. The decimator is equipped with shifters for gain control and 16-bit wide serial outputs to maintain the resolution even at the presence of uncompensated offsets.

The instantaneous error in the sampling, caused by rms jitter Δt in the clock signal, results in the signal-to-noise ratio of

$$SNR = -20\log(2\pi f \Delta t) \tag{1}$$

where f is the frequency of a sinusoidal input signal [25]. According to (1) the SNR is independent of signal amplitude. The maximum allowed jitter of the master clock signal can be approximated by solving Δt from (1). The maximum frequencies of the acceleration signals are 1 and 25 Hz in the two operating modes. Thus, the maximum allowed rms jitter values for 16-bit resolutions are 2.43 μs and 97 ns, respectively.

According to the simulations, the $\Delta\Sigma$ sensor front-end causes the worst case charge transition from the supply of the order of 50 pC in the 25 Hz mode [24]. This is caused by the tail-current-boosted Class AB operational amplifier used in the design [26]. As a consequence, the LDO must be able to supply large current peaks with quite slow settling times. The operation of the building blocks using the regulated supply voltages, except the operation of the decimator, was confirmed with the simulations down to 0.9 V. To avoid the use of off-chip load capacitors and to guarantee the maximum tolerable voltage drop of 100 mV at the LDO output ($\Delta V = \Delta Q/C$), the LDOs are equipped with programmable on-chip load capacitors up to 1 nF. Because of the low-power characteristic of the sensor interface, the LDOs must remain stable with zero load currents.

III. CIRCUIT DESIGN

In this section, the designed building blocks, namely the $\Delta\Sigma$ sensor front-end, the decimator, the frequency reference, the voltage and current reference, the reference voltage buffers, and the LDOs are presented.

A. $\Delta\Sigma$ Sensor Front-End

A schematic of the $\Delta\Sigma$ sensor front-end utilizing both chopper stabilization (CS) and correlated double sampling (CDS), together with a scanning electron microscope (SEM) photograph of the bulk-micromachined sensor element, is shown in Fig. 2(a). This fully single-ended configuration, based on a structure originally presented in [27], has been implemented and presented earlier in detail in [21]. It was chosen due to the following advantages: inherent capacitance-to-digital conversion, mechanical open-loop operation, and the charge balancing behavior that reduces the distorting effects of the nonlinear electrostatic forces.

The front-end uses two main clock phases, A and B, and three main mass selection phases, Mn, n being the index of the proof mass (1–3). In phase A, the mass being read is charged to a proper reference voltage and the first integrator samples the offset and flicker noise of the operational amplifier. Simultaneously, the second integrator feeds the sampling capacitor of the comparator. In phase B, the charge of the mass being read is integrated in the first integrator and the second integrator samples the new output voltage of the first integrator. Additionally, the comparator resolves a new output bit and the digital-to-analog converter (DAC) capacitor of the second integrator is charged to either reference voltage as determined by the new output bit. The second integrator performs the charge transfer while the other masses are read. The positive and negative reference voltages, REFP and REFN, are equal to the supply and ground. In order to manage with the low supply voltage of 1.0 V, the input and output common-mode levels of the operational amplifiers, CM_IN and CM_OUT, are separated to 0.1 and 0.5 V, respectively.

To minimize power dissipation, a tail-current-boosted Class-AB operational amplifier [26] with enhanced dc gain [21] is used in the first integrator. The operational amplifier used in the second integrators is a basic current mirror OTA, whose dc gain is enhanced with the same technique. The simulated dc gains of the two amplifiers are approximately 50 and 45 dB, respectively. A dynamic latch with zero static power dissipation is used as a comparator. Due to the low supply voltage, the gate voltage of an NMOS device in a floating transmission gate is increased to $2 \cdot V_{DD}$ using charge pumps [21]. The symbol $2\times$ is used to indicate the gate-voltage-boosted switches in Fig. 2(a). As the node DMID is especially sensitive to leakage currents, a special ultra-low-leakage switch [21] denoted by ULL in Fig. 2(a) was developed.

1) Transfer Function Analysis: Next, the operation of the front-end is analyzed in more detail by considering a single mass. Because of the structure of the front-end, the average charges flowing from both detection capacitors C_{DP} and C_{DN} are equal but of opposite polarity. As the voltages sampled to both capacitors are equal, the smaller of the two detection capacitors is sampled more often. Every second time, because of the use of CS, the masses are read with inverted references. The two chop phases, P and N, are processed separately in the front-end. The required demodulation, which is realized in this implementation by subtraction of two subsequent output values from each other, is performed in the decimator.

Fig. 2(b) illustrates the charge transfer from the detection capacitors to the first integrator. The average sampled charges in the positive and negative chop phase can be written as

$$\overline{Q}_{P,CDP} = -C_{DP}(1-\overline{B}_P)V_{R+} \tag{2}$$

$$\overline{Q}_{P,CDN} = C_{DN}\overline{B}_P V_{R-} \tag{3}$$

$$\overline{Q}_{N,CDP} = C_{DP}\overline{B}_N V_{R-} \tag{4}$$

$$\overline{Q}_{N,CDN} = -C_{DN}(1-\overline{B}_N)V_{R+} \tag{5}$$

where C_{DP} and C_{DN} are the detection capacitances, $\overline{B}_P$ and $\overline{B}_N$ the bit averages for positive and negative chop phases, and V_{R+} and V_{R-} the detection bias voltages, as defined in Fig. 2(b).

As was already mentioned, the front-end guarantees that $\overline{Q}_{P,CDP} = -\overline{Q}_{P,CDN}$ and $\overline{Q}_{N,CDP} = -\overline{Q}_{N,CDN}$. By substituting (2)–(5) into these equalities and by assuming identical detection bias voltages, $V_{R+} = V_{R-} = V_R$, the following equations for the bit averages can be solved

$$\overline{B}_P = \frac{C_{DP}-C_{DN}}{2(C_{DP}+C_{DN})} + \frac{1}{2} \tag{6}$$

$$\overline{B}_N = -\frac{C_{DP}-C_{DN}}{2(C_{DP}+C_{DN})} + \frac{1}{2} \tag{7}$$

that are independent of V_R. The terms 1/2 are caused by the fact that $\overline{B}_P$ and $\overline{B}_N$ vary between 0 and 1. After the demodulation, the output can be written as

$$\overline{B}_{OUT} = \overline{B}_P - \overline{B}_N = \frac{C_{DP}-C_{DN}}{C_{DP}+C_{DN}}. \tag{8}$$

If the detection capacitors are modeled as simple parallel-plate capacitors, their capacitances under acceleration can be written as

$$C_{DP} = \frac{A\varepsilon_r\varepsilon_0}{d-\Delta d} = C_0\left(\frac{d}{d-\Delta d}\right) \tag{9}$$

$$C_{DN} = \frac{A\varepsilon_r\varepsilon_0}{d+\Delta d} = C_0\left(\frac{d}{d+\Delta d}\right). \tag{10}$$

Here, A is the plate area, ε_r the relative permittivity of the insulator (1 for dry air and vacuum), ε_0 the permittivity of a vacuum, d the initial distance between the capacitor plates, Δd the change in plate distance induced by acceleration, and C_0 the capacitance with $\Delta d = 0$. By substituting (9) and (10) into the dc transfer function (8), the equation

$$\overline{B}_{OUT} = \frac{\Delta d}{d} \tag{11}$$

is obtained. This equation shows that the output of the front-end is ratiometric, in other words, the output is linearly proportional to Δd, and hence to the acceleration.

The effects of the nonideal V_{R+} and V_{R-} can also be studied using the aforementioned method. A common-mode error ΔV_C of the detection bias voltages, $V_{R+} = V_R + \Delta V_C$ and $V_{R-} = V_R + \Delta V_C$, is fully cancelled leading to (11). This can be verified simply by substituting the detection bias voltages with the common-mode error into (2)–(5) and then by resolving (6)–(8) and (11). In the case of a differential error ΔV_D, defined as $V_{R+} = V_R + \Delta V_D$ and $V_{R-} = V_R - \Delta V_D$, the bit average at the output after the demodulation becomes

$$\overline{B}_{OUT} = \frac{\Delta d}{d\left(\frac{V_R^2}{V_R^2-\Delta V_D^2}\right) - \frac{\Delta d^2}{d}\left(\frac{\Delta V_D^2}{V_R^2-\Delta V_D^2}\right)}. \tag{12}$$

It can be assumed that $\Delta V_D^2 \ll V_R^2$. Therefore, the first term of the denominator is very close to d and the second term is very small, because also $\Delta d^2 \ll d$. As a result, this front-end circuit also suppresses the differential errors of the detection bias voltages. According to the above analysis, V_{R+} and V_{R-} do not directly affect the transfer function, which relaxes the accuracy requirements of the absolute reference voltage values.

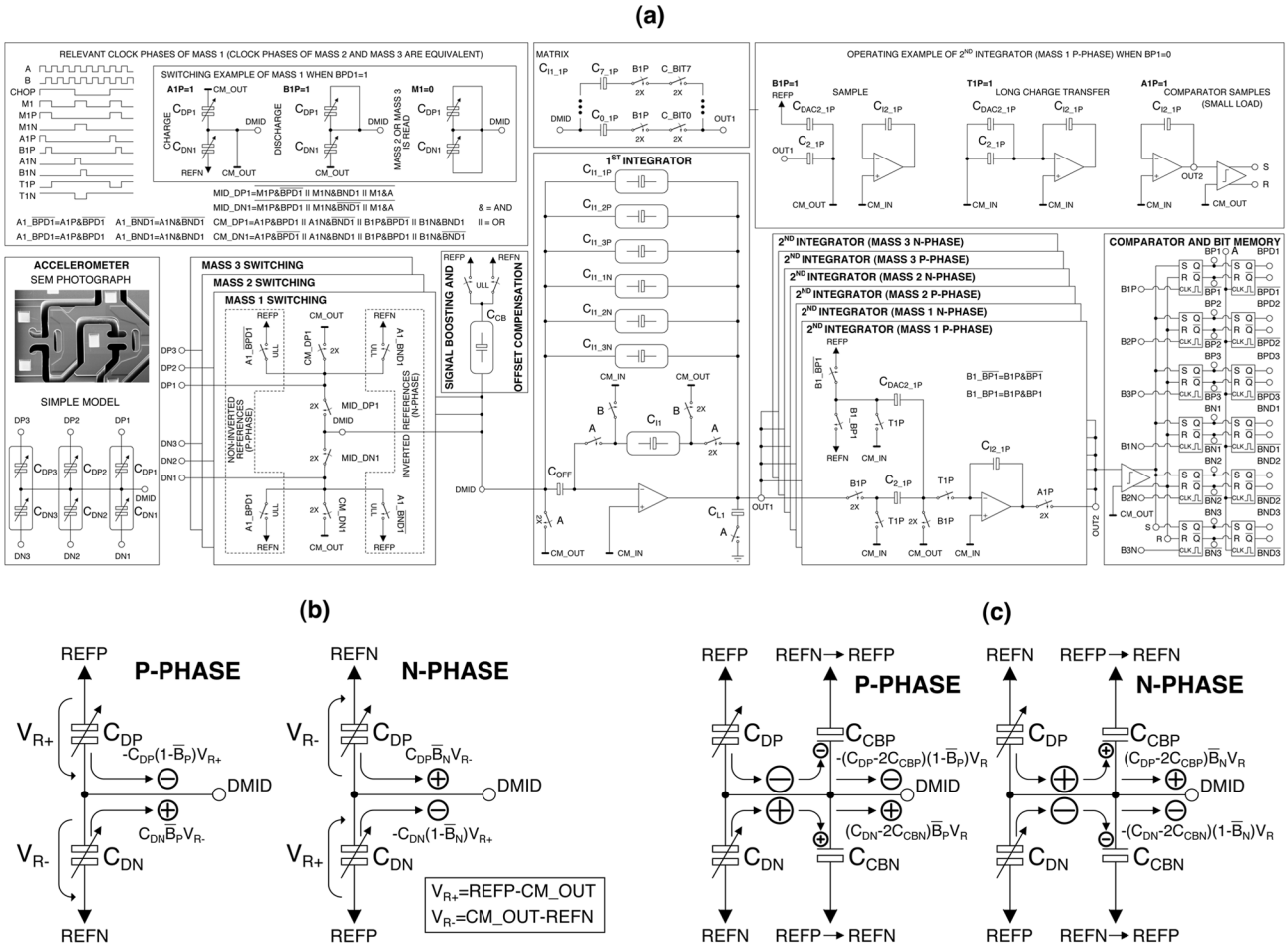

Fig. 2. (a) Schematic of the $\Delta\Sigma$ sensor front-end with an SEM photograph of a capacitive 3-axis micro-accelerometer (SEM image courtesy of VTI Technologies, Vantaa, Finland); (b) charge transfer from the detection capacitances to the first integrator, and (c) charge transfer from the detection capacitances to the first integrator, when the compensation and boosting capacitors C_{CBP} and C_{CBN} are used to sink charge.

The use of CS also has an effect on the low-frequency noise that comes from the reference and common-mode voltages. The sampled low-frequency noise is reduced by the demodulation.

2) Signal Boosting and Offset Compensation: The basic transfer function (8) can be modified by adding extra terms to both numerator and denominator. In this way, two convenient features can be achieved: first, decreasing the denominator in relation to the numerator boosts the available signal, and second, adding or subtracting a constant term from the numerator compensates for the offsets between the sensor capacitors. For this purpose, the front-end was provided with a programmable capacitor matrix C_{CB}. A single matrix is used for all three masses with different programming. It can be used to both sink charge from and source charge to the sensor middle electrode. The following analysis concentrates on the case of charge sinking. However, with small modifications, the same analysis can be repeated for the other case as well. Fig. 2(c) illustrates the charge transfers when the compensation and boosting capacitors, C_{CBP} and C_{CBN}, are used to sink charge. In that case, the new transfer function becomes

$$\overline{B}_{OUT} = \frac{C_{DP} - C_{DN} - 2(C_{CBP} - C_{CBN})}{C_{DP} + C_{DN} - 2(C_{CBP} + C_{CBN})} \tag{13}$$

in which the coefficients 2 result from switching the capacitors between REFP and REFN. According to (13), the signal boosting reduces the denominator of the transfer function, thus boosting the signal. To minimize the offset and distortion, the programmable capacitors C_{CBP} and C_{CBN} can be used to adjust separately the amounts of charges that are sunk from C_{DP} and C_{DN}, respectively. This minimization can be performed during the device test on the basis of individually measured offset and distortion. If $C_{CBP} \neq C_{CBN}$, charge is sunk more from one of the detection capacitors, and this way any offset in the sensor capacitors can be compensated for. By sinking charge from one side and sourcing it into the other side, offsets can also be compensated for without boosting the signal.

When the effect of the parasitic capacitances C_{PP} and C_{PN} in parallel to C_{DP} and C_{DN} is included, the transfer function can be rewritten as

$$\overline{B}_{OUT} = \frac{\Delta d}{d + \frac{(C_P + C_N)(d^2 - \Delta d^2)}{2C_0 d}} + \frac{C_P - C_N}{\frac{2C_0 d^2}{d^2 - \Delta d^2} + C_P + C_N} \tag{14}$$

where $C_P = C_{PP} - 2C_{CBP}$ and $C_N = C_{PN} - 2C_{CBN}$. The first term is the signal and the second one the offset. It can be seen that without the compensation, the parallel parasitics cause both offset and signal distortion. Conversely, the

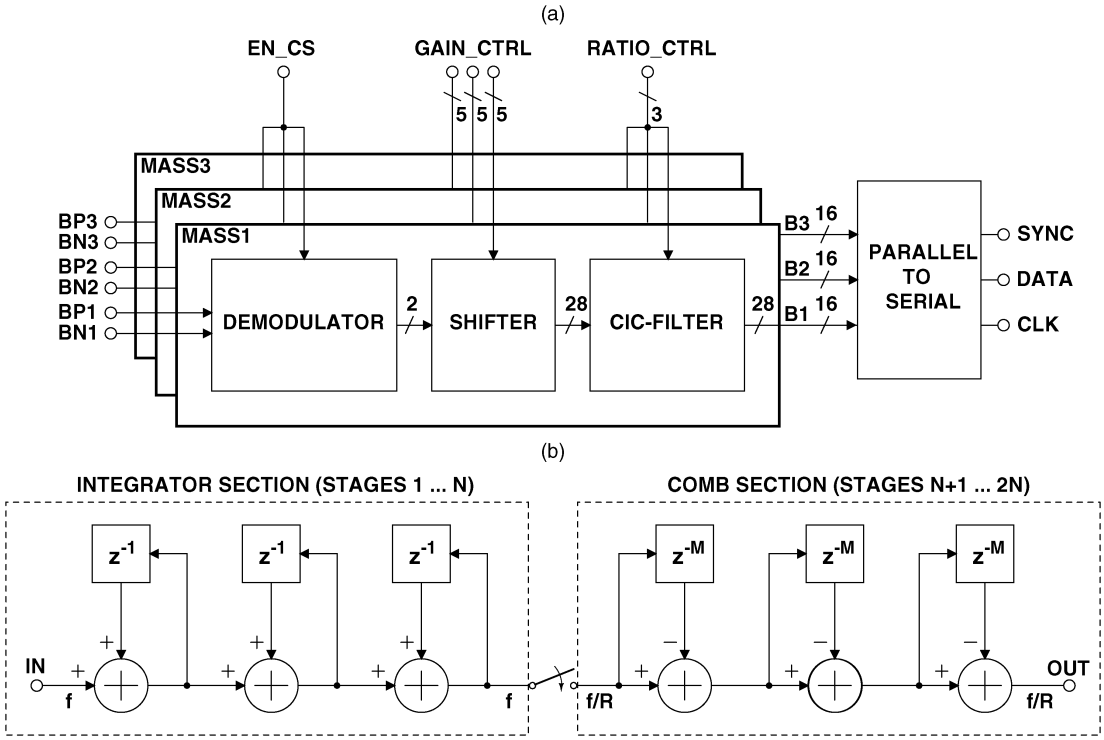

Fig. 3. (a) Simplified block diagram of the decimator, and (b) the structure of the used three-stage CIC filter [28].

matrix C_{CB} can be used to cancel both the offset and the nonlinearity caused by the parallel parasitics. The offset and distortion can be cancelled in this case by tuning the capacitors such that $C_{CBP} = 0.5C_{PP}$ and $C_{CBN} = 0.5C_{PN}$.

B. Decimator

The use of $\Delta\Sigma$-type sensor front-end requires the digital output signal to be decimated. Normally when using CS, the output bits of N-phases are inverted and interleaved with the output bits of P-phases. However, in this implementation, the demodulation is performed by subtracting the output bits of the N-phases from the output bits of the P-phases. Despite the fact that this kind of demodulation halves the data rate compared to the traditional demodulation approach, there are some advantages. First of all, the clock frequency can also be halved in the decimator, thus reducing its power dissipation by approximately a factor of two. Secondly, and more importantly, the implementation is more straightforward and the number of required registers is kept lower, thus reducing the silicon area.

The simplified block diagram of the designed decimator based on three parallel cascaded integrator-comb (CIC) filters [22], one for each proof mass, is shown in Fig. 3(a). Three-stage $(N = 3)$ CIC filters with one sample delays $(M = 1)$ and selectable rate change factor (R) are used. The structure of the CIC filter, shown in Fig. 3(b), is regular consisting of only integrators and comb circuits. These types of filters, commonly known as Hogenauer filters [28], are extremely area-efficient because they require neither multipliers, nor storage for filter coefficients. When the transfer functions of the integrators and differentiators are combined, the resulting transfer function of the filter becomes [28]

$$H(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} = \left(\sum_{k=0}^{RM-1} z^{-k} \right)^N \tag{15}$$

while its magnitude response is of the form

$$|H(f)| = \left| \frac{\sin(\pi M f)}{\sin\left(\frac{\pi f}{R}\right)} \right|^N. \tag{16}$$

In this design, each of the three filters has two 1-bit inputs and a 16-bit wide output. When the CS is not used the filters use only one input, otherwise the demodulation is performed by subtracting the two input bits from each other. After optional demodulations the signals can be scaled with shifters that provide an individual 5-bit gain control for each channel. The 3-bit decimation ratio control can be used to select the decimation ratio between 16 and 512, with each control step doubling the ratio. The outputs from the three filters are fed to a parallel-to-serial converter that outputs the 48 bits. Based on the measurement results [22] the decimator operates nominally using a 1.0 V supply in the 1 Hz mode, and a 1.8 V supply in the 25 Hz mode. The decimation ratios used are 512 and 256 in the 1 and 25 Hz modes, respectively. In the case of the designed filter, the attenuation of 3 dB occurs roughly at a half of the Nyquist frequency, to be exact at $0.523 \cdot f/(2R)$, while the attenuation at the Nyquist frequency is approximately 11.8 dB.

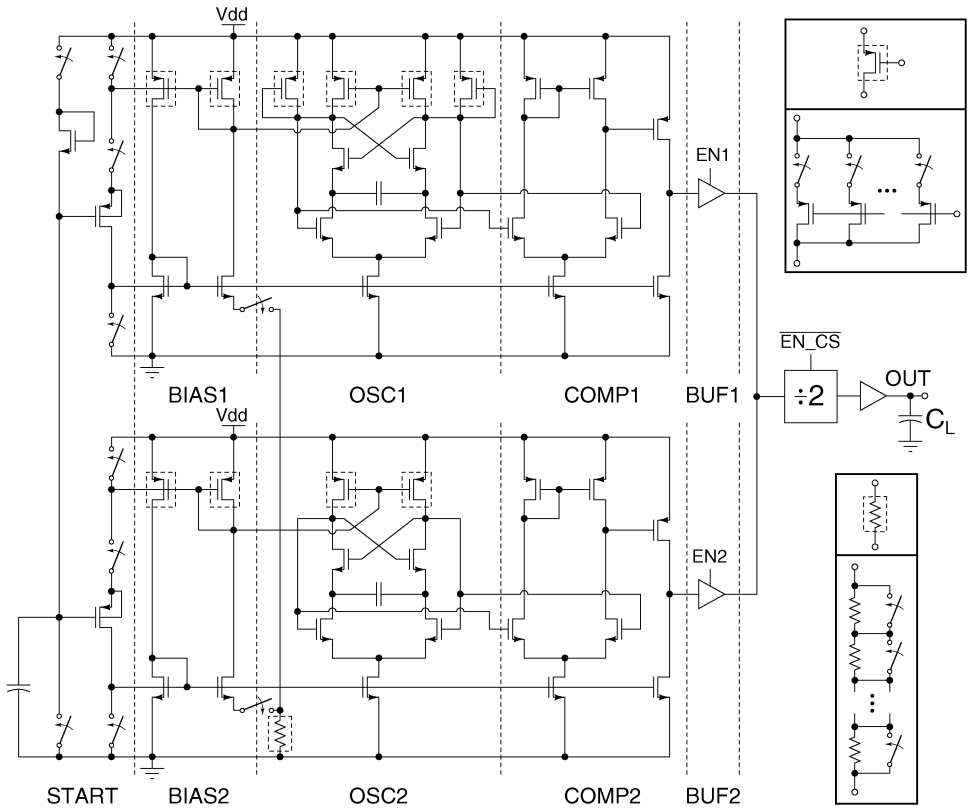

Fig. 4. Schematic of the designed frequency reference.

C. Frequency Reference

The specified master clock frequencies are 24.576 kHz and 307.2 kHz in the 1 and 25 Hz modes, respectively. The frequency reference that provides the master clock signal and which consists of two parallel source-coupled CMOS multivibrator-based structures, one for each mode, is shown in Fig. 4 [23], [29]. The use of only one structure with a single capacitor matrix in the multivibrator to provide coarse tuning over the both operating modes is not possible because of the low supply voltage of 1.0 V. The PMOS transistor matrices and one resistor matrix, outlined with dashed lines in Fig. 4, are used in both modes for coarse and fine tuning, respectively.

Symmetrical loads are used in the multivibrator of the 1 Hz mode to improve the frequency stability [23]. In the case of the multivibrator of the 25 Hz mode, a sufficient stability can also be achieved without the symmetrical loads, and they are thus excluded. To reduce the effect of possible clock interferences on the other building blocks, the frequency reference includes separate bias current generation. Two-stage differential comparators are used to magnify the oscillation amplitudes rail-to-rail, and tri-state buffers interface the parallel frequency references to the divider. Signal $\overline{\text{EN\_CS}}$ enables the divide-by-two operation when CS is not used. The capacitor C_L represents the capacitive load caused by the rest of the circuit.

D. Voltage and Current Reference

The schematics relating to the circuitry designed for the generation of the required reference voltages and currents and regulated supply voltages are shown in Fig. 5. A higher level simplified schematic is shown in the middle of the figure. The current reference IREF together with the bias voltage and current generation for the operational amplifiers are excluded from that for clarity.

The designed V/IREF shown at the top of Fig. 5 is based on the bandgap reference topology presented in [30], and can be implemented with a standard CMOS process. The resistive voltage dividers ($R_1 = R_{11} + R_{12} = R_{21} + R_{22} = R_2$) at the inputs of the Miller-compensated operational amplifier allow the use of supply voltages down to 1.2 V. The effects of process variations on the nominal output voltage level of 0.3 V can be eliminated by trimming R_3 using the provided resistor matrix. The output voltage is defined as [30]

$$V_{REF} = \frac{R_3}{R_1}\left[V_{EB1} + \frac{R_1}{R_0}\ln(N)V_T\right] \tag{17}$$

where R_0, R_1, and R_3 are resistances of the corresponding resistors, V_{EB1} is the emitter-base voltage of the bipolar transistor Q1, N the emitter area ratio, and V_T the thermal voltage. Nominally, the reference current I_{REF} is roughly 270 nA.

In order to achieve sufficient noise performance the bandwidth is limited aggressively by using the compensation capacitor C_C of 50 pF. As a result, the gain-bandwidth product (GBW) of the negative feedback loop is nominally 1.6 kHz. The matrices M1 and M2 enable the optimization of the current consumption of the bandgap reference and the LDOs, while the matrices M3 and M4 provide the programming of the bias currents of the sensor front-end amplifiers. The same kind of resistor and transistor matrix structures are used as in the case of the frequency reference shown in Fig. 4. The NMOS switches

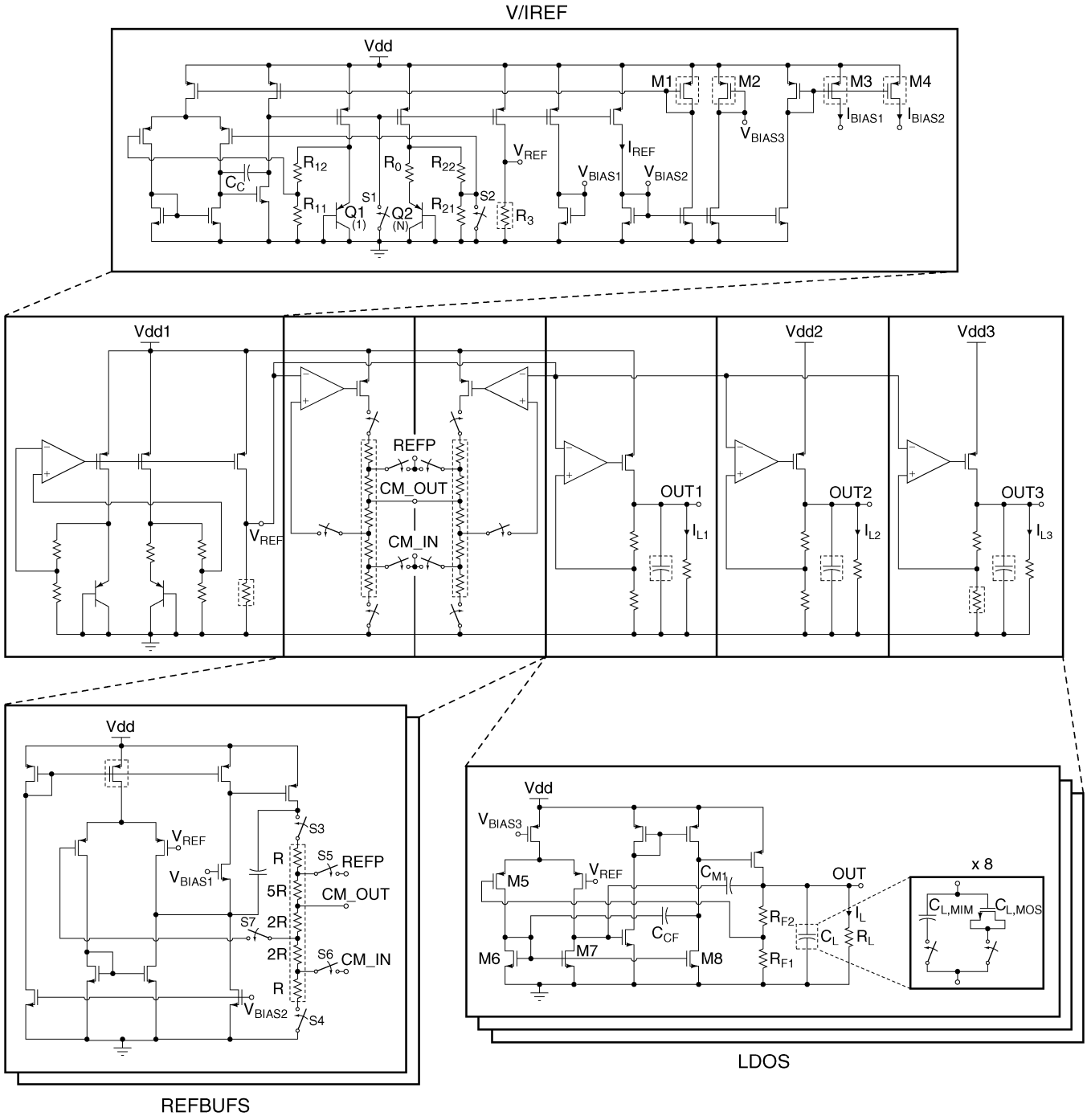

Fig. 5. Schematics of the circuitry designed for the generation of the required reference voltages and currents and regulated supply voltages: a higher level simplified schematic in the middle, the voltage and current reference at the top, a single reference voltage buffer at the bottom left, and an LDO at the bottom right.

S1 and S2 provide a power-on-reset that can be used to force the bandgap reference to the right operating point, if needed.

E. Reference Voltage Buffers

The reference voltage buffers are required to scale and buffer three different voltages from V_{REF}: $V_{REFP} = 1.0$ V, $V_{CM\_OUT} = 0.5$ V, and $V_{CM\_IN} = 0.1$ V, the use of which is illustrated in Fig. 2(a). These voltages are sampled by the front-end at the rate determined by the used operating mode. The REFBUFs, REFBUF1 for the 1 Hz mode and REFBUF2 for the 25 Hz mode, have identical schematics shown at the bottom left of Fig. 5, but different device parameters. Both the tail currents of the operational amplifiers and the resistive networks are programmable. The second stage of the three-stage amplifier operates as a level shifter.

Because only one of the two REFBUFs is used at a time, the switches S3–S7 are required to isolate the REFBUFs from each other. The switch S3 is a PMOS device whose bulk is connected to its source, the switches S4, S6 and S7 are NMOS devices, and S5 is a transmission gate. To guarantee the proper operation of S5 over the whole supply voltage range, the bulk of its PMOS device is connected to V_{BIAS1}. Time constants formed

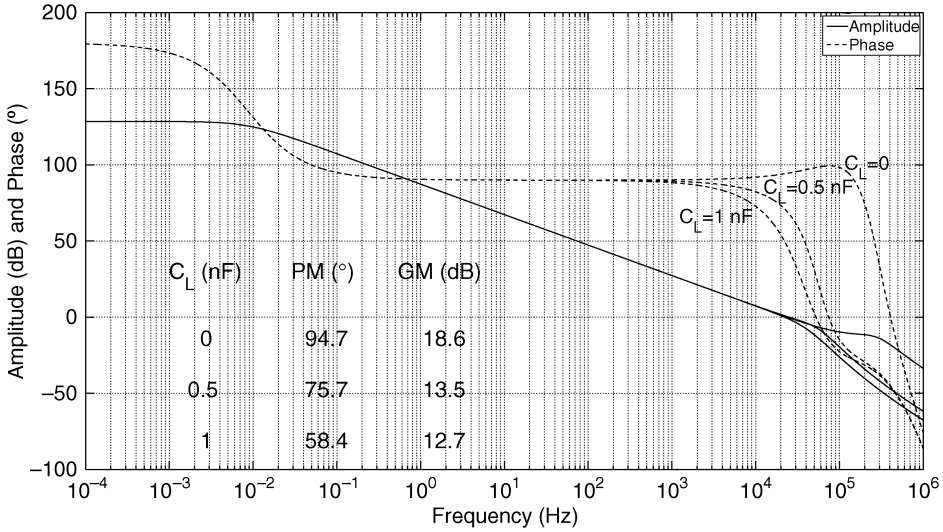

Fig. 6. Simulated loop responses of the LDO at zero load current with different load capacitances.

by the resistances of the resistive networks and the load capacitances caused by the front-end and the sensor element determine the settling accuracies. Two parallel resistive networks were included for both REFBUFs to enable the optimization of the current consumption according to the process corner and load capacitances. The used unit resistors (R) are 20 kΩ and 35 kΩ for the 1 Hz mode, and 1 kΩ and 2 kΩ for the 25 Hz mode. The resistive networks can also be used in parallel to further reduce R. According to the simulated loop responses, the dc gains and GBWs of the REFBUF1 with $R = 20$ kΩ and REFBUF2 with $R = 1$ kΩ are nominally 88.0 dB and 32.7 kHz, and 100.6 dB and 336.5 kHz, respectively. The currents flowing through the resistive networks dominate the current consumptions of the REFBUFs.

The front-end causes four different loading conditions depending on both the clock phase and the previous output bit. The load capacitance for the common-mode output voltage is particularly large. In the worst case it was estimated to be in the order of 30 pF. The worst case resistance of the designed front-end switches, used to sample the reference voltages, is 5 kΩ. There is a half clock period time for settling, corresponding to 40.7 μs and 3.3 μs in the 1 and 25 Hz modes, respectively. The residual error of 4.8 μV was used as the settling accuracy specification for each of the three reference voltages. As discussed in Section II, the maximum allowed rms noise levels are 220 μV for the 1 Hz mode, and 156 μV for the 25 Hz mode, when half of the noise budget is allocated for the reference voltage generation. The settling accuracy could be traded off with the noise performance by reducing the noise bandwidth, either by increasing compensation capacitance or adding extra filtering capacitance to the outputs.

F. LDOs

The LDO shown at the bottom right of Fig. 5 is based on the structure presented in [31]. It uses a Q-reduction technique to minimize both the required on-chip capacitance and the minimum output current. The transistors M5, M6, and M8 form a feedforward transconductance stage. The minimum output current level can be reduced by increasing the compensation capacitor C_{M1} for lowering the GBW. The Q-reduction circuit is formed by the compensation capacitor C_{CF} and a current buffer formed by M6 and M7. The capacitor C_L and resistor R_L represent the equivalent load capacitor and resistor caused by the rest of the circuitry. In the case of the LDO3, the resistor R_{F1} was implemented as a matrix to enable the programming of the supply voltage required by the decimator.

To guarantee the maximum tolerable voltage drop of 100 mV at the LDO output, the LDOs are equipped with programmable on-chip load capacitors up to 1 nF. In this design, the nominal component values of the other passive devices are $C_{M1} = 6.5$ pF, $C_{CF} = 1.5$ pF, $R_{F1} = 150$ kΩ, and $R_{F2} = 350$ kΩ. The worst case condition for stability happens at zero load current, $I_L = 0$, and at maximum load capacitance, as can be seen from the simulated loop response curves of the LDO shown in Fig. 6. Nominally, $C_L = 0.5$ nF is used for all LDOs. The typical dc gain and GBW are 131.0 dB and 18.5 kHz, respectively. The phase and gain margins (PM and GM) are improved when the load current is increased.

To minimize the silicon area required by the programmable 1 nF load capacitors, metal–insulator–metal (MIM) capacitors were stacked above standard MOS capacitors. A load capacitor unit, also shown in the LDO schematic of Fig. 5, consists of one MIM capacitor of 70 pF $(C_{L,MIM})$ and one NMOS capacitor of approximately 55 pF $(C_{L,MOS})$, thus providing a total capacitance of 125 pF in an area of roughly 0.016 mm^2. NMOS switching devices with the W/L ratios of 100 μm/0.25 μm are used for programming. Each LDO includes eight load capacitor units and thus their load capacitances can nominally be adjusted at 55 or 70 pF steps over the whole capacitance range from 0 to 1 nF.

IV. Measurement Results

The prototype sensor interface chip with a 1.73 mm^2 active core area shown in Fig. 7 was fabricated in a 0.25-μm CMOS technology using MIM capacitors and high-resistivity

TABLE II
DISTRIBUTIONS OF THE CURRENT CONSUMPTION AND ACTIVE SILICON AREA

Circuit block	Primary supply	Current consumption in 1 Hz mode				Current consumption in 25 Hz mode				Silicon area	
		Including LDOs		Excluding LDOs		Including LDOs		Excluding LDOs			
		(μA)	(%)	(μA)	(%)	(μA)	(%)	(μA)	(%)	(mm^2)	(%)
$\Delta\Sigma$ sensor front-end	Vdd1	1.1	5.4	1.1	11.0	20.0	20.7	20.0	23.8	0.45	26.1
Decimator	Vdd3	0.2	1.0	0.2	2.0	2.0	2.1	2.0	2.4	0.25	14.5
FREF	Vdd2	0.2	1.0	0.2	2.0	0.8	0.8	0.8	1.0	0.04	2.3
CLKG	Vdd2	0.1	0.5	0.1	1.0	0.5	0.5	0.5	0.6	0.08	4.6
V/IREF	Vdd1	4.8	23.8	4.8	48.0	8.6	8.9	8.6	10.2	0.19	11.0
REFBUF1	Vdd1	3.6	17.8	3.6	36.0	–	–	–	–	0.06	3.5
REFBUF2	Vdd1	–	–	–	–	52.1	54.0	52.1	62.0	0.06	3.5
LDO1	Vdd1	3.4	16.8	–	–	3.4	3.5	–	–	0.20	11.6
LDO2	Vdd2	3.4	16.8	–	–	3.4	3.5	–	–	0.20	11.6
LDO3	Vdd3	3.4	16.8	–	–	5.6	5.8	–	–	0.20	11.6
TOTAL		**20.2**		10.0		**96.4**		84.0		**1.73**	

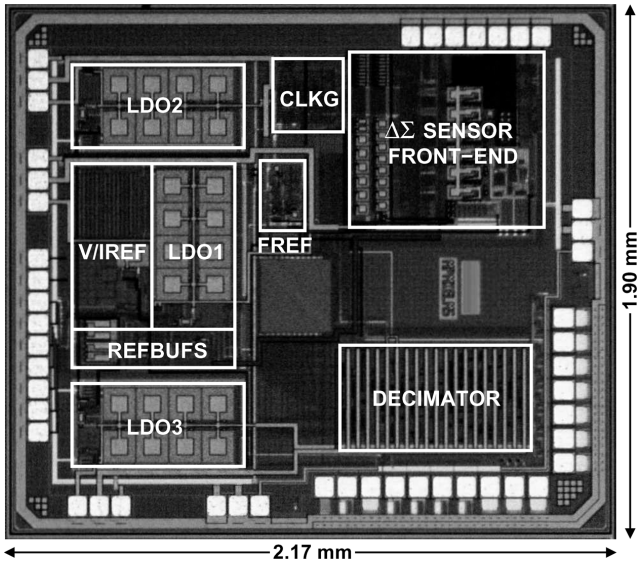

Fig. 7. Microphotograph of the implemented sensor interface chip.

polysilicon resistors. The total die area including bonding pads is 4.12 mm^2. For the measurements, the chip was encapsulated into a plastic quad flat package (QFP) with 64 pins and soldered onto a printed circuit board (PCB). The chip was combined with an external, encapsulated, bulk-micromachined capacitive 3-axis accelerometer with a nominal acceleration range of $\pm$4-g on the PCB.

The distributions of the current consumption and active silicon area are shown in Table II. To reduce interference conducting through the supply rail, the primary supply voltage, which is nominally 2.5 V and ranges from 1.2 to 2.75 V, is divided into three separate but identical supply regions, Vdd1, Vdd2, and Vdd3, as indicated in the middle of Fig. 5. It is not possible to directly measure the current consumptions of the individual building blocks. Thus, the current consumptions listed in the table are simulated values. In order to arrive at comparable results, the chip was programmed equally during the simulations and the measurements. The measured overall current consumptions from Vdd1...3, reported later in Table III, agree well with 4.7% and 1.2% accuracies when compared with the corresponding simulations in the 1 and 25 Hz modes, respectively. The effect of the quiescent currents of the LDOs on the total current consumption can be seen by comparing the columns including/excluding LDOs.

In the 1 Hz mode, the V/IREF, the REFBUF1, and the LDOs together dominate the current consumption by consuming 18.6 μA, which is 92% from the total current consumption of 20.2 μA. The reason for this kind of current distribution is that the major part of the currents of the V/IREF and LDOs are not scalable with frequency. Furthermore, a high resolution is required for the reference voltage generation. When the LDOs in the 1 Hz mode are excluded, the total current consumption is reduced to 10.0 μA and it is clearly dominated by the V/IREF and the REFBUF1. The remaining building blocks, that is, the $\Delta\Sigma$ sensor interface including the decimator, the FREF, and the CLKG, consume together only 1.6 μA. In the 25 Hz mode, the REFBUF2 consumes over half of the total current of 96.4 μA, though the current flowing through the resistive network is minimized. The relative part of the $\Delta\Sigma$ sensor front-end is almost quadrupled compared to the 1 Hz mode because of the higher sampling frequency, while the relative effect of the quiescent currents of the LDOs on the total current consumption is reduced considerably compared to the 1 Hz mode. The $\Delta\Sigma$ sensor front-end occupies most of the active silicon area, that is, 26.1% of the total active area of 1.73 mm^2.

Next, the most essential measurement results are presented, first for the individual building blocks, and then for the whole sensor interface system. All the results, including the individual building blocks, were measured by using on-chip references and on-chip power management. Unless otherwise mentioned, the primary supply voltage was 2.5 V, the LDO1 and LDO2 had fixed output levels of 1.0 V, and the output of the LDO3 was programmed to the level of 1.8 V. Additionally, the load capacitors at the outputs of the LDOs were programmed to their nominal

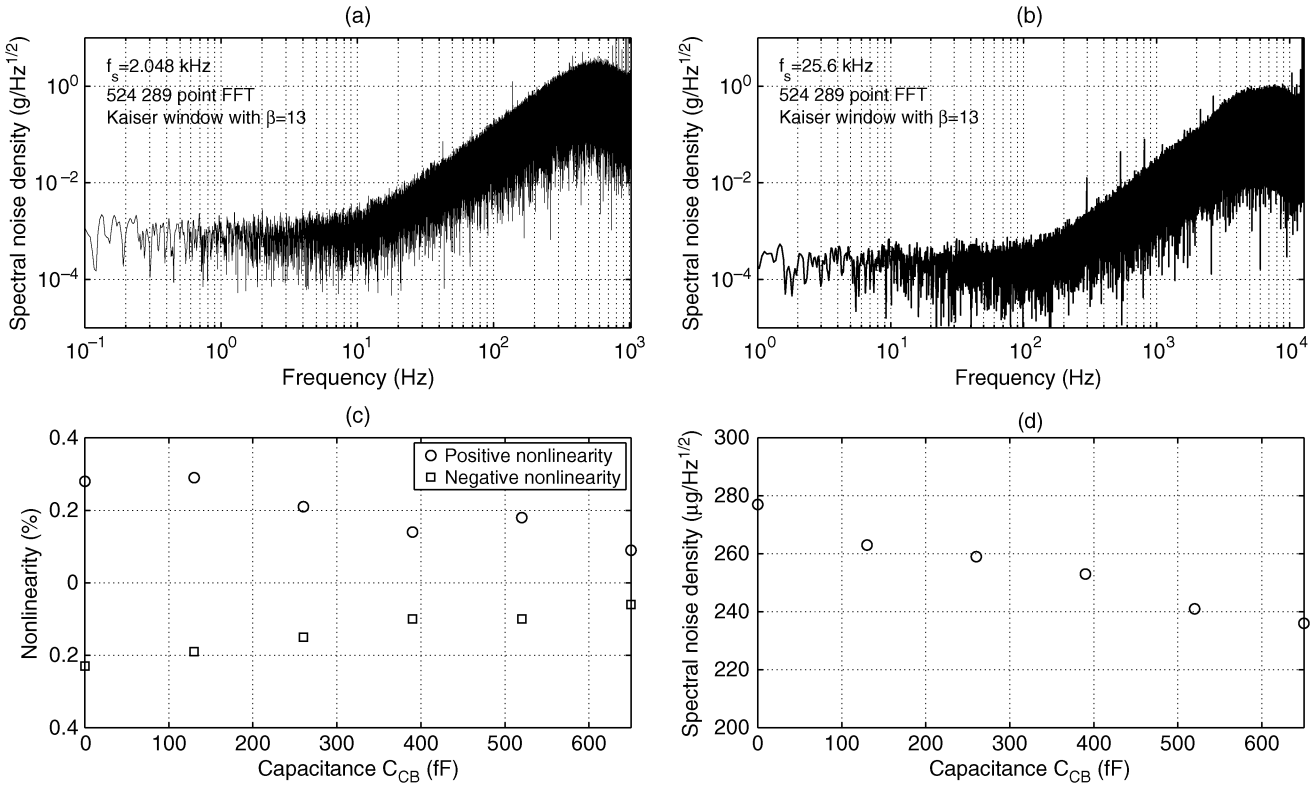

Fig. 8. FFTs of (a) x-directional data in the 1 Hz mode and (b) z-directional data in the 25 Hz mode. 524 289-point FFT, Kaiser window with $\beta = 13$, sampling frequencies of 2.048 and 25.6 kHz in the 1 and 25 Hz modes, respectively. The measured (c) $-4\ldots0$-g range nonlinearity and (d) spectral noise density, both measured for z-direction in the 25 Hz mode, as a function of the compensation and boosting capacitance C_{CB}.

values of 0.5 nF. The CS and CDS were used in the $\Delta\Sigma$ sensor front-end throughout the measurements, but the signal boosting and offset compensation method was used only in some measurements, and thus its use is stated in the context. Both the front-end and system measurements were performed by using the off-chip $\pm$4-g capacitive 3-axis accelerometer. The off-chip sensor element was replaced with integrated capacitors when the capacitance sensitivity of the $\Delta\Sigma$ sensor front-end was determined.

A. $\Delta\Sigma$ *Sensor Front-End*

FFTs of x-directional data in the 1 Hz mode and z-directional data in the 25 Hz mode, both measured from the output of the $\Delta\Sigma$ sensor front-end, that is, without the decimator, are shown in Figs. 8(a) and (b), respectively. The effect of the compensation and boosting capacitance, $C_{CBP} = C_{CBN} = C_{CB}$, on both linearity and noise was studied for z-direction in the 25 Hz mode and the results measured from the output of the decimator are presented in Figs. 8(c) and (d), respectively. The effect of the C_{CB} on the nonlinearity was measured with accelerations ranging from -4 to 0-g, since the measurement of one side of the acceleration ramp was considered to be sufficient when studying the relative change in nonlinearity and noise. According to Fig. 8(c) the nonlinearity (% from full-scale of $\pm$4-g) is improved as a function of C_{CB}, which is in agreement with the analysis presented in Section III-A2. The measured noise results indicate that by increasing C_{CB} the spectral noise density is slightly reduced as shown in Fig. 8(d).

The capacitance sensitivity of the $\Delta\Sigma$ sensor front-end was determined for both operating modes by using integrated capacitors in place of the off-chip sensor element. When all the detection capacitances C_{DP} and C_{DN} were replaced with the integrated capacitors of 3 pF, the average noise floors measured from the output of the front-end were -100.7 and -110.8 dB/Hz for the 1 and 25 Hz modes, respectively (the single-ended input capacitance ranges from 0 to 6 pF). These correspond to single-ended capacitance resolutions of 55.4 and 17.3 aF/$\sqrt{\text{Hz}}$ for the static capacitances of 3 pF. Next, by using (8) with $C_{DP} = C_0 + \Delta C$ and $C_{DN} = C_0 - \Delta C$, it can be calculated that the required single-ended sensitivities $\Delta C/\Delta a$ for 12-bit resolution for a $\pm$4-g dc acceleration signal have to be 28.4 and 44.3 fF/g for the 1 and 25 Hz modes, respectively. These sensitivities are below the corresponding minimum sensitivities of the sensor element, i.e., 50 fF/g. However, it must be noted that in the system measurements the sensor element was encapsulated and connected with the interface IC on the PCB. Accordingly, the parasitic capacitances, and thus also the static capacitances, are significantly increased.

B. *Frequency Reference*

According to the measured frequency reference calibration curves, a sufficiently large tuning range can be achieved in both modes to cover process variations. At room temperature the calibrated master clock frequencies were 24.56 kHz and 310.2 kHz in the 1 and 25 Hz modes, respectively. Temperature dependency of the oscillation frequency measured in the 1 Hz mode is shown in Fig. 9(a). Temperature stability, determined

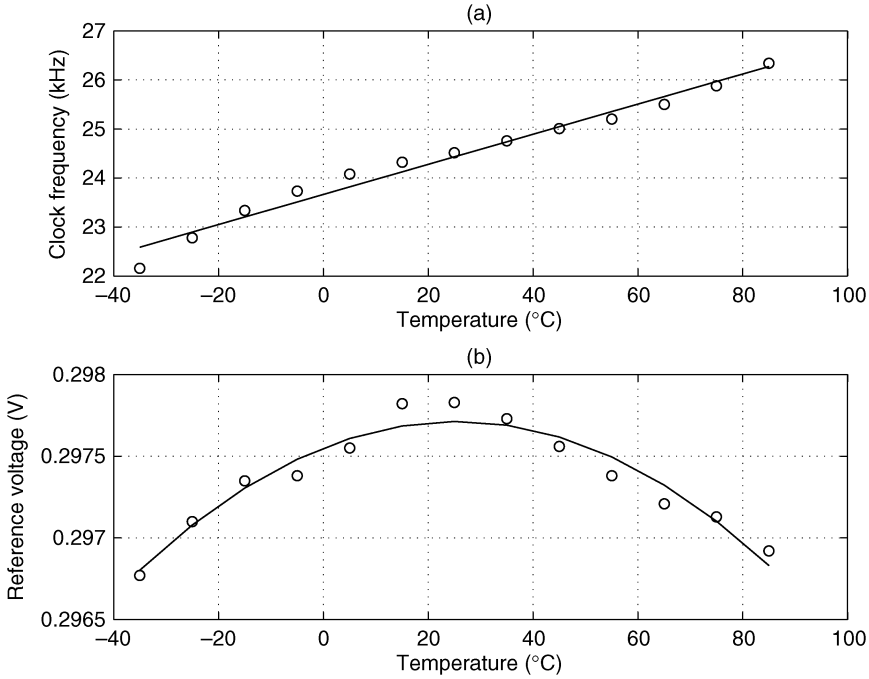

Fig. 9. Measured temperature dependencies of (a) the master clock frequency in the 1 Hz mode and (b) the reference voltage V_{REF}.

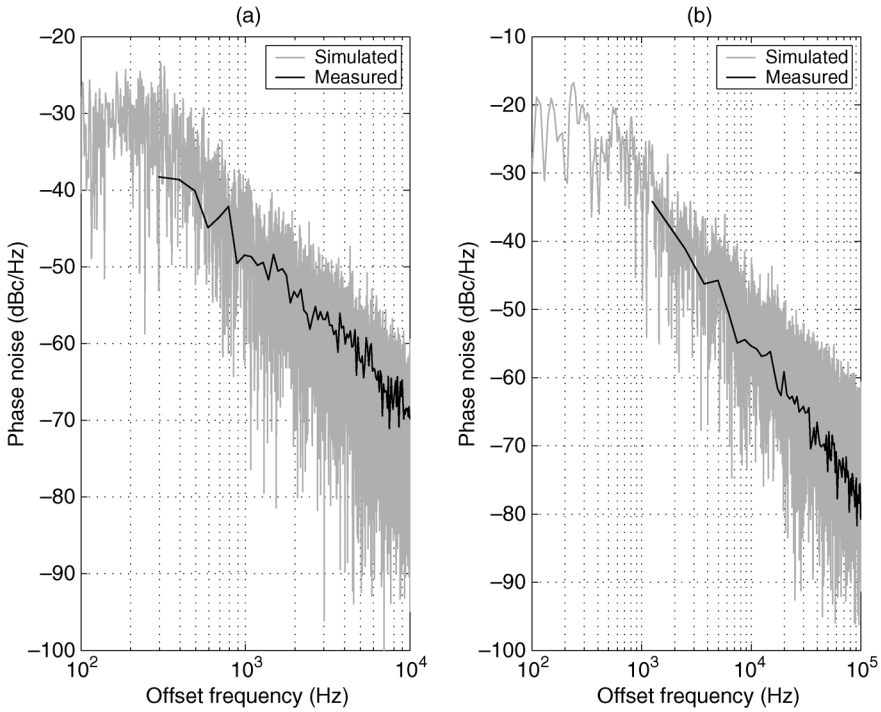

Fig. 10. Simulated and measured phase noise spectra of the frequency reference in the (a) 1 and (b) 25 Hz modes.

according to the plotted linear fitting curve, is $+7.5/-8.2\%$ when extrapolated down to -40°C. The measured supply voltage stability over the supply voltage range from 0.9 to 1.1 V is $+0.05/-3.8\%$. In the 25 Hz mode, the measured temperature and supply voltage stabilities are $+5.1/-13.0\%$ and $+0.8/-9.8\%$, respectively.

The simulated and measured phase noise spectra obtained at room temperature correlate well with each other, as shown in Figs. 10(a) and (b) for the 1 and 25 Hz modes, respectively. The simulated spectra were obtained from transient noise simulations. The measured phase noise levels are -68 dBc/Hz at 10 kHz and -77 dBc/Hz at 100 kHz offset frequencies from the carrier in the 1 and 25 Hz modes, respectively. These phase noise values, determined from the white noise regions with slopes of -20 dB/dec, can be converted to cycle-to-cycle jitters by using the equation

$$\Delta t_{cc} = \frac{\Delta f}{f_0^{1.5}} 10^{L\{\Delta f\}/20} \tag{18}$$

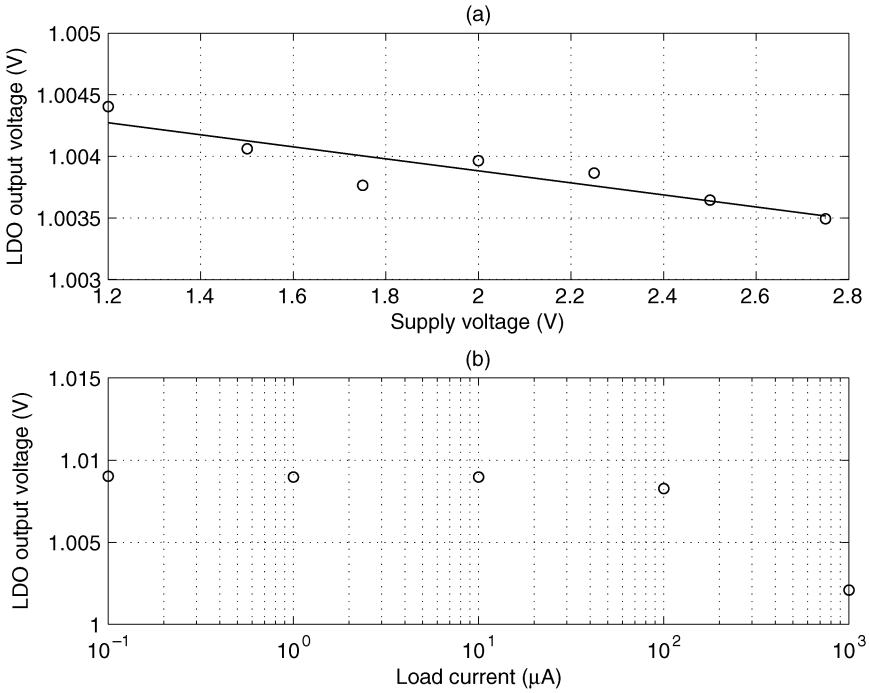

Fig. 11. Measured (a) line and (b) load regulation of the LDO.

where Δf is the offset frequency from the carrier, f_0 the oscillation or carrier frequency, and $L\{\Delta f\}$ the phase noise at certain offset frequency from the carrier in decibels [32]. The cycle-to-cycle jitters of 1.03 μs and 82 ns can be evaluated for the 1 and 25 Hz modes, respectively. These jitter values closely fulfill the requirements stated in Section II.

C. Voltage and Current Reference

The reference voltage varies linearly as a function of the resistance R_3 according to (17). The smallest step of R_3 is nominally 2 kΩ, which changes the reference voltage by approximately 1.6 mV. In the measurements R_3 was set to 372 kΩ. Fig. 9(b) shows the reference voltage measured over the temperature range. According to the second-order fitting curve, a temperature coefficient of 28.8 ppm/°C can be calculated. The rms output noise of the voltage reference measured from the bandwidth ranging from 1 Hz to 100 kHz is 186.1 μV, which is roughly 10 μV higher than the corresponding simulated one. The reference current cannot be measured directly but its value can be assumed to be close to the nominal value of 270 nA, because the measured current consumptions of the whole sensor interface agree well with the simulated ones, as discussed earlier.

D. LDOs

The measured line and load regulation of the designed LDO are shown in Figs. 11(a) and (b), respectively. The line regulation over the supply voltage range predicted by the linear fitting curve is approximately 0.5 mV/V. The load regulation is 6.9 mV/mA. The unloaded output voltage levels of Figs. 11(a) and (b) differ from each other because the line regulation was measured from the LDO1 and the load regulation from the LDO2. The LDO2 was used in the load regulation measurement as it made it possible to extend the measurement range towards smaller load currents by powering down the FREF, and thus also the CLKG.

The largest average current that one LDO must supply in this application is in the order of 20 μA ($\ll$1 mA). The power supply rejection ratios (PSRRs) of the designed bandgap reference and therefore that of the LDO are low because of the required aggressive noise bandwidth limitation. The measured PSRR+ at the output of the LDO is 11.1 dB at 100 Hz and 25.5 dB at 1 kHz. In the system measurements, only half of the total load capacitance was used at the output of each LDO. By halving the capacitor bank of each LDO a total area saving of approximately 0.19 mm^2 could be achieved. Additionally, from a silicon area and power dissipation point of view, it would be better to tailor each LDO individually, instead of using three identical LDOs.

E. System Measurements

FFTs and root Allan variances [33] were measured from the output of the decimator for both 1 and 25 Hz modes. The FFTs measured for z-directional data are shown in Figs. 12(a) and (b), and the root Allan variances measured for y-directional data in (c) and (d), respectively. The spectra were smoothed by using a moving average of 11 points. The measured data were scaled by the dc gains of the system in both operating modes. The attenuation of the decimation filter can clearly be seen in the frequency range between the signal bandwidth and the Nyquist frequency. The insets of the root Allan variance plots show the time domain curves. A dashed line with an ideal slope of $-1/2$ in the white noise region has been plotted for both modes, and the obtained long-term bias stabilities are included for each direction. The thermal noise floors read from the Allan plots correspond to those obtained from the spectra. In the 1 Hz mode, the level of the long-term bias stability clearly affects the slope of the root Allan variance plot at short averaging times. The flattening of

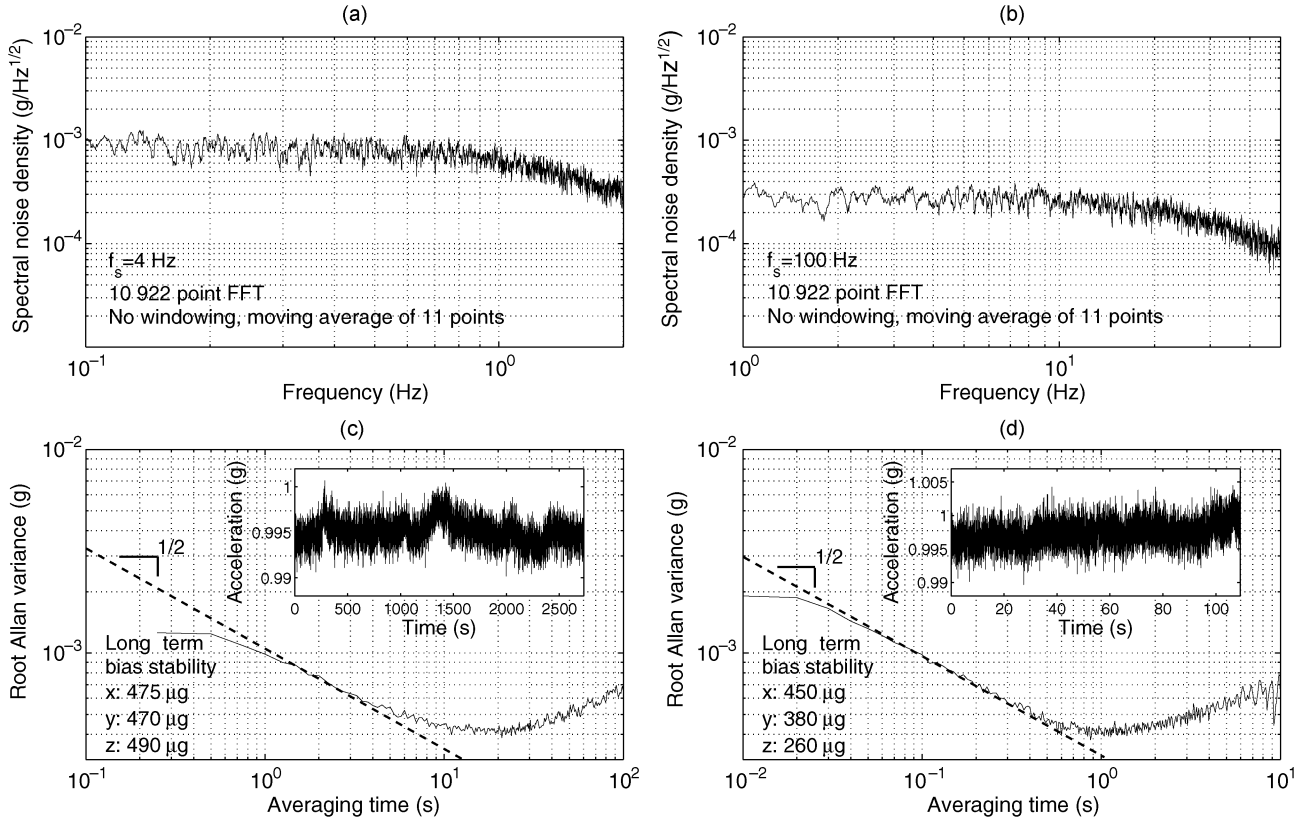

Fig. 12. FFTs of data measured from the output of the decimator for z-directional data in the (a) 1 and (b) 25 Hz modes. 10 922-point FFT, no windowing, moving average of 11 points, sampling frequencies of 4 and 100 Hz in the 1 and 25 Hz modes, respectively. Root Allan variances measured for y-directional data in the (c) 1 and (d) 25 Hz modes.

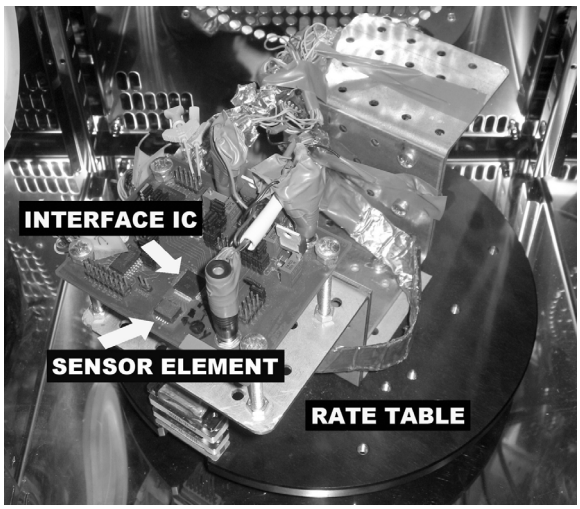

Fig. 13. PCB mounted on the rate table.

the root Allan variance plots at the shortest averaging times is caused by the low-pass decimation filter.

The functionality of the sensor interface was verified by exciting the system with -4-g$\ldots+4$-g dc accelerations. Accelerations were generated on a rotating rate table. The used measurement setup is shown in Fig. 13. Centrifugal acceleration $a = r\omega^2$, where r is the distance of the sensor element from the center of the rate table and ω the angular velocity, was used to excite the sensor in all three sensitive directions, one at the time. The measured $\pm$4-g dc ramps with ideal curves and the worst case nonlinearities (% from full-scale range) for the 1 and 25 Hz modes are shown in Figs. 14(a) and (b), respectively. The nonlinearity results are very similar for both modes, in the order of $\pm 0.35\%$ for the $\pm$4-g range. The positive and negative ramps for all of the three directions were measured separately. Each of the positive and negative ramps were calibrated by removing offsets and gain errors, after which the ramps of each direction were combined and the nonlinearities were determined by using the best fit straight line method.

The performance measured for both modes using a 2.5 V supply voltage and 0.5 nF load capacitors at the outputs of the LDOs is summarized in Table III. All the results were measured by using both CS and CDS, but without using signal boosting and offset compensation. The core circuit consumes 21.2 μA in the 1 Hz mode and 97.6 μA in the 25 Hz mode. The noise results yield dynamic ranges of 76 and 73 dB for a $\pm$4-g dc signal range in the 1 and 25 Hz modes, respectively. In general, the results are expected to improve when the interface IC is bonded directly to the sensor, as this significantly reduces the parasitic capacitances.

The functionality of the IC was verified also by using a primary supply voltage of 1.2 V at room temperature. The regulated output of the LDO3 was then programmed to the same level with the other two LDOs, i.e. 1.0 V. In other words, the V/IREF, the REFBUFs, and all the LDOs operated directly from

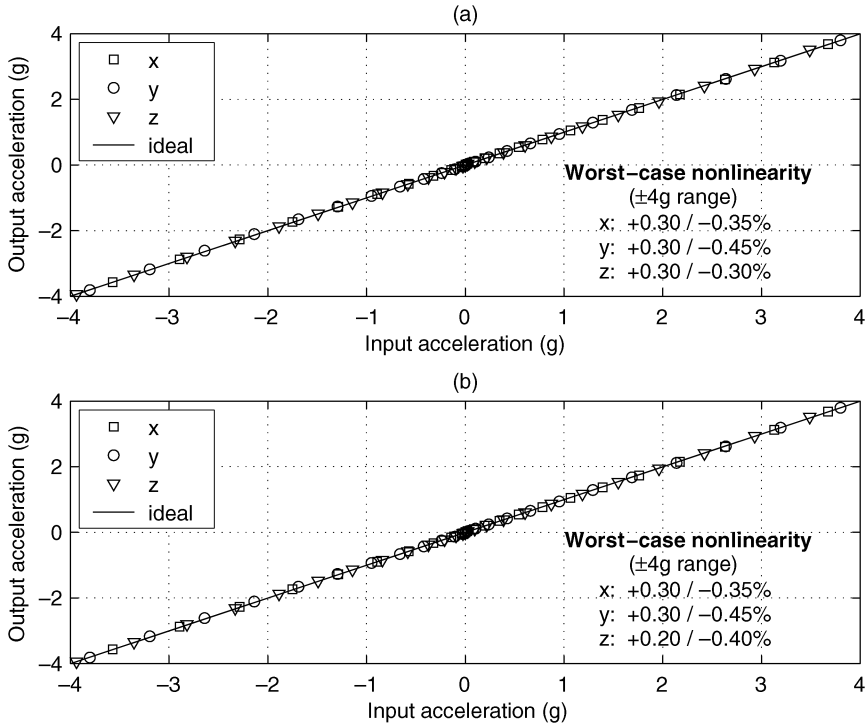

Fig. 14. Measured ±4-g acceleration ramps in the (a) 1 and (b) 25 Hz modes.

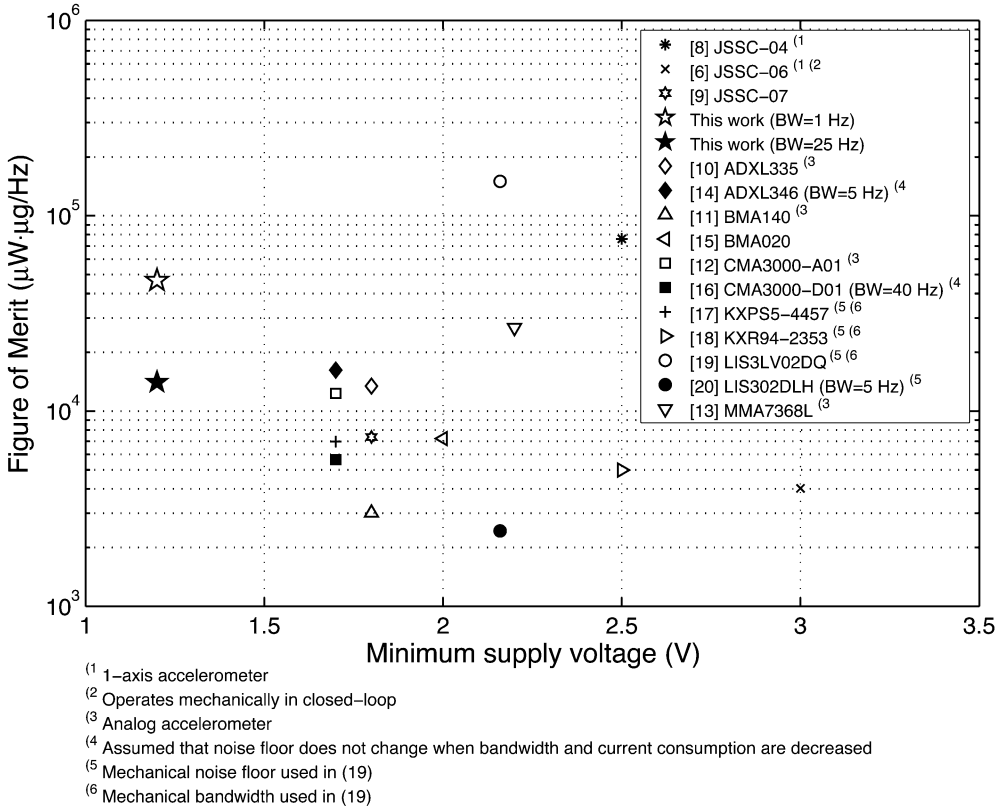

Fig. 15. Performance comparison with other recently published or commercially available, low-g, low-power accelerometers. Typical FOMs are plotted as a function of the minimum reported supply voltages.

1.2 V, while all the other building blocks, including the decimator, operated from the regulated supplies of 1.0 V. It was observed that, although the functionality of the decimator cannot be guaranteed below 1.8 V over process and temperature variations, the whole interface IC under test worked correctly at those conditions in both the 1 and 25 Hz modes. As a result, from

TABLE III
SUMMARY OF MEASURED PERFORMANCE

Process	0.25-μm CMOS with MIM capacitors and high-resistivity polysilicon resistors		
Supply	$1.2 - 2.75\,V$ Two $1.0\,V$ and one $1.0 - 1.8\,V$ regulated on chip		
Configuration	With CS and CDS Without signal boosting and offset compensation		
Active area	$1.73\,mm^2$		
Mode	**1 Hz**	**25 Hz**	
f_s per mass	4.096	51.2	kHz
Current consumption			
Vdd1[a]	14.5	84.3	μA
Vdd2[b]	3.5	5.2	μA
Vdd3[c]	3.2	8.1	μA
Total	21.2	97.6	μA
Noise floor at the output of the front-end / decimator			
x-axis	1080 / 1080	340 / 360	$\mu g/\sqrt{Hz}$
y-axis	1165 / 1100	325 / 320	$\mu g/\sqrt{Hz}$
z-axis	930 / 930	275 / 275	$\mu g/\sqrt{Hz}$
Long-term bias stalibity			
x-axis	475	450	μg
y-axis	470	380	μg
z-axis	490	260	μg
Worst-case nonlinearity at ± 4-g range			
x-axis	$+0.30/-0.35$	$+0.30/-0.35$	%
y-axis	$+0.30/-0.45$	$+0.30/-0.45$	%
z-axis	$+0.30/-0.30$	$+0.20/-0.40$	%

[a] LDO1, V/IREF, REFBUFs, and $\Delta\Sigma$ sensor front-end
[b] LDO2, FREF, and CLKG
[c] LDO3 and decimator

the aforementioned supply voltage reduction, the noise performance degraded by roughly 1 dB.

F. Performance Comparison

Fig. 15 shows the performance comparison with other recently published or commercially available, low-g, low-power accelerometers [6], [8]–[20]. Unless otherwise mentioned in the figure, the devices are 3-axis accelerometers with digital output and operate mechanically in open-loop configuration. All the devices are not directly comparable with each other, because the implementations of [6] and [8] use a 1-axis accelerometer, the implementation of [6] is further based on a $\Delta\Sigma$ structure that operates mechanically in closed-loop configuration, and the four products [10]–[13] have analog outputs.

To the best of authors' knowledge, a fundamental Figure of Merit (FOM) used for accelerometers in the past, comparable to the Walden's FOM widely used for A/D converters [34], does not exist. Therefore, a representative FOM was derived based on the most relevant performance parameters: the supply voltage V_{dd}, the current consumption I_{dd}, the noise floor a_n, and the signal bandwidth BW. The FOMs in units of $(\mu\mathrm{W} \cdot \mu g/Hz)$ are calculated with

$$FOM = \frac{V_{dd} I_{dd} a_n \sqrt{BW}}{BW}. \tag{19}$$

For each accelerometer the following parameters are used: the typical supply voltage and current consumption, the maximum noise floor, and the minimum signal bandwidth. The devices [14], [16], [20] have several active modes with different signal bandwidths. The operating modes that were used in the calculations, and which resulted in the best FOMs for these devices, are also clarified in Fig. 15. In the case of this work, the FOMs are calculated by using a supply voltage of 2.0 V, which is close to the average of the supply range, and the current consumptions, the maximum noise floors, and the signal bandwidths reported in Table III. Based on the measurements performed with the minimum supply voltage of 1.2 V, the noise performance can be assumed to remain the same when the supply voltage is lowered from 2.5 V to 2.0 V. The use of the minimum reported supply voltage on the horizontal axis of Fig. 15 was chosen to highlight the low-voltage operation of the presented interface IC, because the ability of the implemented sensor interface to operate from a 1.2 V supply in both operating modes was verified at room temperature, and the robustness of the system could be further improved by tailoring the digital library cells for low-voltage operation. However, it is worth noting that the minimum supply voltages are not used in the FOM calculations. According to Fig. 15, the presented accelerometer achieves competitive FOMs, especially in the 25 Hz mode, when compared with the best commercially available digital 3-axis accelerometers. In addition, the minimum possible supply voltage is significantly smaller than that of the other devices.

V. CONCLUSION

In this paper, a fully-integrated, micropower, $\Delta\Sigma$-based interface IC for a capacitive 3-axis micro-accelerometer was presented. The IC was implemented in a 0.25-μm CMOS process. The system functionality measurements proved a good noise performance, and excellent current consumption and linearity. The presented performance comparison supports the conclusion that by using the chosen circuit techniques, a competitive, low-voltage, low-power, high-performance sensor interface can be implemented. The overall performance and silicon area could be further optimized by using direct wire bonding between the interface IC and the sensor, by avoiding the use of the third LDO by using a tailored digital standard cell library working down to 0.9 V, and by individually optimizing both remaining LDOs.

ACKNOWLEDGMENT

The authors wish to thank VTI Technologies for providing the sensor elements. From our colleagues at Electronic Circuit Design Laboratory, Mr. Lasse Aaltonen is acknowledged for many valuable discussions and advice during the course of the project. Additionally, Mr. Mika Pulkkinen is acknowledged for his assistance and contribution in automating the rate table measurements.

REFERENCES

[1] P. Salomon, "Micro sensors—World wide markets and economic impact," in *Proc. Eurosensors*, Göteborg, Sweden, Sep. 2006.

[2] M. Paavola, M. Kämäräinen, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen, and K. Halonen, "A 21.2 μA $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Fukuoka, Japan, Nov. 2008, pp. 101–104.

[3] W. Henrion, L. DiSanza, M. Ip, S. Terry, and H. Jerman, "Wide dynamic range direct digital accelerometer," in *Solid-State Sensor and Actuator Workshop Tech. Dig.*, Hilton Head Island, SC, Jun. 1990, pp. 153–157.

[4] M. Lemkin and B. E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 456–468, Apr. 1999.

[5] J. Chae, H. Kulah, and K. Najafi, "A monolithic three-axis micro-g micromachined silicon capacitive accelerometer," *J. Microelectromech. Syst.*, vol. 14, no. 2, pp. 235–242, Apr. 2005.

[6] B. V. Amini, R. Abdolvand, and F. Ayazi, "A 4.5-mW closed-loop $\Delta\Sigma$ micro-gravity CMOS SOI accelerometer," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2983–2991, Dec. 2006.

[7] J. Wu, G. K. Fedder, and L. R. Carley, "A low-noise low-offset capacitive sensing amplifier for a 50-$\mu g/\sqrt{Hz}$ monolithic CMOS MEMS accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 722–730, May 2004.

[8] B. V. Amini and F. Ayazi, "A 2.5-V 14-bit $\Sigma\Delta$ CMOS SOI capacitive accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2467–2476, Dec. 2004.

[9] M. Paavola, M. Kämäräinen, J. Järvinen, M. Saukoski, M. Laiho, and K. Halonen, "A micropower interface ASIC for a capacitive 3-axis micro-accelerometer," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2651–2665, Dec. 2007.

[10] ADXL335: Small, Low Power, 3-Axis $\pm$3 g Accelerometer, Datasheet, Analog Devices, Norwood, MA, 2008.

[11] BMA140: Analog, Triaxal Acceleration Sensor, Datasheet, Bosch, Reutlingen, Germany, 2008.

[12] CMA3000-A01: 3-Axis Low Power Analog Output Accelerometer, Datasheet, VTI Technologies, Vantaa, Finland, 2008.

[13] MMA7368L: $\pm$1.5 g Three Axis Low-g Micromachined Accelerometer, Datasheet, Freescale Semiconductor, Denver, CO, 2008.

[14] ADXL346: Three-Axis, $\pm$2 g/$\pm$4 g/$\pm$8 g/$\pm$16 g Digital Accelerometer, Datasheet, Analog Devices, Norwood, MA, 2009.

[15] BMA020: Digital, Triaxal Acceleration Sensor, Datasheet, Bosch, Reutlingen, Germany, 2008.

[16] CMA3000-D01: 3-Axis Ultra Low Power Accelerometer With Digital SPI and I^2C Interface, Datasheet, VTI Technologies, Vantaa, Finland, 2008.

[17] KXPS5-4457: $\pm$3 g Tri-Axis Accelerometer Specifications, Datasheet, Kionix, Ithaca, NY, 2006.

[18] KXR94-2353: $\pm$2 g Digital Tri-Axis Accelerometer Specifications, Datasheet, Kionix, Ithaca, NY, 2007.

[19] LIS3LV02DQ: 3-Axis $\pm$2 g/ $\pm$6 g Digital Output Low Voltage Linear Accelerometer, Datasheet, STMicroelectronics, Geneva, Switzerland, 2005.

[20] LIS302DLH: MEMS Digital Output Motion Sensor Ultra Low-Power High Performance 3-Axes "Piccolo" Accelerometer, Datasheet, STMicroelectronics, Geneva, Switzerland, 2009.

[21] M. Kämäräinen, M. Paavola, M. Saukoski, E. Laulainen, L. Koskinen, M. Kosunen, and K. Halonen, "A 1.5 μW 1 V 2nd-order $\Delta\Sigma$ sensor front-end with signal boosting and offset compensation for a capacitive 3-axis micro-accelerometer," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2008, pp. 578–579.

[22] E. Laulainen, M. Kosunen, L. Koskinen, M. Paavola, and K. Halonen, "Decimation filter for a low-power sensor-interface system," in *Proc. IEEE Norchip Conf.*, Aalborg, Denmark, Nov. 2007.

[23] M. Paavola, M. Saukoski, M. Laiho, and K. Halonen, "A nanopower double-mode 1-V frequency reference for an ultra-low-power capacitive sensor interface," in *Proc. IEEE Eur. Conf. Circuit Theory and Design*, Sevilla, Spain, Aug. 2007, pp. 104–107.

[24] M. Paavola, M. Kämäräinen, M. Saukoski, and K. Halonen, "A micropower low-dropout regulator with a programmable on-chip load capacitor for a low-power capacitive sensor interface," in *Proc. IEEE Int. Conf. Electronics, Circuits, and Systems*, Malta, Sep. 2008, pp. 450–453.

[25] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 220–224, Feb. 1990.

[26] R. Harjani, R. Heineke, and F. Wang, "An integrated low-voltage class AB CMOS OTA," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 134–142, Feb. 1999.

[27] Y. Cao and G. C. Temes, "High-accuracy circuits for on-chip capacitance ratio testing or sensor readout," *IEEE Trans. Circuits Syst. II*, vol. 41, no. 9, pp. 637–639, Sep. 1994.

[28] E. E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. ASSP-29, no. 2, pp. 155–162, Apr. 1981.

[29] M. Paavola, M. Laiho, M. Saukoski, M. Kämäräinen, and K. Halonen, "Impulse sensitivity function-based phase noise study for low-power source-coupled CMOS multivibrators," *Analog Integr. Circ. Sig. Process.*, 10.1007/s10470-009-9316-8, accepted for publication.

[30] K. N. Leung and P. K. T. Mok, "A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002.

[31] S. K. Lau, P. K. T. Mok, and K. N. Leung, "A low-dropout regulator for SoC with Q-reduction," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 658–664, Mar. 2007.

[32] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.

[33] *Recommended Practice for Inertial Sensor Test Equipment, Instrumentation, Data Acquisition and Analysis*, IEEE Std. 1554, 2005.

[34] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

Matti Paavola (S'06) was born in Kaustinen, Finland, in 1980. He received the M.Sc. and Lic.Sc. degrees in electrical engineering in 2005 and 2007, respectively, from the Helsinki University of Technology (TKK), Espoo, Finland, where he is currently working toward the D.Sc. degree in electrical engineering in the SMARAD-2/Electronic Circuit Design Laboratory.

His research interests include low-voltage low-power analog circuit designs related to sensor interfaces, especially to reference circuits and power management.

Mika Kämäräinen (S'07) was born in Helsinki, Finland, in 1975. He received the M.Sc. and Lic.Sc. degrees in electrical engineering in 2006 and 2007, respectively, from the Helsinki University of Technology (TKK), Espoo, Finland, where he is currently working toward the D.Sc. degree in electrical engineering in the SMARAD-2/Electronic Circuit Design Laboratory.

His research interests include low-voltage low-power analog circuit designs related to sensor front-ends.

Erkka Laulainen (S'08) was born in Jyväskylä, Finland, in 1979. He is currently working toward the M.Sc. degree in electrical engineering in the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology (TKK), Espoo, Finland.

His research interests include low-power digital designs.

Mikko Saukoski (S'06-M'09) was born in Savukoski, Finland, in 1978. He received the M.Sc. and D.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 2004 and 2008, respectively.

From 2003 to 2007, he was a Research Assistant and then a Research Engineer with the SMARAD-2/Electronic Circuit Design Laboratory, TKK. Since 2008, he has been with ELMOS Semiconductor AG, Dortmund, Germany, as a System Design Engineer with ELMOS Microsystems. His research interests include microelectromechanical sensors and actuators, and low-voltage low-power high-accuracy analog circuit design.

Lauri Koskinen (M'03) was born in Helsinki, Finland, in 1972. He received the M.Sc. and D.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 1999 and 2005, respectively.

Since 1998, he has been with the SMARAD-2/Electronic Circuit Design Laboratory, Department of Micro and Nano Sciences, TKK. He received the Academy of Finland Postdoctoral Researcher position in 2008. His research interests include ultra-low-power silicon VLSI implementations, especially sub-threshold operation and mixed-mode parallel processor arrays.

Marko Kosunen (S'97-M'07) was born in Helsinki, Finland, in 1974. He received the M.Sc., Lic.Sc. and D.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 1998, 2001, and 2006, respectively.

He is currently working as a Postdoctoral Researcher with the SMARAD-2/Electronic Circuit Design Laboratory, Department of Micro and Nano Sciences, TKK. His expertise is in implementation of DSP algorithms for wireless transceivers, and current steering D/A converters.

Kari A. I. Halonen (M'02) received the M.Sc. degree in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 1982, and the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1987.

Since 1988, he has been with the SMARAD-2/Electronic Circuit Design Laboratory, TKK. From 1993 to 1997, he was an Associate Professor and, since 1997, a Full Professor with the Faculty of Electrical Engineering and Telecommunications. He became the Head of the Electronic Circuit Design Laboratory in 1998. He specializes in CMOS and BiCMOS analog integrated circuits, particularly for telecommunication applications. He is the author or co-author of more than 200 international and national conference proceedings and journal publications on analog integrated circuits.

Prof. Halonen is a member of Technical Program Committee (TPC) of the European Solid-State Circuits Conference (ESSCIRC) and International Solid-State Circuits Conference (ISSCC). He was the TPC Chairman of ESSCIRC 2000. He has been an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I and a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He received the Beatrice Winner Award at the ISSCC'2002.