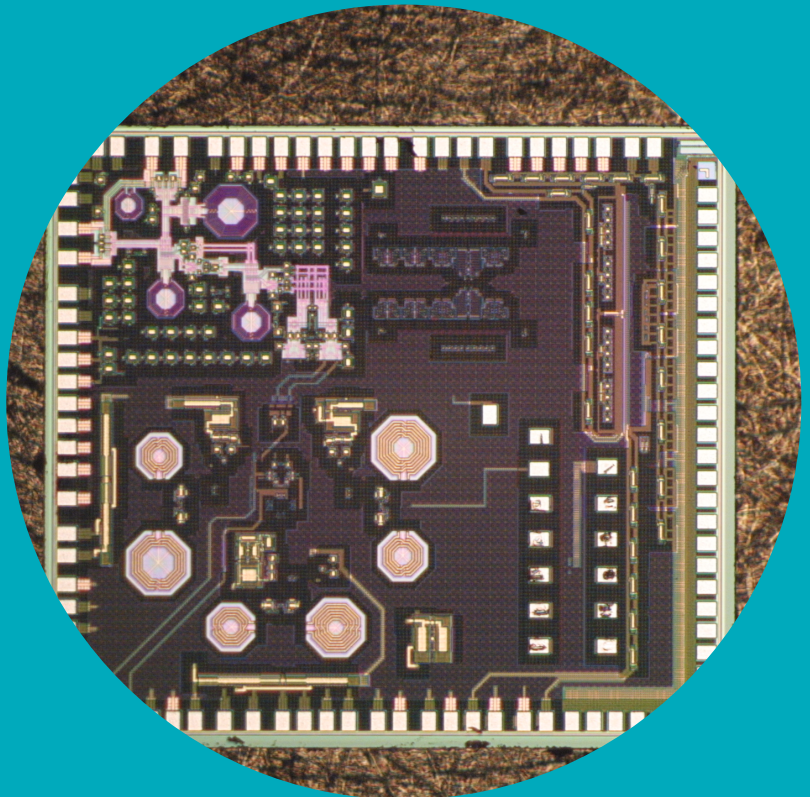


Department of Micro- and Nanosciences

# Continuous-time low-pass filters for integrated wideband radio receivers

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Ville Saari





Aalto University publication series  
**DOCTORAL DISSERTATIONS** 23/2011

# Continuous-time low-pass filters for integrated wideband radio receivers

**Ville Saari**

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This thesis concentrates on the design and implementation of analog baseband continuous-time low-pass filters for integrated wideband radio receivers. A total of five experimental analog baseband low-pass filter circuits were designed and implemented as a part of five single-chip radio receivers in this work.

After the motivation for the research work presented in this thesis has been introduced, an overview of analog baseband filters in radio receivers is given first. In addition, a review of the three receiver architectures and the three wireless applications that are adopted in the experimental work of this thesis is presented. The relationship between the integrator non-idealities and integrator Q-factor, as well as the effect of the integrator Q-factor on the filter frequency response, are thoroughly studied on the basis of a literature review. The theoretical study that is provided is essential for the gm-C filter synthesis with non-ideal lossy integrators that is presented after the introduction of different techniques to realize integrator-based continuous-time low-pass filters. The filter design approach proposed for gm-C filters is original work and one of the main points in this thesis, in addition to the experimental IC implementations.

Two evolution versions of fourth-order 10-MHz opamp-RC low-pass filters designed and implemented for two multicarrier WCDMA base-station receivers in a 0.25- $\mu$ m SiGe BiCMOS technology are presented, along with the experimental results of both the low-pass filters and the corresponding radio receivers. The circuit techniques that were used in the three gm-C filter implementations of this work are described and a common-mode induced even-order distortion in a pseudo-differential filter is analyzed. Two evolution versions of fifth-order 240-MHz gm-C low-pass filters that were designed and implemented for two single-chip WiMedia UWB direct-conversion receivers in a standard 0.13- $\mu$ m and 65-nm CMOS technology, respectively, are presented, along with the experimental results of both the low-pass filters and the second receiver version. The second UWB filter design was also embedded with an ADC into the baseband of a 60-GHz 65-nm CMOS radio receiver. In addition, a third-order 1-GHz gm-C low-pass filter was designed, rather as a test structure, for the same receiver. The experimental results of the receiver and the third gm-C filter implementation are presented.

**Keywords** Analog integrated circuits, CMOS, continuous-time filters, radio receivers**ISBN (printed)** 978-952-60-4066-0**ISBN (pdf)** 978-952-60-4067-7**ISSN-L** 1799-4934**ISSN (printed)** 1799-4934**ISSN (pdf)** 1799-4942**Pages** 230 **Location of publisher** Espoo **Location of printing** Helsinki **Year** 2011**The dissertation can be read at** <http://lib.tkk.fi/Diss/>



**Tekijä**

Ville Saari

**Väitöskirjan nimi**

Jatkuva-aikaisten alipäästösuodattimien toteutus integroituihin laajakaistaisiin radiovastaanottimiin

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Tässä väitöskirjassa on tutkittu analogisten kantataajuisten jatkuva-aikaisten alipäästösuodattimien toteutusta integroituihin laajakaistaisiin radiovastaanottimiin. Työssä on suunniteltu ja toteutettu yhteensä viisi analogista kantataajuista alipäästösuodatinpiiriä viiteen yhdelle puolijohdepalalle integroituihin radiovastaanottimeen.

Väitöskirjan alussa esitetään tutkimustyön taustoja, jonka jälkeen luodaan yleiskatsaus analogisiin kantataajuussuodattimiin osana radiovastaanotinta. Lisäksi tarkastellaan niitä kolmea vastaanotinarkkitehtuuria ja langatonta sovellusta, joihin työssä esitetyt suodatinpiirit alunperin suunniteltiin. Tämän jälkeen tarkastellaan integraattorin epäideaalisuuksien ja Q-arvon välistä yhteyttä sekä integraattorin Q-arvon vaikutusta suodattimen taajuusvasteeseen kirjallisuustutkimuksen pohjalta. Integraattorin Q-arvon merkityksen ymmärtäminen on välttämätöntä, kun työssä esitetään, kuinka gm-C -suodatinsovellus toteuttaa epäideaalisilla häviöllisillä integraattoreilla. Sitä ennen kuitenkin esitellään erilaisia piiritekniikoita toteuttavaa integraattoreihin perustuvia jatkuva-aikaisia alipäästösuodattimia. Tässä työssä esitetty gm-C -suodattimien suunnittelumenetelmä on yksi tämän väitöskirjan pääkohtia toteutettujen suodatinpiirien lisäksi.

Tässä väitöskirjassa on esitetty kahden neljäasteisen 10 MHz:n opamp-RC -suodattimen suunnittelu ja toteutus mittaustuloksineen kahteen WCDMA-järjestelmän monikantoaaltotukiasemavastaanottimeen 0,25  $\mu\text{m}$ :n SiGe BiCMOS -teknologialla. Lisäksi työssä esitetään niitä piiritekniikoita, joita kolmessa työssä toteutetussa gm-C -suodattimessa on käytetty. Työssä on analysoitu yhteisluotoisen häiriösignaalin pseudo-differentiaalisessa suodatinpiirissä aiheuttamaa toisen kertaluvun säröä. Kaksi viisiasteista 240 MHz:n gm-C -alipäästösuodatinpiiriä, jotka tässä työssä suunniteltiin ja toteutettiin kahteen WiMedia UWB -suoramuunnosvastaanottimeen 0,13  $\mu\text{m}$ :n ja 65 nm:n CMOS -teknologioilla, on esitetty. Kummankin suodattimen sekä jälkimmäisen vastaanottimen mittaustulokset on esitetty. Toinen UWB-suodatin integroitiin AD-muuntimen kanssa myös osaksi 65 nm:n CMOS:lla toteutettua 60 GHz:n radiovastaanotinta. Samaan vastaanottimeen suunniteltiin testirakenteena 1 GHz:n gm-C -alipäästösuodatin. Sekä 60 GHz:n vastaanottimen että kolmannen gm-C -suodatinpiirin mittaustulokset on esitetty.

**Avainsanat** Analogiset integroidut piirit, CMOS, jatkuva-aikaiset suodattimet, radio vastaanottimet**ISBN (painettu)** 978-952-60-4066-0**ISBN (pdf)** 978-952-60-4067-7**ISSN-L** 1799-4934**ISSN (painettu)** 1799-4934**ISSN (pdf)** 1799-4942**Sivumäärä** 230**Julkaisupaikka** Espoo**Painopaikka** Helsinki**Vuosi** 2011**Luettavissa verkossa osoitteessa** <http://lib.tkk.fi/Diss/>





# Preface

The work for this thesis was carried out in the Electronic Circuit Design Laboratory of Helsinki University of Technology between 2004 and 2009 and in the Department of Micro- and Nanosciences at the Aalto University School of Science and Technology in 2010. The work presented in this thesis is part of research projects funded in part by Nokia Networks, the Nokia Research Center, the Finnish Funding Agency for Technology and Innovations (TEKES), and the Centre of Excellence program (SMARAD2). During the years 2007–2008, I was privileged to be a postgraduate student of the Graduate School in Electronics, Telecommunications, and Automation (GETA), which partially funded my studies. In addition to the TKK Graduate School of Electrical and Communications Engineering, I would also like to acknowledge the HPY Research Foundation, Finnish Foundation for Technology Promotion (TES), Finnish Society of Electronics Engineers (EIS), Nokia Foundation, Walter Ahlström Foundation, and Ulla Tuominen Foundation for awarding scholarships for my postgraduate studies.

I would like to thank my supervisor Prof. Jussi Rynnänen for his encouragement and guidance throughout my career as a Research Engineer at the laboratory since 2001. I would also like to thank Prof. Kari Halonen for giving me the opportunity to work with interesting research topics at the lab for so many years. I am grateful to D.Sc. Jarkko Jussila for his guidance at the beginning of my research work in the area of analog baseband circuit design in 2004. During the years 2005–2008, I had the honor of doing research work with an exceptionally intelligent and innovative person, Prof. Saska Lindfors. I wish to express my gratitude to him for instructing me on the topic of this thesis with a professional, but, at the same time, rousing manner. I also wish to warmly thank Assoc. Prof. Andrea Baschiroto and D.Sc. Kimmo Koli for reviewing this thesis and for their comments and suggestions.

I want to express my gratitude to all my present and former colleagues at the laboratory for creating a pleasant working atmosphere. I am grateful to all the team members with whom I had the opportunity to work in the

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My warmest thanks go to my parents, Tuula and Pertti, for the support and encouragement they have given me throughout my life. I am also grateful to my parents-in-law, Mirja and Tauno, for the great times we have had together. Finally, my beloved wife, Sanna, deserves my dearest thanks for the love and support she has given me.

Espoo, February 2011

Ville Saari

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# List of Abbreviations

AC	Alternating current
ADC	Analog-to-digital converter
APPF	Active polyphase filter
BB	Baseband
BER	Bit error rate
BG	Band group
BG1	Band group #1 (related to the WiMedia UWB system)
BG3	Band group #3 (related to the WiMedia UWB system)
BiCMOS	Bipolar complementary metal oxide semiconductor
BS	Base-station
BUF	Buffer amplifier
CM	Common mode
CMFB	Common-mode feedback
CMFF	Common-mode feedforward
CMOS	Complementary metal oxide semiconductor
CMRR	Common-mode rejection ratio
CP	Charge pump
DAC	Digital-to-analog converter
DBF	Dual bias feed (LNA linearization technique)
DC	Direct current
DCR	Direct-conversion receiver
DIV <sub>2</sub>	Divide by two
DS-CDMA	Direct-sequence code division multiple access
DS-UWB	Direct-sequence ultra wideband (impulse radio technique)
ETSI	European Telecommunications Standard Institute
FCC	Federal Communications Commission
FDD	Frequency division duplex
GBW	Gain bandwidth product
GIC	General impedance converter
GMSK	Gaussian minimum shift keying
GND	Ground
GSM	Global System for Mobile Communications
HD	High density

HD <sub>2</sub>	Second-order harmonic distortion
HD <sub>3</sub>	Third-order harmonic distortion
HG	High gain
HSPA	High Speed Packet Access
HSPA+	Enhanced High Speed Packet Access
IC	Integrated circuit
ICP	Input –1-dB compression point
IDAC	Current-steering digital-to-analog converter
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate frequency
IIP <sub>2</sub>	Second-order input intercept point
IIP <sub>3</sub>	Third-order input intercept point
IMT-2000	International Mobile Telecommunications-2000
IS-95	Interim Standard 95
ISO	International Organization for Standardization
ITU	International Telecommunication Union
LC	Inductor-capacitor
LG	Low gain
LNA	Low-noise amplifier
LO	Local oscillator
LPF	Low-pass filter
LSB	Least significant bit
LTE	Long Term Evolution
MB-OFDM	Multiband orthogonal frequency division multiplexing
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MS	Mobile station
MSB	Most significant bit
MUX	Multiplexer
NF	Noise figure
NMOS	N-channel metal oxide semiconductor
OFDM	Orthogonal frequency division multiplexing
opamp	Operational amplifier
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PD	Phase detector
PDC	Personal Digital Cellular
PGA	Programmable gain amplifier
PMOS	P-channel metal oxide semiconductor



PVT	Process, voltage, and temperature
RC	Resistor-capacitor
RF	Radio frequency
SC	Switched capacitor
SDR	Signal-to-distortion ratio
SFDR	Spurious-free dynamic range
SFG	Signal flow graph
SIG	Special Interest Group
SiGe	Silicon-germanium
SNR	Signal-to-noise ratio
TDD	Time division duplex
THD	Total harmonic distortion
TRIM	Trimming
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
UTRA	Universal Terrestrial Radio Access, UMTS Terrestrial Radio Access
UWB	Ultra wideband
VCCS	Voltage-controlled current source
VCO	Voltage-controlled oscillator
VGA	Variable gain amplifier
V-I	Voltage-current
VSVS	Voltage-controlled voltage source
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WLAN	Wireless local area network
WPAN	Wireless personal area network
2G	Second generation
3G	Third generation
4G	Fourth generation
3GPP	Third Generation Partnership Project

# List of Symbols

$A$	Amplitude of the signal, amplifier
$A_{BB}$	Amplitude of the baseband signal
$A_{CM}$	Common-mode voltage gain, amplitude of the common-mode signal
Active-gm-RC	Filter technique that uses operational amplifiers, transconductances, resistors, and capacitors
$A_{DC}$	DC gain
$A_{DC,opamp}$	Open-loop DC gain of the operational amplifier
$a_i$	Polynomial coefficients
$A_{IF}$	Amplitude of the IF signal
$a_n$	Voltage gain from the input of the $n$ th stage to the circuit output
$A_{opamp}(s)$	Frequency dependent open-loop gain of the operational amplifier
$A_{RF}$	Amplitude of the RF signal
$A_{V,RF}$	Voltage gain of the RF front-end
$A_{V,RX}$	Voltage gain of the receiver
$A_{VTH}$	Process-related constant
$A_{V,transconductor}$	Voltage gain of the transconductor
$A_{\beta}$	Process-related constant
$B$	Amplitude of the signal
$B_n$	Bit, $n = 1, 2, 3, \dots$
$BBoutI$	Baseband output I-branch
$BBoutQ$	Baseband output Q-branch
$B_{BB}$	Equivalent baseband noise bandwidth
$b_j$	Polynomial coefficients, $j = 1, 2, 3, \dots$
$b_j'$	Polynomial coefficients, $j = 1, 2, 3, \dots$
$B_{RF}$	Equivalent RF noise bandwidth of the channel
$BW$	Channel bandwidth
$C_0$	Fixed capacitor of the capacitor matrix
$C_{0,metal}$	Fixed capacitor of the capacitor matrix consisting of a metal-metal capacitor
$Chn$	Channel, $n = 1, 2, 3, \dots$
$C_k$	Capacitor, capacitance, $k = 1, 2, 3, \dots$
$C_{k,off}$	Capacitance of the $k$ th switched capacitor when the capacitor is switched off, $k = 1, 2, 3, \dots$

$C_L$	Load capacitor, load capacitance
$C_{Mn}$	Miller capacitor, Miller capacitance, $n = 1, 2, 3...$
$C_n$	Capacitor, capacitance, $n = 1, 2, 3...$
$C_{nom}$	Nominal capacitance value
$C_{SW}$	Switched extra capacitor
$C_{Swn,k}$	Parasitic capacitance of the $n$ th switch, $n = 1, 2, 3..., k = 1, 2, 3...$
Ctrl	Control
$C_x$	Unit capacitor, unit capacitance
$C_{zero}$	Capacitor realizing a transmission zero
$CZ_n$	Capacitor realizing a transmission zero, $n = 1, 2, 3...$
$D(s)$	Polynomial in the denominator
$D_{out, imd3}$	Amplitude of the third-order intermodulation distortion term at the circuit output
$f_{-3dB}$	-3-dB frequency
$f_c$	Passband edge frequency
$G_{Cn}$	Shunt conductance of the $n$ th capacitor, $n = 1, 2, 3...$
$G_{complex}$	Gain coefficient
$g_{dsn,m}$	Drain-source conductance of the transistors $M_n$ and $M_m$
$G_L$	Load conductor, load conductance
$G_{lossy}$	Gain coefficient
$gm$	Transconductance
$gm_{1,mod}$	Modulated transconductance
$gm_{1,orig}$	Original transconductance value
Gm-C	Filter technique that uses transconductors and capacitors
$gm_{mixer}$	Transconductance of the mixer
$gm_n$	Transconductance, $n = 1, 2, 3...$
$Gm_n$	Transconductor, $n = 1, 2, 3...$
$gm_{nM}$	Transconductance (negative branch), $n = 1, 2, 3...$
$gm_{nP}$	Transconductance (positive branch), $n = 1, 2, 3...$
Gm-OTA-C	Filter technique that uses transconductors, operational transconductance amplifiers, and capacitors
$G_n$	Power gain (expressed as absolute values, not in decibels) of the $n$ th receiver block, conductor, conductance, $n = 1, 2, 3...$
$G_{neg}$	Negative conductance
$g_{out}$	Output conductance

$g_o$	Output conductance
$G_{RC}(\omega)$	Gain (i.e. attenuation) of the RC pole
$G_{real}$	Gain coefficient
$H(f)$	Frequency response of the circuit
$H(j\omega)$	Transfer function of a filter
$H_{int}(s)$	Transfer function of an integrator
$H_{lossy}(s)$	Transfer function of the lossy filter
I	In-phase
$I_{Bn}$	Bias current, $n = 1, 2, 3\dots$
$I_{BOOST}$	Boost current
$I_D$	Drain current
$I_{DBF}$	Dual-bias-feed current
$I_{DC}$	DC current
$I_{dd}$	DC current, current consumption
$I_{error}$	Error current
$I_{ERROR}$	Error current
$iip2$	Second-order input intercept point (expressed in watts, not in $dBm$ values)
$iip3_n$	Third-order input intercept point (expressed in watts, not in $dBm$ values) , $n = 1, 2, 3\dots$
$I_{in}$	Input current
$imd2$	Second-order intermodulation distortion component
$imd2_{CM-to-differential}$	Second-order intermodulation distortion component as a result of the common-mode signal leakage back to the differential path
$imd2_{two-tone}$	Second-order intermodulation distortion component as a result of the two-tone test
$I_n$	Current of the $n$ th branch of the network, $n = 1, 2, 3\dots$
$inm, INM$	Circuit input (negative branch)
$INN$	Circuit input (negative branch)
$inp, INP$	Circuit input (positive branch)
$I_{out}$	Output current
$i_{OUT}(t)$	Output current
$i_{OUTM}(t)$	Output current (negative branch)
$i_{OUTP}(t)$	Output current (positive branch)
$I_{REF}$	Reference current
$k$	Boltzmann's constant $\approx 1.3807 \cdot 10^{-23}$ J/K
$k_1$	Linear gain
$k_3$	Non-linear coefficient

$k_1'$	Linear gain
$k_3'$	Non-linear coefficient
$K_i$	Coefficient, $i = 1, 2, 3...$
$k_L$	Scaling factor
$K_m$	Coefficient, $m = 1, 2, 3...$
$k_n$	Scaling factor, $n = 1, 2, 3...$
$k_S$	Scaling factor
$L$	Channel length of a MOSFET
$L_n$	Inductor, inductance, $n = 1, 2, 3...$
LO <sub>M</sub>	Local oscillator signal (negative branch)
LO <sub>P</sub>	Local oscillator signal (positive branch)
$M(\omega)$	Magnitude response
$M_L$	Load MOSFET
$M_n$	MOSFET, $n = 1, 2, 3...$
$M_{nn}$	MOSFET (negative branch), $n = 1, 2, 3...$
$Mn_n$	N-channel MOSFET, $n = 1, 2, 3...$
$Mnp$	MOSFET (positive branch), $n = 1, 2, 3...$
MOSFET-C	Filter technique that uses MOSFETs, capacitors, and amplifiers
$MP_n$	P-channel MOSFET, $n = 1, 2, 3...$
$N$	Degree of the denominator, division count
$N(s)$	Polynomial in the numerator
$NF_{LNA}$	Noise figure of the low-noise amplifier
$NF_{Low-IF}$	Low-IF noise figure
$NF_{RF}$	Noise figure of the RF front-end
$NF_{RX}$	Overall noise figure of the receiver
Opamp-RC	Filter technique that uses operational amplifiers, resistors, and capacitors
$Outm, OUTM$	Circuit output (negative branch)
$OUTN$	Circuit output (negative branch)
$Outp, OUTP$	Circuit output (positive branch)
$P_{FUND}$	Power of the fundamental signal
$P_{FUND,IN}$	Power of the fundamental signal at the circuit input
$p_i$	Pole, $i = 1, 2, 3...$
$P_{IMDn}$	Power of an input-referred $n$ th-order intermodulation component
$P_{IMD2,IN}$	Power of the input-referred second-order intermodulation product
$P_{IMD3,IN}$	Power of the input-referred third-order intermodulation product

$P_{IMD3,OUT}$	Power of the third-order intermodulation product at the circuit output
$P_{IN}$	Power of the fundamental input signal component
$P_{in,min}$	Sensitivity
$P_{IN,\omega n}$	Power of the $n$ th interferer at the circuit input, $n = 1, 2, 3...$
$P_{NOISE,IN}$	Input-referred in-channel noise power
$P_{OUT}$	Power of the of the fundamental signal component
$Q$	Quadrature phase, quality factor, bipolar transistor
$Q_n$	Bipolar transistor, $n = 1, 2, 3...$
$Q_C$	Capacitor quality factor
$Q_{cap,n}(\omega)$	Quality factor of the $n$ th capacitor, $n = 1, 2, 3...$
$Q_{int}(\omega)$	Integrator quality factor
$Q_L$	Inductor quality factor
$Q_{n,eff}$	Effective quality factor of the $n$ th filter stage, $n = 1, 2, 3...$
$Q_{pole}$	Pole quality factor
$RF_{HG}$	Radio frequency high-gain-mode input of the circuit
$RF_{IN}$	Radio frequency input of the circuit
$RF_{LG}$	Radio frequency low-gain-mode input of the circuit
$R_{if}$	Input resistance of the shunt-series feedback amplifier
$R_{in}$	Input resistance
$R_L$	Load resistor, load resistance
$R_n$	Resistor, resistance, $n = 1, 2, 3...$
$R_n'$	Resistor, resistance, $n = 1, 2, 3...$
$r_{out}$	Output resistance
$r_{out}'$	Output resistance
$R_S$	Source resistor, source resistance
$S_I$	Switch
$S_{11}(s)$	Reflection coefficient at the input port
$S_{21}(s)$	Transfer function
$SDR_i$	Signal-to-distortion ratio at the baseband output in case of the current-mode baseband input
$SDR_v$	Signal-to-distortion ratio at the baseband output in case of the voltage-mode baseband input
$SNR_{min}$	Minimum signal-to-noise ratio required for successful detection
$S_{out,in-band}$	In-band signal amplitude at the circuit output
$Sw_n$	Switch, $n = 1, 2, 3...$

$V_{BIAS}$	Bias voltage
$V_{bn}$	Bias voltage, $n = 1, 2, 3...$
$V_c$	Control voltage
$V_{CM}$	Common-mode voltage
$V_{CM,IN}$	Common-mode input signal
$V_{CM,IN,PMOS}$	Common-mode input signal at the gate of the PMOS transistor
$V_{CONTROL}$	Control voltage
$V_{CONTROLn}$	Control voltage, $n = 1, 2, 3...$
$V_{DD}$	Positive supply voltage
$V_{error}$	Error voltage
$V_{ERROR}$	Error voltage
$V_{GS}$	Gate-source voltage of a MOSFET
$\hat{v}_{iip2}$	Amplitude value of the second-order input intercept point
$v_{imd2,in}(t)$	Voltage value of the $imd2$ term referred to the circuit input
$V_{in}$	Input voltage
$v_{in}(t)$	Input voltage
$v_{IN}(t)$	Input voltage
$V_{in,CM}$	Common-mode input voltage
$v_{INM}(t)$	Input voltage (negative branch)
$V_{inn}$	Input voltage (negative branch)
$V_{inp}$	Input voltage (positive branch)
$v_{INP}(t)$	Input voltage (positive branch)
$V_n$	Voltage of the $n$ th node of the network, $n = 1, 2, 3...$
$V_{out}$	Output voltage
$V_{out,CM}$	Common-mode output voltage
$V_{outn}$	Output voltage (negative branch)
$V_{out,noLNA}$	Total integrated output noise when the LNA is biased off
$V_{out,nom}$	Total integrated output noise when the LNA is biased on
$V_{outp}$	Output voltage (positive branch)
$V_{REF}$	Reference signal
$V_{SS}$	Negative supply voltage
$V_{TH}$	Threshold voltage of a MOSFET
$W_n$	Channel width of a MOSFET, $n = 1, 2, 3...$
$XB_n$	Inverted $n$ th bit, $n = 1, 2, 3...$
$x_n$	Polynomial coefficients, $n = 1, 2, 3...$

$z_i$	Transmission zero, $i = 1, 2, 3...$
$Z_{11}(s)$	Input impedance
$Z_L(\omega)$	Load impedance
$v_{IMD2}(t)$	Second-order intermodulation term
$v_{IMD3}(t)$	Third-order intermodulation term
$v_{in}(t)$	Input voltage
$\overline{v_{n,in,BB}}$	Input-referred integrated noise voltage of the analog baseband circuit
$v_{out}(t)$	Output voltage
$\alpha$	Ratio of the error current and the drain current
$\alpha_0$	DC offset
$\alpha_1$	Linear gain
$\alpha_2, \alpha_3$	Non-linear coefficients
$\alpha_2', \alpha_3'$	Relative non-linear coefficients
$\alpha_2'', \alpha_3''$	Relative non-linear coefficients
$\beta$	Feedback factor, current factor
$\beta A_{opamp}(s)$	Frequency dependent loop gain of the feedback connected operational amplifier
$\phi$	Phase
$\overline{\phi}$	Inverse phase
$\phi_{int}(\omega)$	Integrator phase
$\eta_{nom}$	Nominal LO duty-cycle factor
$\theta(\omega)$	Phase responses
$\rho_{in}$	Reflection coefficient at the input port
$\rho_{out}$	Reflection coefficient at the output port
$\sigma$	Standard deviation
$\sigma^2$	Variance
$\tau(\omega)$	Group delay function
$\tau_{int}$	Time constant of the integrator
$\omega$	Angular frequency
$\omega_{BB}$	Frequency of the desired in-band signal at the baseband (expressed as an angular frequency)
$\omega_c$	Passband edge frequency (expressed as an angular frequency)
$\omega_{GBW}$	Unity-gain frequency of the operational amplifier
$\omega_{IFn}$	Frequency of the IF signal (expressed as an angular frequency)
$\omega_{md2}$	Low-frequency beat
$\omega_{int}$	Integrator unity-gain frequency



$\omega_{p1}$	Low-frequency dominant pole
$\omega_{p1,opamp}$	Low-frequency dominant pole of the operational amplifier
$\omega_{p2}$	High-frequency non-dominant pole
$\omega_{zero}$	Transmission zero frequency
$\Delta gm$	Transconductance value deviation
$\Delta gm_{tot}$	Deviation of the total transconductance value
$\Delta M(\omega)$	Magnitude error
$\Delta R$	Resistance deviation
$\Delta V_{TH}$	Threshold voltage deviation
$\Delta \eta$	Deviation of the LO duty-cycle factor
$\Delta \beta$	Current factor deviation
$\Delta \phi_{in}(\omega)$	Deviation of the integrator phase from its ideal value



# 1 Introduction

## 1.1 Motivation for the thesis

During the past decade, new wireless technologies have continued to arouse enormous research interest both in industry and in academia. Technological evolution has simultaneously continued to be rapid. At the moment, there exist a host of new wireless applications that have emerged on the consumer market or are currently under development. As a consequence, wireless access to the Internet is part of our everyday life and the third-generation cellular systems, such as WCDMA, provide broadband multimedia services (up to tens of Mbps) to mobile users. Despite the notable progress achieved by far, one of the current trends is to strive for ever-higher data rates, even with reduced operating ranges. Two examples of such a development trend are the WiMedia UWB and 60-GHz radio technologies. The former targets throughputs of up to 480 Mbps and the latter of over 1 Gbps over short distances. Both technologies are thus suitable candidates for future high-speed wireless personal area network (WPAN) applications and the latter may also be used in wireless local area network (WLAN) applications.

From an integrated circuit (IC) designer's point of view, a high data rate typically implies wideband radio transceiver building blocks. This is often the case although the transfer capacity of a system could also be increased by using spectral efficient modulation schemes. In wireless systems, the performance of the radio receiver has a significant role in determining whether the transferred information can be successfully detected from the radio channel. Signal amplification and filtering are two signal-processing operations that are often used in radio receivers to support the most important function of a receiver, signal demodulation. These two supportive operations are typically distributed between different receiver blocks. This thesis concentrates on the design and implementation of analog baseband continuous-time low-pass filters for wideband single-chip radio receivers. The filters are designed to have voltage gain in order to

accomplish both of the aforementioned signal-processing operations with a single circuit at the analog baseband.

Because of the co-existence of a wide variety of cellular and ad hoc networks, a lot of research effort has recently been invested in developing digitally-assisted circuit solutions, such as software-defined radio and cognitive radio [1]-[6]. These types of radios are intended to be able to flexibly select the transmitted and received radio frequency, channel bandwidth, and modulation scheme according to the desired radio standard with a single IC. Hence, they are potential candidates when looking for cost- and power-efficient solutions for future mobile terminals. Similarly, in base-station applications, a single-system multicarrier transceiver can be digitally adjusted to simultaneously transmit or receive one to multiple channels with a single IC [7], [8]. In these multifunction radio chips, the objective is to place the analog-to-digital interface close to the antenna in order to perform most of the signal processing in the digital domain. However, when implementing wideband transceivers for high-data-rate radio systems, it is often more feasible and less power-consuming, in practice, to employ analog filters and amplifiers instead of replacing them by digital signal processing. The physical world is analog in nature and continuous-time filters are usually deployed in analog-to-digital (and digital-to-analog) interfaces, for instance [9], [10]. In addition to wireless communication systems, continuous-time filters are needed, for example, in hard disk drive read/write channels and video signal processors [11]-[14]. Since continuous-time filters can provide advantages over their digital counterparts, especially in wideband applications, the author strongly believes that analog filters will be used in power-efficient radio ICs in the future as well.

The CMOS technology enables the analog and digital parts of a radio transceiver to be integrated on a single chip, potentially with a small die area. It is currently known to be the foremost technology for low-cost, high-volume production. In this millennium, silicon germanium (SiGe) BiCMOS technologies, dedicated to RF and microwave applications, have been a popular alternative when realizing high-performance single-chip RF transceivers with the yield, manufacturing advantages, and high functionality associated with conventional CMOS implementations [15], [16]. However, because of the recent advances in standard CMOS technologies, it has become feasible to implement not only RF front-ends operating in the crowded radio frequencies below 10 GHz, but also millimeter-wave circuit blocks operating up to 100 GHz (and even beyond) in standard nanoscale (sub-100-nm) CMOS processes [17]-[19]. Single-chip, low-power SiGe BiCMOS and, especially, pure CMOS radio

transceiver implementations are currently of special interest for consumer electronic products.

Modern ultra-deep-submicron CMOS technologies, such as the 0.13- $\mu\text{m}$  and 65-nm ones adopted in this work, are optimized for digital circuitry. Thus, their use poses new challenges for analog IC design, despite the advantages of faster transistors and a higher transistor density. For instance, small feature size demands a low supply voltage (around 1.2 V), the intrinsic gain of the transistor ( $g_m/g_{ds}$ ) is reduced, increased gate leakage currents impose degradation on the device-matching characteristics, and accurate prelayout simulations cannot be performed as a result of the limited tool set currently available to the analog IC designer [20]-[22]. The low nominal supply voltage limits the number of stacked transistors and voltage swing in analog circuits, thereby potentially reducing the achievable dynamic range and increasing power dissipation [21], [23]. The deployment of nanoscale CMOS technologies calls for new circuit solutions in order to overcome the effects of the aforementioned disadvantages.

In wideband wireless applications, it is often desired that the frequency response of a receiver chain is flat for in-band signals. At the same time, the receiver has to be capable of suppressing interfering out-of-band signals and adjacent channels to a sufficiently low level for them not to degrade the bit error rate of the receiver. Especially in direct-conversion and low-IF receivers, selective analog baseband low-pass filtering with a small passband ripple is needed. However, the non-idealities of the integrated active devices forming the filter easily cause the shape of the filter frequency response to deteriorate. The wide bandwidth that is required exacerbates this undesirable effect further. Therefore, the primary goal for the study presented in this thesis was to investigate if integrated wideband continuous-time low-pass filters with an accurate frequency response shape can be implemented in standard ultra-deep-submicron CMOS technologies. In the work, an accurate filter frequency response can be defined as consisting of the exact location of the passband edge frequency, a small passband ripple, and the desired transition band steepness, including the exact location of the stopband transmission zeros. The baseline for the study was to accept (i.e. live with) the non-idealities of the low-voltage, active devices forming the filter but to take their effect into account beforehand in the filter synthesis. As a limitation, the non-idealities that are considered must be quantities that can be measured and controlled in one way or another.

## 1.2 Research contribution and publications

The focus of the research described in this thesis is on the design and implementation of integrator-based continuous-time low-pass filters for wideband radio receivers. This thesis includes a total of five experimental low-pass filter circuits designed or co-designed by the author during the years 2004–2008. All of them are embedded into a single-chip radio receiver IC. The first two experimental circuits are designed for a multicarrier WCDMA base-station receiver in a 0.25- $\mu\text{m}$  SiGe BiCMOS technology. To the best of the author's knowledge, this is the first published single-chip multicarrier WCDMA receiver implementation. The third and fourth circuits are designed for a WiMedia UWB direct-conversion receiver targeted for mobile terminals in standard 0.13- $\mu\text{m}$  and 65-nm CMOS technologies, respectively. The last experimental work consists of two parts. The second UWB filter design was embedded with an ADC into the I-branch of a 60-GHz 65-nm CMOS radio receiver. Instead of a similar analog baseband with a similar ADC also being placed into the Q-branch, an ultra-wideband filter circuit followed by a limiting amplifier chain was designed for it. Thus, the Q-branch of the receiver is rather a test structure. In any case, to the best of the author's knowledge, this is the first published receiver implementation that includes a 60-GHz millimeter-wave front-end, an IF stage, an analog baseband circuit, and an ADC on a single silicon chip. Although the five experimental filter circuits are designed according to the specifications of the targeted radio system and the receiver architecture that was adopted, they can be utilized in other wideband applications as well. The circuit implementations form the main part of the work. They are presented in separate application cases in this thesis, together with the experimental results of both the low-pass filter and the corresponding receiver.

In this thesis, the meaning of the term *wideband* is twofold. In a multicarrier WCDMA receiver capable of receiving up to four adjacent channels simultaneously, the bandwidth of the analog baseband filter becomes four times wider compared to the conventional single-channel reception. In this case, we talk about a 10-MHz bandwidth. On the other hand, in the WiMedia UWB and 60-GHz radio receiver applications, the bandwidth of the filter needs to be well over 200 MHz. In fact, in the fifth experimental circuit, the design goal for the filter bandwidth was set to be as wide as 1 GHz.

In addition to the IC implementations, one of the key points in this thesis is to propose a filter design approach that conveniently combines a loss-mapping technique, a frequency response predistortion, a broadband

transconductor structure, and a transconductor DC gain control. The design method, presented in detail in this thesis, originates from the collaboration of the author, Mikko Kaltiokallio, and Prof. Saska Lindfors. Although some of the techniques used in the proposed approach have previously been published in the literature, their use at the same time makes this design approach original. The third and fourth experimental filter circuits demonstrate the usability of the method in realizing wideband continuous-time filters in modern ultra-deep-submicron CMOS technologies. Moreover, on the basis of the experimental results of the fifth ultra-wideband filter implementation, some conclusions regarding the limitations of the approach are drawn. It is worth emphasizing that at the beginning of the work (i.e. the first two experimental circuits), a rather conventional filter design approach was first used to study the imperfections and challenges related to wideband filter design.

A huge number of analog baseband low-pass filters have been reported in the literature. It is not the purpose of this thesis to review the development of these filters comprehensively. The emphasis is on the recently-published designs and especially, on the work carried out by the author in the field of continuous-time low-pass filters. Hence, this thesis is mainly based on the contents of the previously published international journal and conference articles which are briefly introduced in the following paragraphs. In addition, the contribution of the author to each paper is described in the following discussion.

Paper [24] describes a single-chip multicarrier WCDMA receiver targeted for base-station applications. The IC that was implemented can receive four adjacent WCDMA channels simultaneously. The research team which designed, implemented, and measured the receiver consisted of seven members, including the author. The other members were D.Sc. Jussi Ryyänen, D.Sc. Jarkko Jussila, D.Sc. Lauri Sumanen, Mikko Hotti, Arto Malinen, and Tero Tikka. Prof. Kari Halonen was the leader who was responsible for the project. D.Sc. Jussila and D.Sc. Ryyänen made the system design for the receiver. The author designed and implemented the 10-MHz low-pass filter, together with D.Sc. Jussila. D.Sc. Sumanen contributed to the layout design of the filter capacitor matrices and in addition, he was responsible for designing the ADC buffer. The author participated in the receiver measurements and measured the low-pass filter. D.Sc. Ryyänen, Hotti, and Malinen implemented the RF front-end. Tikka assisted them in the RF front-end measurements.

Paper [25] presents the low-pass filter circuit of the single-chip multicarrier WCDMA receiver of publication [24] with more extensive measurement results. The circuit that is presented is the first

implementation that the author co-designed in the research area of analog baseband filters for integrated radio receivers. The contribution of the author is the same as in paper [24]. As a new design team member, Jussi Mustola assisted the author in the filter measurements.

Paper [27] is a journal article based on papers [24] and [25].

Publication [26] describes the second evolution version of the single-chip multicarrier WCDMA base-station receiver. The research team which designed, implemented, and measured the receiver consisted of five members, including the author. The other members were D.Sc. Jussi Ryyänen, Mikko Hotti, Tero Tikka, and Jussi Mustola. Prof. Kari Halonen was the leader who was responsible for the project. In this circuit, the analog baseband low-pass filter was partially re-designed, for example to have a programmable bandwidth from 2.5 MHz to 10 MHz in 2.5-MHz frequency steps. In addition, the gain of the filter was designed to be programmable. As a consequence of the modifications, the second receiver prototype can be programmed to receive from one to four adjacent WCDMA channels simultaneously. The author was responsible for designing the low-pass filter with the assistance of Mustola. The author participated in the receiver measurements and instructed Mustola in the measurements of the low-pass filter. D.Sc. Ryyänen, Hotti, and Tikka implemented the RF front-end.

Paper [28] presents the low-pass filter circuit of the second single-chip multicarrier WCDMA receiver published in paper [26] with extensive measurement results. The contribution of the author is the same as in paper [26]. Prof. Saska Lindfors participated in the writing of the manuscript.

Paper [32] is a journal article based on paper [28].

Invited paper [34] compares different techniques for the design of highly linear downconversion mixers in SiGe BiCMOS technology. Although the paper concentrates mainly on the mixer design, it also discusses issues related to the implementation of the mixer-baseband interface. The author is responsible for the mixer-baseband discussion, together with D.Sc. Jussila. Tikka and Prof. Ryyänen are responsible for the RF mixer-related issues and discussions in the paper.

Paper [30] describes the analysis and predistortion of gm-C leapfrog filters constructed from transconductors with a precise DC gain. The filter design approach that is presented is suitable for use when realizing wideband integrated filter circuits in modern deep-submicron CMOS technologies. This is because the losses of finite-DC-gain filter integrators forming the filter are taken into account in the filter synthesis and thus, a simple broadband transconductor with a low DC gain can be employed for



the filter integrators. The proposed approach originates from the collaboration of the author, Kaltiohallio, and Prof. Lindfors.

To demonstrate the feasibility of the filter design approach presented in paper [30], the author has designed, implemented, and measured three experimental filter circuits. Prof. Lindfors instructed the work. The first experimental circuit was implemented in a 0.13- $\mu\text{m}$  CMOS technology and the other two ICs in a 65-nm CMOS technology. The first implemented circuit is presented in paper [29] and the other two are presented in papers [33], [35], and [36].

Paper [29] describes a 240-MHz gm-C low-pass filter designed for a single-chip WiMedia UWB radio receiver in a 0.13- $\mu\text{m}$  CMOS technology. The filter design approach which conveniently combines a loss-mapping technique, a filter frequency response predistortion, a simple broadband pseudo-differential transconductor structure, and a negative resistance load was successfully used for the first time. The contribution of the author was described in the previous paragraph. Prof. Lindfors and Prof. Rynnänen participated in the writing of the manuscript for this paper. The research team which designed and implemented the single-chip WiMedia UWB receiver consisted of eight members altogether, including the author. The other researchers were Prof. Saska Lindfors, Prof. Jussi Rynnänen, D.Sc. Jouni Kaukovouri, Mikko Kaltiohallio, Olli Viitala, Kari Stadius, and Tapio Rapinoja. Prof. Kari Halonen was the leader who was responsible for the project. Prof. Lindfors, Prof. Rynnänen, and Kaltiohallio performed the system design. Prof. Rynnänen and D.Sc. Kaukovouri implemented the RF front-end. Stadius and Rapinoja implemented the synthesizer. Viitala and Prof. Lindfors implemented the ADC. Although most of the individual circuit blocks of the receiver IC that was implemented have been published separately, the entire receiver has not been published.

Paper [31] presents a theoretical analysis of common-mode induced even-order distortion in a pseudo-differential gm-C filter. The analysis that is presented is valuable when designing pseudo-differential baseband circuits in single-chip radio receivers. The mathematics and numerical calculations presented in the paper were carried out by the author under the supervision of Prof. Lindfors.

Paper [33] presents the second experimental implementation of the single-chip WiMedia UWB receiver in a 65-nm CMOS technology. The research team which designed, implemented, and measured the single-chip WiMedia UWB receiver consisted of seven members altogether, including the author. The other researchers were Prof. Saska Lindfors, Prof. Jussi Rynnänen, Mikko Kaltiohallio, Olli Viitala, Kari Stadius, and Tapio Rapinoja. Prof. Kari Halonen was the leader who was responsible for the

project. The author designed, implemented, and measured the low-pass filter, as described earlier, and participated in the receiver measurements. Prof. Lindfors, Prof. Rynänen, and Kaltiokallio performed the system design of the receiver. Kaltiokallio and Prof. Rynänen implemented the RF front-end. Stadius and Rapinoja implemented the synthesizer. Viitala and Prof. Lindfors implemented the ADC.

Paper [36] provides an extensive description of the implementation and measurement results of a 240-MHz gm-C low-pass filter designed for the single-chip WiMedia UWB receiver described in publication [33]. The author designed, implemented, and measured the low-pass filter, as already introduced. Prof. Lindfors and Prof. Rynänen participated in the writing of the manuscript. The baseline for the filter implementation is the same as in paper [29]. However, because of the 65-nm CMOS technology that was used, a re-design had to be done. For example, the capacitor matrices were completely re-designed. Moreover, as a result of further investigation, some improvements regarding the filter synthesis originally presented in paper [30] were made by the author and Kaltiokallio.

Paper [35] describes a 60-GHz single-chip radio receiver in a 65-nm CMOS with an on-chip ADC. The analog basebands for the I- and Q-branches of this experimental receiver IC are different. The I-branch consists of a 240-MHz low-pass filter, similar to that described in paper [36], and an on-chip ADC. The Q-branch incorporates a 1-GHz low-pass filter followed by a limiting amplifier chain. In paper [35], the focus is on the receiver with the I-branch. The research team which designed, implemented, and measured the experimental 60-GHz CMOS radio receiver consisted of eight members altogether, including the author. The other members were Prof. Saska Lindfors, Prof. Jussi Rynänen, Mikko Varonen, Mikko Kärkkäinen, Mikko Kaltiokallio, Olli Viitala, and Kalle Kekkonen. Prof. Kari Halonen was the leader who was responsible for the project. The author contributed to the receiver system design by carrying out manual calculations for the specifications of the 1-GHz analog baseband circuit. The 1-GHz filter designed by the author for this receiver is the third experimental filter implementation in which the filter design approach presented in paper [30] has been used. Varonen implemented the 60-GHz front-end. Kaltiokallio and Prof. Rynänen implemented the IF stage of the receiver. Viitala and Prof. Lindfors implemented the ADC. Kekkonen designed the limiter for the Q-branch, together with the author. In addition, the author participated in the receiver measurements and measured the low-pass filters of the I- and Q-branches.

### 1.3 Organization of the thesis

This thesis is organized into seven chapters. After the introduction, Chapter 2 gives an overview of the design of analog baseband filters for integrated radio receivers. The receiver architectures and wireless communication systems that are adopted in this thesis are briefly reviewed. In addition, the most important definitions and design parameters for analog baseband filters are presented.

Chapter 3 introduces different techniques used to realize integrator-based low-pass filters. The main emphasis is on the opamp-RC and gm-C techniques employed in the experimental circuits of this thesis. At the beginning of the chapter, the effect of integrator non-idealities on the filter frequency response is studied theoretically by means of the integrator Q-factor.

In Chapter 4, some important matters related to filter prototype design are first briefly reviewed from the literature. The main focus in this chapter is, however, on filter synthesis with lossy integrators. In particular, a filter design approach for continuous-time gm-C low-pass filters consisting of lossy integrators is proposed. In addition to the following chapters, 5–7, this chapter is one of the main parts of this thesis.

Chapter 5 describes the circuit design of the first two experimental filter circuits of this work, together with the measurement results of both the filters and the corresponding integrated RF receivers. The SiGe BiCMOS technology and opamp-RC technique are utilized in the filter realizations that are presented. In addition, in the first section, design issues related to the implementation of a single-chip multicarrier WCDMA base-station receiver are addressed. Moreover, in the second section, design issues related to the implementation of the RF-baseband interface in integrated radio receivers are studied.

Chapter 6 concentrates on circuit techniques for wideband pseudo-differential gm-C filters in modern ultra-deep-submicron CMOS technologies. The main emphasis is on the broadband, pseudo-differential transconductor circuit that was designed, as well as on the linearity analysis performed for a pseudo-differential gm-C filter.

In Chapter 7, three experimental gm-C filter circuits implemented in ultra-deep-submicron CMOS technologies as a part of an integrated radio receiver are presented, together with the measurement results. In addition, the experimental results of the corresponding WiMedia UWB radio receiver IC and the 60-GHz radio receiver IC are shown. Finally, the thesis is summarized with conclusions.

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## 2 Overview of analog baseband filters in radio receivers

In this work, the analog baseband low-pass filter is defined as the receiver block between the RF front-end and the analog-to-digital converter (ADC). In a superheterodyne receiver, however, it is placed between the IF stage and the ADC, to be exact. The analog baseband filter is responsible for performing channel-select filtering, either partially with the digital back-end or completely in the analog domain. In addition, the preceding receiver stages may also include passive filters, potentially alleviating the selectivity, and, especially, the stopband linearity requirements of the analog baseband filter. The partitioning of the filtering in a radio receiver depends on the receiver architecture selected, the gain and the linearity of the receiver building blocks employed, and the wireless application that is targeted, including the interferer scenario. The analog baseband filter can be a continuous-time or a discrete-time filter. Continuous-time filters have a speed advantage when compared to their discrete-time counterparts, since no sampling is required [1]-[3]. Therefore, it is often the case that continuous-time filters are more suitable for wideband applications. Moreover, the following ADC requires anti-aliasing filtering, which can be performed only by continuous-time filters. To accomplish simultaneous channel-select and anti-aliasing filtering and hence to reduce the number of power-consuming and noisy filter stages in a receiver, the employment of continuous-time low-pass filters is a practical choice. This work concentrates on the design and implementation of continuous-time filters and, thus, discrete-time filters are excluded from this thesis.

In direct-conversion and low-IF receivers, the analog baseband circuit is typically required to have an adjustable gain control to amplify both the minimum and maximum in-band signals that are received to the desired full-scale level of the following ADC. When aiming at a compact and more power-efficient realization with a reduced noise contribution, it is beneficial, at least partially, to merge the low-pass filter and the variable gain amplifier together at the baseband.

When analog baseband filters for radio receiver ICs are being designed, there are many issues that have to be addressed, including the receiver architecture adopted and the requirements set by the wireless application that is targeted. Particularly in direct-conversion and low-IF receivers, the performance and the realization of the preceding RF front-end and of the following ADC affect the performance requirements and the implementation of the analog baseband block.

This chapter gives a system overview of analog baseband circuit design in radio receivers. First, three different receiver architectures are reviewed in Section 2.1. All the architectures presented have been adopted in the five application cases presented in Chapter 5 and Chapter 7 of this thesis. Important design parameters of the analog baseband filter are examined and defined in Section 2.2. Section 2.3 discusses issues that have to be considered when analog baseband filters for single-chip radio receivers are being designed. The main emphasis is on the different choices that can be made in the system-level design of an interference-tolerant receiver. At the end of this chapter, there is a brief introduction to the UTRA FDD WCDMA mobile communication system, as well as to the WiMedia UWB and 60-GHz radio technologies. The experimental ICs of this work were originally targeted for the wireless applications that are discussed.

## **2.1 Receiver architectures**

This section gives a review of the three most frequently used receiver architectures, covering superheterodyne, direct-conversion, and low-IF receivers. All the topologies that are studied are adopted, potentially with some modifications, in the application cases presented in this thesis. Other receiver architectures, such as wideband-IF, sub-sampling, RF sampling, and super-regenerative receivers [4]-[7], also exist, but they are not described in this thesis. In addition, a software-defined radio, cognitive radio, and concurrent dual-band receiver are discussed elsewhere [8]-[11].

### **2.1.1 Superheterodyne receiver**

Superheterodyne architecture, shown in Fig. 2.1, is based on a concept in which the RF signal that is received is downconverted into one or multiple intermediate frequencies (IF) before the final translation into the baseband and digitization. It has been the most widely used architecture in radio receivers in the past and is known for its high sensitivity and selectivity [12], [13]. The excellent sensitivity and selectivity are achieved by sequentially performing filtering and signal amplification in cascaded



receiver stages and, especially, by employing passive highly linear and selective RF and IF filters. As a drawback, the high-Q RF and IF filters are, in practice, realized with external (i.e. off-chip) passive components, thus reducing the level of integration of the receiver. Moreover, the incorporation of several receiver stages increases the power consumption and complexity of the system. Therefore, during the past decade, the more compact direct-conversion counterpart suitable for full integration has become popular in wireless communication system applications.

The conventional operation of the superheterodyne receiver is as follows. Before the downconversion, usually to a fixed IF, the signal that is received is filtered and amplified at RF with a passive pre-select band-pass filter and a low-noise amplifier (LNA), respectively, as shown in Fig. 2.1. In a traditional superheterodyne receiver, another RF band-pass filter is placed between the LNA and the downconversion mixer to perform image rejection. The image-reject filter is not needed if Hartley's [14] or Weaver's [15] image-reject receiver topology is deployed. The first downconversion is followed by a high-Q band-pass IF filter, which performs the channel selection by attenuating unwanted out-of-channel signals. The desired signal at the output of the IF filter is next amplified with a variable gain amplifier (VGA) prior to the downconversion to a lower IF or the demodulation of the signal. The IF stage considerably relaxes the out-of-band linearity and in-band dynamic range requirements of the subsequent stages. The demodulator depicted in Fig. 2.1 consists of a quadrature downconversion mixer and an analog baseband low-pass filter. The latter finalizes the channel selection and acts as an anti-aliasing filter for the analog-to-digital converter (ADC).

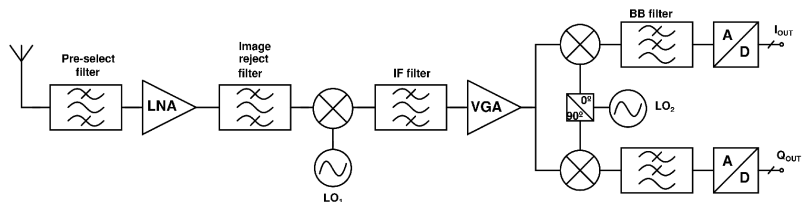


Figure 2.1. Superheterodyne receiver.

### 2.1.2 Direct-conversion receiver

In a direct-conversion receiver, shown in Fig. 2.2, the received RF signal is directly downconverted to the baseband (i.e. zero-IF) without any additional receiver stages. Therefore, this receiver architecture is also called a homodyne or zero-IF receiver [16]. In the case of direct conversion reception, the image band is the same as the signal band itself. This eliminates the need for the off-chip image-reject filter but necessitates the

use of a quadrature downconversion mixer. Similarly to the superheterodyne receiver, the incoming RF signal is first filtered and amplified with a pre-select band-pass filter and an LNA, respectively. However, instead of external channel-select IF filters, the analog baseband low-pass filter is responsible for further filtering the signal that is received and selecting the desired channel with a digital baseband filter. The selectivity and linearity requirements of the analog baseband filter become more stringent compared to its superheterodyne counterpart because of the absence of preceding highly linear high-Q RF and IF filters. The baseband low-pass filters in the I and Q signal branches can be integrated with the remaining sections of the receiver. Moreover, the integrated analog filters can be designed to be programmable, which makes the direct-conversion receiver suitable for multi-band, multi-standard operation [17], [18].

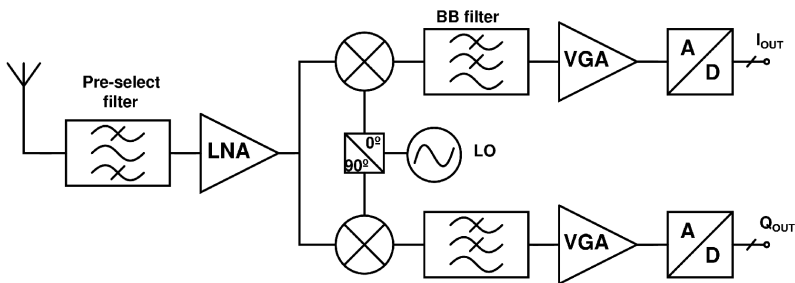


Figure 2.2. Direct-conversion receiver.

Typically, in a radio receiver, a VGA is employed to adjust the amplitude of the signal that is received to the desired full-scale level of the ADC. In a direct-conversion receiver, this amplifier is usually implemented in the baseband, as depicted in Fig. 2.2. Because of the moderate gain provided by the RF front-end and the elimination of the IF stage, the variable gain range of the VGA may be required to be several tens of decibels. For the same reason, the noise contribution of the baseband circuitry becomes considerably higher compared to the superheterodyne receiver.

Besides the advantages, including the high degree of integration and the potential for reduced power consumption and lowered costs compared to its superheterodyne counterpart, undesired phenomena specific to this particular architecture also exist. DC offset voltages can corrupt the desired downconverted signal located around zero frequency or saturate the subsequent receiver stages [19]. The origin of DC offsets is mainly related to the fact that in the direct-conversion receiver the RF and LO frequencies are the same. Even-order non-linearities in the receiver will also generate DC offsets, in addition to unwanted low-frequency even-order distortion. A gain and phase imbalance between the I and Q branches will degrade the

operation of the demodulator, thereby increasing the bit error rate. Furthermore, flicker noise can cause the signal-to-noise ratio (SNR) to deteriorate at frequencies close to zero. These phenomena are discussed in more detail in, for example, [16], [19]-[23]. It is mandatory to take them into account when designing analog baseband filters for direct-conversion receivers.

### 2.1.3 Low-IF receiver

The block diagram of the low-IF receiver is basically the same as for its direct-conversion counterpart shown in Fig. 2.2. The difference is that the RF signal that is received is downconverted with a quadrature mixer to a low intermediate frequency (IF), not to the zero-IF one. Typically, the IF is selected to be as low as one or two times the signal bandwidth [13], [24], [25]. The idea behind the low-IF receiver topology is the ambition to combine the benefits of the superheterodyne and direct-conversion receivers. Since the downconverted signal is not located around DC, the DC offset problem is alleviated and the effect of flicker noise is reduced compared to the direct-conversion approach. Similarly to the direct-conversion receiver, the image frequency is not attenuated prior to the first quadrature downconversion. Thus, instead of external high-Q RF and IF filters, the downconverted signal is filtered in the quadrature paths with complex bandpass, real bandpass, or real low-pass analog filters [24], [25]. All these alternatives can be integrated on the same silicon chip with the entire receiver because of the low IF. However, as opposed to the direct conversion counterpart, the bandwidth of the I and Q channels at a low IF equals the RF signal bandwidth. This requires a wider bandwidth, twice at the minimum, from the analog filters that are employed when compared to the baseband low-pass filters in a direct-conversion receiver.

After filtering at the low IF, the signal that is received needs to be downconverted from the IF to the baseband for demodulation, as is also the case in superheterodyne receivers. In a low-IF receiver, the second downconversion can be carried out either in the analog or in the digital domain. One of the main challenges in low-IF receivers is to obtain the high I/Q matching required for the separation of the desired signal from its image after the first quadrature downconversion [26], [27]. Therefore, probably the most feasible choice in many cases is to sample the signal at the low IF after the filtering, as shown in Fig. 2.2. In this option, the rest of the signal processing operations are performed in the digital domain, in which perfect matching can be achieved. The sample rate and dynamic range requirements of ADCs operating at the low IF are more demanding

compared to their direct-conversion counterparts when the ADCs are preceded by real analog filters instead of complex ones [24].

## 2.2 Definitions and design parameters for analog baseband filters

This section provides an overview of the most important design parameters and definitions related to analog baseband filter design in radio receivers. The key design parameters, presented here at a general level, are used in the later parts of this thesis when the design and testing of the experimental filter circuits aimed at a particular receiver and wireless application are being described. In radio receiver design, a lot of attention has to be paid to the noise and linearity performance of the analog baseband circuit in order not to seriously limit the dynamic range of the entire receiver. The noise and linearity of the analog baseband circuit are critical design parameters, especially in direct-conversion and low-IF receivers, as a result of the absence of high-gain stages and high-Q passive filters prior to the baseband (or low-IF) block. Owing to the low supply voltage of modern ultra-deep-submicron CMOS processes, as well as the reduced intrinsic gain of transistors, it is challenging to achieve a high dynamic range in the analog baseband.

In radio receiver IC design, the analog baseband designer must be familiar with using both *dBm* values and power gains, as well as *dBV* values and voltage gains. This is because in RF design power values are conventionally used and, for example, the linearity specifications for the whole receiver are typically given as *dBm* values. However, in analog baseband IC design, it is much more convenient to use *dBV* values and voltage gains. This is because, usually, the impedance levels at the input and output interface and at the internal nodes of the analog baseband circuit cannot be well defined. A more comprehensive discussion of this subject is given in [23].

### 2.2.1 Sensitivity and input-referred noise voltage

The reliability of a digital system is typically measured in terms of a bit error rate (BER) in the data transmission [28]. The BER defines the number of bits received erroneously. A small BER value corresponds to a high-quality system. Sensitivity is the minimum signal at the receiver input for which there is a sufficient signal-to-noise ratio (SNR) at the receiver output in order to achieve a given BER in the detection. Sensitivity can be defined as [12], [28]

$$P_{in,\min} = -174 \text{ dBm/Hz} + 10 \log(B_{RF}) + NF_{RX} + SNR_{\min}, \quad (2.1)$$

where  $-174 \text{ dBm/Hz}$  is the available noise power from the source at a temperature of  $290 \text{ K}$ ,  $B_{RF}$  is the equivalent RF noise bandwidth of the channel,  $NF_{RX}$  is the overall noise figure of the receiver, and  $SNR_{\min}$  is the minimum signal-to-noise ratio required for successful detection. The noise figure of the receiver is a measure of how much the SNR degrades as the incoming signal passes through the receiver [12]. As can be seen in (2.1), the noise figure of the receiver ( $NF_{RX}$ ) is the key design parameter for sensitivity in wireless receivers. The overall noise figure of an integrated receiver can be calculated by means of the cascade noise figure of each receiver stage when the fact that the interfaces are not power-matched in an integrated receiver is taken into account [12], [22], [29], [30]. However, since the impedance level at the mixer-baseband interface typically differs from the nominal  $50\text{-}\Omega$  impedance in an on-chip receiver, it is more convenient to express the noise of the analog baseband block either with an input-referred noise voltage integrated over a specific frequency band or with an input-referred noise density instead of a noise figure. The relation between the overall receiver noise figure and the input-referred noise voltage of the analog baseband circuit ( $\bar{v}_{n,in,BB}$ ) can be expressed as

$$NF_{RX} = 10 \log_{10} \left[ 10^{NF_{RF}/10} + \frac{(\bar{v}_{n,in,BB})^2}{kTB_{RF}R_S(A_{v,RF})^2} \right], \quad (2.2)$$

where  $NF_{RF}$  and  $A_{v,RF}$  are the noise figure and the voltage gain of the RF front-end (or the RF front-end and the IF stage), respectively,  $k = 1.3807 \cdot 10^{-23} \text{ J/K}$  is the Boltzmann's constant,  $T = 290 \text{ K}$  is the temperature,  $R_S$  the source resistance ( $50 \text{ }\Omega$  or  $100 \text{ }\Omega$  in practice), and  $B_{RF}$  is the equivalent RF noise bandwidth of the channel. In a direct-conversion and superheterodyne receiver, the equivalent baseband noise bandwidth is  $B_{BB} = B_{RF} / 2$  as a result of the quadrature signal processing. The equivalent baseband noise bandwidth can be defined as

$$B_{BB} = \frac{1}{|H(f_1)|^2} \int_0^{\infty} |H(f)|^2 df, \quad (2.3)$$

where  $H(f)$  is the frequency response of the filter. In (2.3), the gain of the filter is defined at a baseband frequency  $f$ . It should be pointed out that although there are two identical downconversion mixers and analog baseband circuits in a receiver, in the event of quadrature signal processing,

the noise contribution of each receiver building block is still accounted for only once in (2.2), as is explained in more detail in [29].

It can be concluded in (2.2) that the input-referred noise voltage of the analog baseband block has to be sufficiently low not to degrade the overall noise figure of the receiver too much. However, the total receiver noise figure does not depend only on the input-referred noise voltage of the analog baseband circuit but also the voltage gain of the RF front-end. Therefore, in system-level design, it has to be taken into account that, in addition to PVT variations, the gain of the RF front-end can degrade, for example, as a result of a phenomenon called blocking [31]. The degraded gain of the RF front-end leads directly to an increased receiver noise figure.

### 2.2.2 Linearity

To meet the BER requirement in the detection, the SNR at the receiver output should not be degraded by unwanted spurious signals, i.e. harmonics and intermodulation distortion components generated by non-linear receiver blocks. The behavior of a weakly non-linear memoryless time-invariant system can be modeled with the first four terms of a Taylor series expansion [12], [22], [32]:

$$v_{out}(t) = \alpha_0 + \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t), \quad (2.4)$$

where  $\alpha_0$  is the DC offset,  $\alpha_1$  is the linear gain of the system, and  $\alpha_2$  and  $\alpha_3$  are the second- and third-order non-linear coefficients of the system, respectively. In this subsection, gain compression and harmonic distortion, as well as the second- and third-order intercept points, are studied by means of (2.4) after the discussion of in-channel and out-of-channel linearity in radio receivers.

#### 2.2.2.1 In-channel and out-of-channel linearity

A radio receiver must be able to pass and amplify the desired in-channel signals, not only with low added noise but also with acceptably small power levels of spurious signals in order to avoid degrading the SNR and, hence, the signal quality in the detection at the receiver output. As a consequence, in-channel and out-of-channel linearity are important design parameters in radio receivers. Let us start the discussion with the latter.

Potentially, there are large interfering signals present in the neighborhood of the desired channel at the wireless receiver input. These interfering signals may also include leakage signals from the transmitter(s) integrated on the same silicon chip or embedded into the same mobile terminal as the receiver. In any case, receiver non-linearities will produce harmonics and

intermodulation distortion components when the incoming signal contains out-of-channel interfering signals. From the successful signal detection standpoint, the distortion components that fall into the desired channel in the receiver are the most harmful ones. Moreover, in an extreme case, the inadequate attenuation of the out-of-channel interfering signals in the preceding receiver stages can lead to saturation of the subsequent stages. Therefore, it is often the case that the radio receiver has to be capable of handling large out-of-channel interfering signals, as well as suppressing them to a sufficiently low power level while simultaneously passing the desired, potentially weak, in-channel signal with an acceptable SNR. This mandates linear out-of-channel signal processing in a radio receiver. Particularly in direct-conversion and low-IF receivers, the stopband linearity of the analog baseband filter plays an important role when the rejection of out-of-channel signals before the analog-to-digital conversion is being considered. The stopband linearity requirement of the analog baseband filter can be considerably alleviated by suppressing out-of-channel interfering signals in the preceding receiver stages.

As the power level of the desired in-channel signals is small, the out-of-channel linearity typically dominates in a wireless receiver. However, when the power level of the in-channel signals is higher (i.e. closer to the maximum specified value), the in-channel linearity must also be taken into consideration. This is due to the fact that the unwanted spurious signals caused by high-power-level in-channel signals may become as significant as the ones resulting from out-of-channel non-linearities. The last receiver stages prior to the ADC are usually responsible for handling the largest in-channel signals, since the signals are deliberately amplified to the desired full-scale level of the ADC. At the same internal nodes, out-of-channel interfering signals have already been rejected, at least to some extent, by the preceding receiver stages. Therefore, the last receiver stages prior to the ADC, including the analog baseband filter, are liable to encounter a more demanding in-channel linearity requirement than the first receiver stages.

It is worth pointing out that the in-band linearity of a continuous-time low-pass filter is not constant over the whole passband. The in-band linearity is usually highest at frequencies close to DC. Correspondingly, the in-band linearity tends to be worst at frequencies close to the passband edge because the gains of the internal filter nodes typically have their maximum values at those frequencies. In addition, the loop gain usually decreases at higher frequencies, simultaneously degrading the linearity of feedback-connected structures.

### 2.2.2.2 Gain compression and harmonic distortion

When a single sinusoidal signal,  $A_1 \cos(\omega_1 t)$ , is applied to the input of a non-linear circuit modeled with (2.4), the output signal can be written as

$$v_{out} = \left( \alpha_0 + \frac{\alpha_2 A_1^2}{2} \right) + \left( \alpha_1 A_1 + \frac{3\alpha_3 A_1^3}{4} \right) \cos(\omega_1 t) + \frac{\alpha_2 A_1^2}{2} \cos(2\omega_1 t) + \frac{\alpha_3 A_1^3}{4} \cos(3\omega_1 t) \quad (2.5)$$

It can be seen in (2.5) that the fundamental frequency component includes a third-order term in addition to the linear gain  $\alpha_1$ . When  $\alpha_1$  and  $\alpha_3$  have an opposite sign, the total coefficient of the fundamental frequency component at the circuit output becomes smaller than the linear gain  $\alpha_1$  when the amplitude  $A$  of a single-tone input signal is increased (although typically  $\alpha_1 \gg \alpha_3$ ). This phenomenon, shown in Fig. 2.3, is called gain compression. The *input -1-dB compression point* (ICP) is defined as being the input signal power at which the gain of the circuit is reduced by 1 dB from its linear gain value.

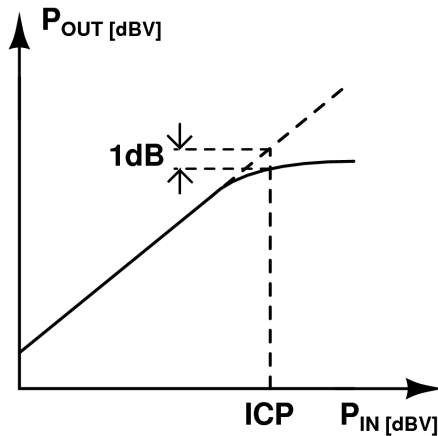


Figure 2.3. Definition of the input -1-dB compression point (ICP).

As can be seen in (2.5), the output signal of a non-linear circuit also includes the harmonics of the fundamental component at the frequencies  $2f_1$  and  $3f_1$  when a single-tone signal is inserted into the circuit. The *third-order harmonic distortion* ( $HD_3$ ) is defined as the magnitude ratio between the third harmonic component and the fundamental component. The *second-order harmonic distortion* ( $HD_2$ ) is defined similarly by comparing the magnitude of the second harmonic component with the magnitude of the fundamental component. In low-pass filter design, a common



parameter for measuring the filter passband linearity is to use the *total harmonic distortion (THD)* [23], [32]

$$THD = \sqrt{\frac{\sum_{n=2}^N |V_{out}(nf_1)|^2}{|V_{out}(f_1)|^2}}, \quad (2.6)$$

where  $N-1$  harmonics are taken into account. In practice, however, integrated analog baseband filters are designed to be balanced structures in which the odd-order harmonics dominate. Therefore, in weakly non-linear balanced filter circuits, it is the third-order harmonic component that dominates and  $THD$  is often approximated with  $HD_3$ . The other reason for this approximation is that higher-order harmonics easily lie at the stopband of the filter and are thus filtered out. Even the third-harmonic component can appear at the stopband when the frequency-dependent in-band linearity of a low-pass filter is supposed to be measured at frequencies close to the passband edge. In wireless receiver design, the second- and third-order intercept points studied in the following subsection are typically used as design parameters instead of  $THD$ .

### 2.2.2.3 Third- and second-order intercept points

The linearity of a radio receiver and its building blocks is typically characterized with one or multiple two-tone tests. Since receiver building blocks are weakly non-linear circuits, only the second- and third-order distortion are of importance. When a two-tone signal,  $A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$ , is applied to the input of a non-linear circuit modeled with (2.4), the output signal contains harmonics and intermodulation products in addition to the two fundamental signal components, as presented, for example, in [22], [32], and [33].

When the third-order non-linearity is considered, the third-order intermodulation terms of the output signal

$$v_{IMD3}(t) = \frac{3}{4} \alpha_3 A_1^2 A_2 \cos(2\omega_1 t - \omega_2 t) + \frac{3}{4} \alpha_3 A_1 A_2^2 \cos(2\omega_2 t - \omega_1 t) \quad (2.7)$$

are of interest. As can be seen in (2.7), if  $A_1$  equals  $A_2$ , the amplitude of the third-order intermodulation product depends on the third power of the input signal amplitude  $A_i$ . As a consequence, the power of the third-order intermodulation component increases by 3 dB at the circuit output when the level of the input test signals is enlarged by 1 dB. This is illustrated in Fig. 2.4. The *third-order input intercept point (IIP3)* is defined as being the point at which the extrapolated curves of the fundamental signal

component and the third-order intermodulation distortion component intercept in a log-log scale. Mathematically, the  $IIP_3$  can be represented as

$$IIP_3 = \frac{3P_{IN} - P_{IMD3,IN}}{2} = P_{IN} + \left( \frac{P_{OUT} - P_{IMD3,OUT}}{2} \right), \quad (2.8)$$

where  $P_{IN}$  is the power of the fundamental input signal component,  $P_{IMD3,IN}$  the power of the input-referred third-order intermodulation product,  $P_{OUT}$  the power of the fundamental signal component at the circuit output, and  $P_{IMD3,OUT}$  the power of the third-order intermodulation product at the circuit output. In (2.8), all the parameters must be expressed either in  $dBm$  values or  $dBV_{RMS}$  values. For the linearity analysis presented in Section 6.6, the  $IIP_3$  can be written as a function of the linear gain  $\alpha_i$  and the third-order non-linear coefficient  $\alpha_3$  as

$$IIP_3[dBV_{RMS}] = 20 \log_{10} \left( \frac{\hat{v}_{iip3}}{\sqrt{2}} \right) = 10 \log_{10} \left( \frac{2}{3} \left| \frac{\alpha_1}{\alpha_3} \right| \right). \quad (2.9)$$

Equation (2.8) is valid only for two test tones that have equal powers. However, in the interfering scenarios of some communication systems, such as the WiMedia UWB, there can be cases in which the interfering signals are assumed to have different powers. In this case, the  $IIP_3$  can be calculated as [34]

$$IIP_3 = \frac{1}{2} P_{IN,\omega_1} + P_{IN,\omega_2} - \frac{1}{2} P_{IMD3,IN}, \quad (2.10)$$

where  $P_{IN,\omega_1}$  and  $P_{IN,\omega_2}$  are the powers of the two interferers and  $P_{IMD3,IN}$  the power of the input-referred third-order intermodulation product. Equation (2.10) is valid only when the condition  $\omega_{IMD3} > \omega_2 > \omega_1$  is satisfied.

Next, the second-order non-linearity, which plays a crucial role in direct-conversion radio receivers, is examined. In this case, the second-order intermodulation terms of the output signal

$$v_{IMD2}(t) = \alpha_2 A_1 A_2 \cos(\omega_1 t - \omega_2 t) + \alpha_2 A_1 A_2 \cos(\omega_2 t - \omega_1 t) \quad (2.11)$$

are of interest. Again, the test tone frequencies,  $f_1$  and  $f_2$ , have to be chosen to be such that one of these second-order intermodulation products falls in the passband of the baseband low-pass filter of the receiver. When  $A_1 = A_2$ , the power of the second-order intermodulation component increases by 2 dB at the circuit output when the level of the input test signals is enlarged by 1 dB. The *second-order input intercept point* ( $IIP_2$ ) is defined as being the point at which the extrapolated curves of the fundamental signal

component and the second-order intermodulation distortion component intercept in a log-log scale, as shown in Fig. 2.4. The  $IIP2$  can be mathematically represented as

$$IIP2 = 2P_{IN} - P_{IMD2,IN}, \quad (2.12)$$

where  $P_{IN}$  is the power of the fundamental input signal component and  $P_{IMD2,IN}$  the power of the input-referred second-order intermodulation product, both expressed either in  $dBm$  values or  $dBV_{RMS}$  values. For the linearity analysis presented in Section 6.5, the  $IIP2$  can be written as a function of the linear gain  $\alpha_1$  and the second-order non-linear coefficient  $\alpha_2$  as

$$IIP2[dBV_{RMS}] = 20 \log_{10} \left( \frac{\hat{v}_{iip2}}{\sqrt{2}} \right) = 20 \log_{10} \left( \frac{|\alpha_1|}{\sqrt{2}|\alpha_2|} \right). \quad (2.13)$$

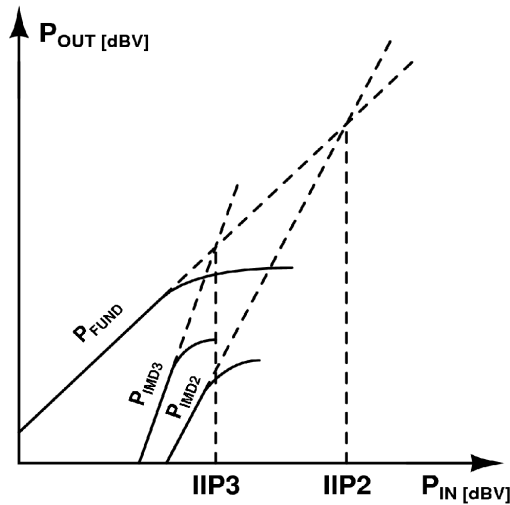


Figure 2.4. Definition of the second- and third-order intercept points ( $IIP2$  and  $IIP3$ ).

#### 2.2.2.4 Third-order intercept point for cascaded receiver blocks

The third-order input intercept point ( $IIP3$ ) of each receiver stage can be calculated using the following equation for the cascaded  $IIP3$  of a coherent receiver [30], [34]-[36]

$$\frac{1}{iip3_{tot}} = \frac{1}{iip3_1} + \frac{G_1}{iip3_2} + \dots + \frac{\prod_{i=1}^{n-1} G_i}{iip3_n}, \quad (2.14)$$

where  $iip3_n$  and  $G_n$  are the third-order input intercept point (expressed in watts, not in  $dBm$  values) and the power gain (expressed as absolute values,

not in decibels) of the  $n$ th receiver block, respectively. In (2.14), the power gain can be replaced by the square of the voltage gain.

### 2.2.3 Spurious-free dynamic range

The *spurious-free dynamic range* (*SFDR*) is a measure of a receiver's ability to operate in a dense signal environment, partially treated in Section 2.2.2.1. The *SFDR* determines, in decibels, the level of a two-tone IIP<sub>3</sub> test signal above the input-referred in-channel noise power ( $P_{NOISE,IN}$ ) which creates input-referred third-order intermodulation products equal to the input-referred noise. Mathematically, the SFDR can be represented as

$$SFDR = \frac{2}{3} (IIP3 - P_{noise,in}). \quad (2.15)$$

According to (2.15), the third-order non-linearity as given by the IIP<sub>3</sub> and the input-referred noise of the baseband low-pass filter determine the *SFDR* of the filter. The *SFDR* can be defined using both the in-channel and out-of-channel IIP<sub>3</sub>.

### 2.2.4 Selectivity

Selectivity is a measure of a receiver's ability to separate the desired band around the carrier frequency from unwanted signals received at out-of-band frequencies. The interfering scenarios alternate in different wireless communication systems and therefore, in radio receiver design, a wide variety of receiver test cases exist. These include different in-band and out-of-band blocking and intermodulation distortion tests, as well as the adjacent channel selectivity. The RF and analog IC designers have to take into account all the test cases that are specified for the radio system that is targeted. The selectivity requirement for the analog baseband filter is derived from these test cases, together with the receiver system-level design covering the receiver architecture that is selected and the performance of the following ADC. In integrated radio receivers intended for wireless communication systems, a typical figure that one can find in the literature for the order of continuous-time low-pass filter implementations is in the range from three to seven.

### 2.2.5 DC offset

Because of different mechanisms in radio receivers, and direct-conversion receivers in particular, both static and dynamic (i.e. time-varying) DC offset exists at the input of the analog baseband circuit. These phenomena are

discussed in, for example, [16], [19]-[23], and [37]-[39]. Without any DC offset removal scheme at the baseband, the DC offset will pass the low-pass filter and be amplified by the variable gain amplifier prior to the ADC. In addition, the analog baseband circuit alone will produce DC offset at its output. Therefore, the analog baseband circuit has to be capable of reducing the DC offset to a sufficiently low level in order to avoid saturating the ADC and to meet the given BER. The amount of DC offset allowed at the input of the ADC depends on the resolution and the full-scale input signal of the ADC. Dynamic DC offset is usually more difficult to overcome than static.

The total DC offset voltage at the output of a multistage amplifier circuit can be calculated as the sum of the offset voltages of the individual circuit stages:

$$V_{OUT} = a_1V_{OS1} + a_2V_{OS2} + \dots + a_nV_{OSn}, \quad (2.16)$$

where  $a_1$  is the voltage gain from the circuit input (i.e. the input of the first stage) to the circuit output,  $a_2$  is the gain from the input of the second stage to the circuit output etc.

### 2.2.6 Group delay

The *frequency response*, or, more generally, the *transfer function* of a filter can be represented as

$$H(j\omega) = |H(j\omega)|e^{j\theta(\omega)}, \quad (2.17)$$

where  $|H(j\omega)|$  and  $\theta(\omega)$  are the *magnitude and phase responses* of the filter. The latter defines how much the phase of a sinusoidal signal is shifted when the signal passes through the filter. The *group delay* function is a measure of the linearity of the phase response. It is defined as

$$\tau(\omega) = -\frac{d\theta(\omega)}{d\omega}. \quad (2.18)$$

On the basis of (2.18), a constant group delay indicates a linear phase response. More importantly, all the signal components are then delayed by the same amount. A more comprehensive study is given in, for example, [40].

In general, it is challenging to design a filter that has both a sharp magnitude response shape and a linear phase response. Once the magnitude response has been specified, one has to live with the resulting phase [2]. However, in certain applications, such as in video and digital

transmission systems, the phase changes introduced by a filter can cause intolerable distortion to the shape of the time-domain signal [2]. As an example, continuous-time filters designed for hard disk drive read channels are usually required to have a linear phase response (i.e. a constant group delay) over a given frequency range [41]-[44]. In the application cases presented in this thesis, only the magnitude responses of the continuous-time low-pass filters are of concern. Phase linearization (i.e. group delay equalization) is left for delay equalizers and all-pass filters to be implemented in the digital domain after the analog-to-digital conversion.

### 2.2.7 Figure of merit

The performance of the filter can be evaluated by the following figure of merits (FoMs). A FoM describing the power dissipation of the filter per the number of filter poles per the filter bandwidth is defined as [3]

$$FoM1 = \frac{P_D}{N \times f_{-3dB}}, \quad (2.19)$$

where  $P_D$  is the power dissipation of the filter,  $N$  is the number of the filter poles, and  $f_{-3dB}$  is the filter  $-3$ -dB frequency (i.e. bandwidth). When the noise and linearity performance of the filter are also taken into account, equation (2.19) can be expanded by means of the spurious-free dynamic range of the filter as [45], [46]

$$FoM2 = \frac{P_D}{N \times f_{-3dB} \times SFDR}. \quad (2.20)$$

It should be noted that the SFDR describes either the in-band or out-of-band performance of the filter as discussed in Section 2.2.3. The filters of this work are designed to have voltage gain. Therefore, in this thesis, the FoM2 defined in (2.20) is expanded next with the gain of the filter in a similar fashion as the gain is taken into account in the FoMs that are defined for LNA designs [47], [48]:

$$FoM3 = \frac{P_D}{G \times N \times f_{-3dB} \times SFDR}, \quad (2.21)$$

where  $G$  is the gain of the filter in absolute values. If the active chip area occupied by the integrated filter is also taken into account, (2.21) can be further expanded as [49]

$$FoM4 = \frac{P_D \times Area}{G \times N \times f_{-3dB} \times SFDR}. \quad (2.22)$$

These FoMs are used in Chapter 5 and Chapter 7 to compare the performance of the filters presented in this thesis with the work of others. Let us consider the limitations related to the FoMs presented in this section. It is worth pointing out that the FoMs (2.19)-(2.22) do not fully take the selectivity of the filter into account. This is because the number of poles (i.e. the filter order) does not unambiguously describe the selectivity of the filter if the filter prototype is omitted. This is the case in the FoMs presented above. Therefore, the maximum quality factor of the filter poles is also sometimes taken into account when defining a FoM for a filter, as presented in, for example, [50]. It may not be straightforward, however, to find out the maximum pole quality factor in the filter publications and hence, the pole quality factor is not included in (2.19)-(2.22). Neither is the effect of a low nominal supply voltage compensated in the FoMs (2.19)-(2.22), although a low supply voltage tends to reduce the achievable *SFDR*.

### 2.3 Partitioning of filtering and amplification

This section briefly discusses some system-level issues related to the partitioning of filtering and signal amplification in single-chip radio receivers. The main purpose is to highlight the fact that there are several different alternative ways to distribute the gain and the filtering in a radio receiver. It is essential to pay careful attention to system design when implementing interference-tolerant radio receivers, for example, for WiMedia UWB applications.

A mobile terminal may contain several radio systems, and in addition, it is likely that the terminal will be used in an environment where many wireless systems are operating simultaneously. Hence, a radio receiver IC intended for such terminals must be able to operate in the presence of, for example, ad hoc networks and cellular systems. This requirement will set stringent demands for the selectivity and out-of-band linearity of the radio receiver. At the same time, in highly-integrated single-chip radio receivers, passive off-chip filtering at the internal nodes of the receiver should be avoided. A single pre-select filter at the receiver input is the only acceptable external component that can be employed to linearly suppress unwanted out-of-band interfering signals prior to the receiver IC. In direct-conversion and low-IF receivers, the channel-select filtering is performed at the baseband, either partially with the digital back-end or completely in the analog domain, as depicted in Fig. 2.5. The stopband linearity requirements of the

analog baseband filter, mainly consisting of active devices, may become unreasonable if potentially large out-of-band interfering signals that are received are not attenuated before the baseband filter. The baseband filter is not allowed to limit the out-of-band linearity of the receiver. As a solution to the problem of alleviating the aforementioned linearity requirements, the low-noise amplifier (LNA) or the downconversion mixer of the preceding RF front-end may include an on-chip bandpass or notch filter, or an RF loop [51]-[58]. They are designed to suppress the most harmful blocking signals before the signal processing with active devices at the baseband. Another possibility is to implement a real pole with passive components at the mixer-baseband interface [59]-[63], as will be discussed in more detail in Sections 4.1.2 and 5.2. Both these options are illustrated in Fig. 2.5. It is also worth pointing out that the analog baseband filter is ordinarily designed in conjunction with the ADC. The greater stopband rejection provided by the former, together with the preceding receiver stages, reduces the sampling rate and number of bits required and, thus, the power consumption of the latter [23], [64].

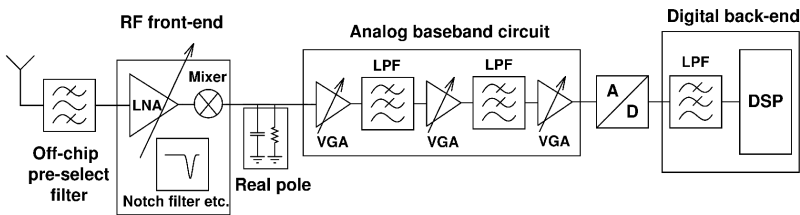


Figure 2.5. Partitioning of filtering and signal amplification in a direct-conversion or a low-IF radio receiver.

To fully utilize the dynamic range of the ADC, a full-scale signal swing at the ADC input is desired. Hence, the preceding receiver chain must be capable of amplifying both minimum and maximum in-band signals that are received to the full-scale level of the ADC. This is typically performed by employing variable gain amplifiers (VGAs). The expected difference between the minimum and maximum powers of the incoming signal depends on the wireless application being targeted. On the other hand, the chosen ADC topology, together with the performance that is targeted, determines the desired full-scale signal level at the ADC input. The variable gain range required and the optimal size of the gain steps in the receiver are thus specific to the wireless application being targeted and dependent on the dynamic range and resolution of the ADC. In direct-conversion and low-IF receivers, the gain is distributed between the RF front-end and the baseband. The RF front-end, predominantly the LNA, can be designed to have a variable gain [34], [58], [64], [65], but it is often more feasible to



realize VGAs at the baseband, especially when small gain steps are needed. The analog baseband circuit may consist of cascaded filters and VGAs, as shown in Fig. 2.5. Another possibility is to merge the baseband filter with the VGA, at least partially. On the basis of this discussion, it should be apparent that the system-level design has a great impact not only on the overall performance but also on the total power consumption and die area of the entire single-chip radio receiver. The minimization of the power dissipation is an important design parameter in analog baseband filter design. However, the overall performance of the receiver obtained with a certain total power consumption is the figure of merit that matters.

## 2.4 Wireless communication systems

This section outlines three different radio systems. In the first sub-section, the third-generation telecommunication system UTRA FDD WCDMA is introduced. The remaining two sub-sections give an overview of wireless short-range communications. The emphasis is on the WiMedia UWB and 60-GHz systems. All the circuits that were implemented and presented in this thesis are intended for the systems being discussed. The WiMedia UWB system was one of the overriding motivators for this thesis.

### 2.4.1 UTRA FDD WCDMA

Third-generation (3G) mobile communication systems have been developed since the late 1980s to offer enhanced data rates and capacity compared to second-generation (2G) systems, such as GSM, PDC, and IS-95. The 3G process, which originally targeted a single global *International Mobile Telecommunications-2000 (IMT-2000)* air interface operating around 2 GHz, was started by the International Telecommunications Union (ITU) [66], [67]. In Europe, the European Telecommunications Standards Institute (ETSI) was initially responsible for the 3G standardization activities under the name *Universal Mobile Telecommunications System (UMTS)*. In 1998, however, the *Third Generation Partnership Project (3GPP)* [68] was formed. The 3GPP partners, including ETSI, agreed on joint efforts for the standardization of *Universal Terrestrial Radio Access (UTRA)*, which originally stood for *UMTS Terrestrial Radio Access* within ETSI [66]. In any case, UMTS has become an umbrella term for the third-generation radio technologies developed within the 3GPP [68]. UTRA has both a *Frequency Division Duplex (FDD)* mode and a *Time Division Duplex (TDD)* mode. The 3GPP's UTRA FDD mode is based on wideband code division multiple access (WCDMA) third-generation radio technology [66],

[69]. The UTRA FDD WCDMA air interface standard was specified in Release 99 (released in 2000) and Release 4 (released in 2003) of the 3GPP's specifications. It is also part of the ITU IMT-2000 family [66], [68], [69]. During the past decade, UTRA FDD WCDMA has emerged as the leading worldwide 3G system technology today [70].

WCDMA is a wideband Direct-Sequence Code Division Multiple Access (DS-SS) system in which user information bits are spread over a wide bandwidth. The spreading is performed by multiplying the user data by quasi-random bits, called chips [66]. The chip rate is 3.84 Mcps, leading to a signal bandwidth of 3.84 MHz, which is wider than the second-generation systems. The nominal channel spacing is 5 MHz [71]. Because of the FDD mode of operation, different frequency bands are allocated for the uplink (from the mobile to the base station) and downlink (from the base station to the mobile) in the UTRA FDD WCDMA standard. Consequently, the transmitter and receiver can be on simultaneously and operate continuously. According to the latest version (V9.3.0, Mar. 2010) of the 3GPP's technical specification 25.101, UTRA FDD WCDMA is defined to operate in the paired bands presented in Table 2.1 [71]. However, the number of operating bands has increased continuously.

Table 2.1. Paired bands for UTRA FDD WCDMA according to the latest version (V9.3.0, Mar. 2010) of the 3GPP's technical specification 25.101 [71].

<b>Operating Band</b>	<b>Uplink</b>	<b>Downlink</b>
I	1920 - 1980 MHz	2110 - 2170 MHz
II	1850 - 1910 MHz	1930 - 1990 MHz
III	1710 - 1785 MHz	1805 - 1880 MHz
IV	1710 - 1755 MHz	2110 - 2155 MHz
V	824 - 849 MHz	869 - 894 MHz
VI	830 - 840 MHz	875 - 885 MHz
VII	2500 - 2570 MHz	2620 - 2690 MHz
VIII	880 - 915 MHz	925 - 960 MHz
IX	1749.9 - 1784.9 MHz	1844.9 - 1879.9 MHz
X	1710 - 1770 MHz	2110 - 2170 MHz
XI	1427.9 - 1447.9 MHz	1475.9 - 1495.9 MHz
XII	698 - 716 MHz	728 - 746 MHz
XIII	777 - 787 MHz	746 - 756 MHz
XIV	788 - 798 MHz	758 - 768 MHz
XV	Reserved	Reserved
XVI	Reserved	Reserved
XVII	Reserved	Reserved
XVIII	Reserved	Reserved
XIX	830 - 845 MHz	875 - 890 MHz
XX	832 - 862 MHz	791 - 821 MHz
XXI	1447.9 - 1462.9 MHz	1495.9 - 1510.9 MHz

Originally, UTRA FDD WCDMA was designed to support data rates up to 2 Mbps. Later on, *High Speed Packet Access (HSPA)*, the first evolution of WCDMA specified in 3GPP's Releases 5 (for downlinks in 2003) and 6 (for uplinks in 2004), boosted the downlink and uplink data rates to 14 Mbps and 5.8 Mbps, respectively. Moreover, 3GPP's Release 7 (2007) introduced HSPA+ (i.e. Enhanced HSPA), capable of peak downlink and uplink throughputs up to 28 Mbps and 11 Mbps, respectively. In addition to the further enhancement for HSPA+, Release 8 (2008) introduced LTE, targeting downlink data rates from 10 Mbps up to over 100 Mbps and uplink data rates from 5 Mbps up to 50 Mbps. However, LTE differs considerably from the original WCDMA concept and should therefore be considered to be a new air interface system, moving strongly towards fourth-generation (4G) mobile communications.

#### **2.4.2 WiMedia UWB**

The history of ultrawideband (UWB) communications dates back to the 1960s. The operation of early systems was based on sending and receiving very short information-bearing RF pulses. The term 'ultrawideband' was not applied to corresponding systems until the end of the 1980s [72], [73]. In this millennium, UWB communication systems have gained renewed attention. In February 2002, the Federal Communications Commission (FCC) in the United States allocated a 7500-MHz wide spectrum, from 3.1 GHz to 10.6 GHz, for the unlicensed use of UWB communication devices [74], [75]. The International ECMA-368 standard, released in December 2005 and approved as the ISO/IEC 26970 standard in 2007, defines the same frequency range for the use of UWB devices [76].

The spectrum allocation for UWB is unique because the band overlaps with other existing communication systems, in addition to its extremely wide bandwidth. The overlapping services and those located nearby are presented in e.g. [56], [77]-[80]. To prevent harmful interferences from degrading the operation of coexisting services in the same frequency range, the transmission power levels of UWB devices are limited by the FCC ruling. At the same time, the transmission power of, for example, cellular phones and Wi-Fi systems sharing the same band of operation is much higher than that of UWB transmitters. Thus, UWB receivers are subject to considerable interference. UWB devices are required to occupy in excess of 500 MHz of bandwidth in the allocated 7500-MHz band. Reliable low-power data transmission in the vicinity of other services can be accomplished by spreading the information that is transmitted over a large bandwidth.

The UWB technology enables high-data-rate wireless communication to take place over short ranges with reduced power consumption. It can be utilized, for instance, in personal area networks (PANs) and in radar, imaging, and positioning systems. The suitability for a wide variety of new wireless applications has raised a great deal of research interest both in industry and in academia since the FCC spectrum allocation in 2002. The development of UWB radios has been concentrated mainly on low-size, low-cost CMOS IC implementations [54], [64], [81]-[83]. The research and development of the wideband gm-C low-pass filters described in this book is related to the same interest. The worldwide activity thus initiated has led to a number of technical approaches proposing how to utilize the UWB spectrum. The International ECMA-368 standard for high-speed UWB wireless connectivity is based on WiMedia's UWB technology, which divides the UWB spectrum into 14 sub-bands that each have a bandwidth of 528 MHz. Within each sub-band, an orthogonal frequency division multiplexing (OFDM) modulation scheme is used to transmit the information. The sub-bands are arranged into six band groups (BGs) as shown in Fig. 2.6 and fast frequency hopping between the sub-bands is utilized inside one band group at a time [84]. As a result of the Multiband OFDM (MB-OFDM) technique, high bit rate transmission rates, from 53.3 Mb/s up to 480 Mb/s over approximately 1 to 10 meters, high spectral efficiency, and the ability to deal with narrow-band interferers are achieved. In order to give an overview, the data rate and operating distance of the WiMedia UWB technology is compared with Wi-Fi, Bluetooth, and ZigBee systems that currently exist in Table 2.2. In March 2009, the WiMedia Alliance transferred all the specifications to the Bluetooth Special Interest Group (SIG), Wireless Universal Serial Bus (USB) Promoter Group, and USB Implementers Forum. At the moment, it seems likely that Certified Wireless USB will be based on the WiMedia UWB common radio platform. It is also worth mentioning that another alternative approach, the direct-sequence impulse radio technique (DS-UWB), is capable of providing similar throughputs to WiMedia UWB [85]. The UWB technology can thus be expected to have an interesting future.

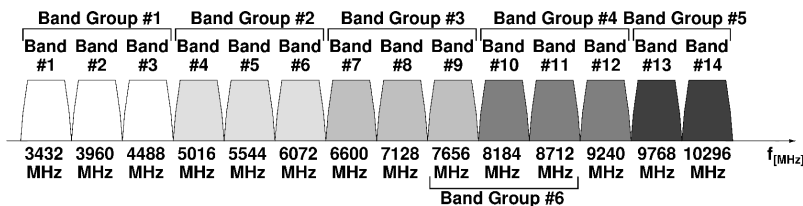


Figure 2.6. WiMedia UWB band group allocation.

Table 2.2. Comparison of WiMedia UWB technology with Wi-Fi, Bluetooth, and ZigBee systems that currently exist [25], [86]-[88].

	IEEE 802.11 Wi-Fi	Bluetooth (versions 1.1 - 2.1)	IEEE 802.15.4 ZigBee	WiMedia UWB
<b>Frequency range</b>	2.4 GHz (802.11b,g) 5 GHz (802.11a)	2.4 GHz	868 MHz (Europe) 915 MHz (America) 2.4 GHz (global)	3.1 - 10.6 GHz
<b>Channel bandwidth</b>	16.25 MHz (802.11a) 22 MHz (802.11b) 16.5-22 MHz (802.11g)	1 MHz	600 kHz (868-MHz band) 1.2 MHz (915-MHz band)* 2 MHz (2.4-GHz band)**	528 MHz
<b>Data rate</b>	up to 11 Mb/s (802.11b) up to 54 Mb/s (802.11a,g)	1 - 3 Mb/s	20 kb/s 40 kb/s 250 kb/s	53.3 - 480 Mb/s
<b>Operating distance</b>	100 m (802.11b,g) 50 m (802.11a)	6 - 100 m	10 - 100 m	1 - 10 m

\*) 2-MHz channel spacing

\*\*) 5-MHz channel spacing

### 2.4.3 60-GHz radio systems

During the past decade, an increased effort has been put into developing 60-GHz radio systems and CMOS integrated circuits operating at millimeter-wave frequencies [89]-[98]. One of the main reasons for the excitement is an extremely wide bandwidth, up to 7 GHz, available worldwide around 60 GHz. In 1995, the Federal Communications Commission (FCC) in the United States made the 59-64-GHz band (millimeter wave band) available for use by unlicensed devices [99] and later expanded the band to cover 57-64 GHz in 2001 [100]. In July 2009, the European Telecommunications Standards Institute (ETSI) published an updated version of a Harmonized European Standard [101]. The new standard covers microwave links that operate in the frequency bands 57-59 GHz, 59-64 GHz, 64-66 GHz, 71-76 GHz, and 81-86 GHz. Moreover, regulation activities for the 60-GHz band have also been performed in Canada (57-64 GHz), Japan (59-66 GHz), Australia (59.4-62.9 GHz), and Korea (57-64 GHz) [102].

The large bandwidth offers a high transfer capacity and thus makes gigabit-rate or even multi-gigabit-rate wireless data transmission achievable at 60 GHz with a variety of modulation and coding schemes. In addition, the 60-GHz band is a much less congested spectrum compared to the one allocated for the use of UWB devices at 3.1-10.6 GHz, leading to lower interference from coexisting systems and less restricted transmission power levels. The latter can be used to compensate for the higher propagation loss at the 60-GHz frequency range. While the propagation loss limits the practicable operating range of 60-GHz radio systems, it also increases frequency reuse in an indoor dense local network, reduces co-channel interference, and improves the safety of a secure short-range point-to-point link by providing additional spatial isolation [103], [104]. Because of its suitability for short-range high throughput wireless connectivity, the

60-GHz technology can be utilized in a host of different applications, including high-speed WPANs, the next evolution version of a higher-data-rate WLAN operating at a shorter range, wireless high-density (HD) video streaming, short- or medium-range point-to-point links, and vehicular radar applications.

Another driver behind the emergence of interest in 60-GHz communication systems is the significant advance in CMOS process technologies. Modern nanoscale CMOS technologies provide transistors which are capable of operating efficiently up to 100 GHz and beyond owing to their high unity current gain frequency and high maximum frequency of oscillation [105], [106]. As a result of this technological development, it has become feasible to realize millimeter-wave ICs in a standard CMOS process, which makes possible a high level of integration and reduces the cost of high-volume production. Therefore, the efficient implementation of a complete single-chip 60-GHz radio with an integrated DSP is an attractive alternative for mass market applications.

The great potential of 60-GHz radio systems has led to a lot of standardization activity. In addition to the WirelessHD high-speed radio communication standard (specified in January 2008) and the international ECMA-387 standard (released in December 2008 and approved as the ISO/IEC 13156 standard in 2009), there are two IEEE task groups concentrating on the 60-GHz frequency band: task group 3c operating under IEEE 802.15 WPAN and task group ad operating under IEEE 802.11 [107]-[111].

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## 3 Integrated continuous-time low-pass filters

Integrated continuous-time filters are most often constructed from inverting and non-inverting lossy and lossless integrators [1]-[5]. In addition, summers or related circuits are typically needed to add two or more signals together, thereby completing the structure of the filter. These integrator-based active filters are suitable for integration at the baseband since, contrary to their passive LC ladder counterparts, they do not employ passive inductors. As explained in more detail in, for example, [3], [6], [7], at (low) baseband frequencies, integrated passive inductors easily occupy an impractically large die area. Moreover, their Q-factor tends to be low, preventing the implementation of highly selective passive filters [8]. In wideband applications, in which the low-pass filters to be designed are required to have, let us say, a bandwidth of over 100 MHz, the integration of passive LC ladder filters may be considered [9]. However, this thesis addresses the design and implementation of integrator-based active continuous-time low-pass filters.

Filter prototype selection and synthesis are left for Chapter 4. Instead, the first subject of this chapter is to study the non-idealities of an integrator and their effect on the filter frequency response. Next, the most important circuit techniques used to realize these filter building blocks on a silicon chip are briefly introduced. Several different circuit techniques to implement analog baseband filters exist. The most popular ones are based on operational amplifiers, such as the opamp-RC technique, and transconductors, the gm-C technique for instance. Both these techniques have been utilized in the experimental circuits presented in this thesis and hence, they are discussed in more detail in this chapter than others are. Finally, for the sake of completeness, the fundamental principle of the automatic on-chip tuning of integrator time constants is described. The description is given at the block diagram level since the design and implementation of automatic tuning circuits lie outside the scope of the investigation in this work.



### 3.1 Non-ideal integrator

In this section the effect of integrator non-idealities on the frequency response of an active filter is examined. An understanding of the relationship between the integrator non-idealities and the filter frequency response accuracy is essential in this work, as will be seen in Chapter 4. This section is based on material that others have published earlier [1]-[3], [6], [7], [10]-[12].

An ideal integrator has an infinite DC gain. The dominant pole thus lies at a zero frequency (i.e. at DC) but there are no other poles or finite-frequency zeros. The transfer function of an ideal non-inverting integrator can be expressed as

$$H_{\text{int}}(s) = \frac{\omega_{\text{int}}}{s} . \quad (3.1)$$

It can be concluded from (3.1) that the magnitude response rolls off unrestrictedly at -6 dB/octave (or -20 dB/decade) from DC to an infinite frequency and has a value of one (i.e. 0 dB) at the integrator unity-gain frequency  $\omega_{\text{int}}$ . Moreover, the phase response is constant,  $-\pi/2$  radians, over all frequencies. These ideal characteristics are illustrated in Fig. 3.1 with dashed lines. It should be noted that the integrator unity-gain frequency  $\omega_{\text{int}}$  is simply the inverse of the time constant  $\tau_{\text{int}}$  of the integrator.

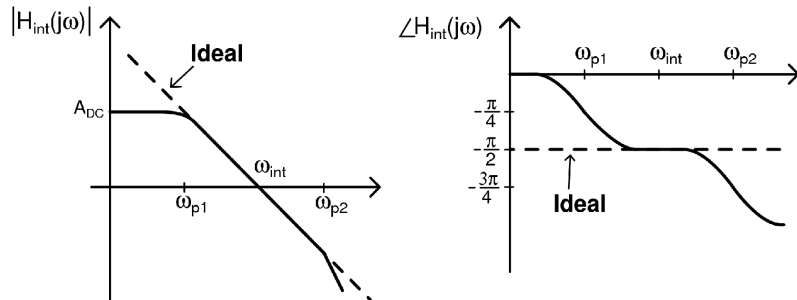


Fig. 3.1 Magnitude and phase responses of an ideal (dashed line) and a real (solid line) integrator.

In practice, however, a real integrator has a finite DC gain,  $A_{DC}$ . Therefore, the low-frequency dominant pole is located at a non-zero frequency of  $\omega_{p1} = \omega_{\text{int}}/A_{DC}$ . In addition, a real integrator may have one or more high-frequency non-dominant poles. In this study, a single non-dominant pole is assumed to appear at  $\omega_{p2}$ . The effects of the finite DC gain and the dominant and non-dominant poles on the integrator magnitude and phase

responses are shown in Fig. 3.1 with solid lines. The transfer function of a real integrator can be written as

$$H_{\text{int}}(s) = \frac{A_{DC}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}. \quad (3.2)$$

The losses (i.e. non-idealities) of capacitors and inductors in a passive LC ladder network can be determined by means of capacitor and inductor quality factors (Q-factors), respectively. The quality factor is a figure of merit that is often used for passive, ideally lossless, reactive elements (i.e. L and C), fundamentally defining how much energy is stored in the element relative to how much energy is dissipated [13]-[15]. The capacitor Q-factor will be used in the analysis presented in Chapter 4. In a similar fashion, the integrator quality factor can be defined as [1], [3], [6], [7], [10]-[12]

$$Q_{\text{int}}(\omega) = -\frac{\text{Im}\{H_{\text{int}}(j\omega)\}}{\text{Re}\{H_{\text{int}}(j\omega)\}} = \frac{\text{Im}\left\{\frac{1}{H_{\text{int}}(j\omega)}\right\}}{\text{Re}\left\{\frac{1}{H_{\text{int}}(j\omega)}\right\}}. \quad (3.3)$$

When (3.2) is substituted into (3.3) and it is assumed that the non-dominant pole occurs at a much higher frequency compared to the low-frequency dominant pole (i.e.  $\omega_{p2} \gg \omega_{p1}$ ), the inverse of the quality factor of a real integrator becomes

$$\frac{1}{Q_{\text{int}}(\omega)} \approx \frac{\omega_{\text{int}}}{\omega A_{DC}} - \frac{\omega}{\omega_{p2}}. \quad (3.4)$$

As can be seen in (3.4), the integrator Q-factor is a frequency-dependent quantity. The unity-gain frequencies of the integrators forming an active filter are close to the passband edge of the filter transfer function. The filter passband edge is usually the most sensitive frequency in the filter transfer function [3], [7], [12]. Therefore, the Q-factor of an integrator is of importance, particularly at the integrator unity-gain frequency  $\omega_{\text{int}}$ .

Let us examine the effect of the finite DC gain and, on the other hand, the effect of the high-frequency non-dominant pole on the integrator Q-factor at  $\omega_{\text{int}}$  with two separate study cases. If, first, the non-dominant pole at  $\omega_{p2}$  is moved to infinity and only the finite DC gain of the integrator is of interest, it follows from (3.4) that

$$Q_{\text{int}}(\omega_{\text{int}}) \approx A_{DC}. \quad (3.5)$$

On the basis of (3.5), two conclusions can be drawn. Since an ideal integrator has an infinitely high DC gain, the Q-factor of an ideal integrator becomes infinite. A finite DC gain of a real integrator leads to a finite, positive integrator Q-factor value. In this case, the integrator can be said to be a *lossy integrator*. The correspondence with a lossy capacitor or a lossy inductor that has a finite positive capacitor or inductor Q-factor is obvious and this observation will be used in the filter synthesis presented in Chapter 4. If the integrator is then assumed to have an infinitely high DC gain and only the effect of the non-dominant pole is taken into account, (3.4) leads to

$$Q_{\text{int}}(\omega_{\text{int}}) \approx -\frac{\omega_{p2}}{\omega_{\text{int}}}. \quad (3.6)$$

In (3.6), the integrator Q-factor is negative. This is a result that is not encountered in a passive LC ladder network. Clearly, on the basis of (3.5) and (3.6), the quality factor of an active integrator is a function of both the DC gain and the non-dominant pole of the integrator. More importantly, the two non-idealities under consideration result in Q-factor values with opposite signs. They can thus be expected to have an opposite effect on the filter magnitude response and the behavior of the phase, as will be studied next.

The active filter implementations presented in this thesis are based on signal flow graph (SFG) LC ladder simulations, as will be further discussed in Chapter 4. In such active filters, the quality factors of the integrators simulating the operation of the desired LC ladder filter have an effect on the filter magnitude response accuracy, basically in much the same way as the inductor and capacitor Q-factors do in the corresponding LC ladder filter. Therefore, when examining the effect of the integrator Q-factor on the filter magnitude response accuracy, it is reasonable in this work, and in many other cases, to utilize the following study from the literature. The relative magnitude error in the transfer function of an LC ladder filter can be represented as [3], [12]:

$$\frac{\Delta M(\omega)}{M(\omega)} = -\frac{1}{2} \left( \frac{1}{Q_L} + \frac{1}{Q_C} \right) \omega \tau(\omega) + \frac{1}{4} \left( \frac{1}{Q_L} - \frac{1}{Q_C} \right) \text{Im}\{\rho_{\text{in}}(j\omega) + \rho_{\text{out}}(j\omega)\}, \quad (3.7)$$

where  $Q_L$  and  $Q_C$  are the inductor and capacitor Q-factors, respectively,  $\rho_{\text{in}}$  and  $\rho_{\text{out}}$  are the reflection coefficients at the input and output port, respectively, and  $\tau(\omega)$  is the filter group delay. It should be noted that in

this study all inductors and, correspondingly, all capacitors in the LC ladder filter are assumed to have an equal Q-factor. If both  $\omega\alpha(\omega) \gg 1$  and  $|\rho_{in} + \rho_{out}| \ll 1$  are satisfied over the passband of the LC ladder filter, the first term in (3.7) becomes dominant. Hence, (3.7) can be approximated as [3], [12]

$$\frac{\Delta M(\omega)}{M(\omega)} \approx -\frac{1}{2} \left( \frac{1}{Q_L} + \frac{1}{Q_C} \right) \omega\tau(\omega). \quad (3.8)$$

When first (3.5) and then (3.6) are substituted into (3.8), it can be concluded that the finite DC gain of the integrators causes *gain drooping*, while the high-frequency non-dominant pole of the integrators causes *gain peaking* in the vicinity of the filter passband edge frequency.

The phase error of the integrator (i.e. the deviation of the integrator phase from its ideal value of  $-\pi/2$  radians) and the Q-factor of the integrator have the relation [3]

$$\Delta\phi_{int}(\omega) = \tan^{-1} \left[ \frac{1}{Q_{int}(\omega)} \right]. \quad (3.9)$$

Thus, the integrator phase can be written as [3], [6], [7], [11]

$$\phi_{int}(\omega) = -\frac{\pi}{2} + \Delta\phi_{int}(\omega) = -\frac{\pi}{2} + \tan^{-1} \left[ \frac{1}{Q_{int}(\omega)} \right]. \quad (3.10)$$

It can be noted from (3.10) that with finite positive integrator Q-factor values the phase of the integrator is higher than  $-\pi/2$  radians. This is called *phase lead* and it corresponds to the gain drooping near the filter passband edge frequency (i.e. finite integrator DC gain). Conversely, with finite, negative integrator Q-factor values, the phase is lower than  $-\pi/2$ . This is called *phase lag* and it corresponds to the gain peaking at frequencies close to the filter passband edge (i.e. integrator with a high-frequency non-dominant pole).

In addition to high-frequency non-dominant (left half-plane) poles, a non-ideal integrator may have parasitic positive (i.e. right half-plane) zeros, for example, as a result of the parasitic Miller capacitances of the active devices forming the integrator. A parasitic positive zero affects the integrator phase response and thus, the integrator Q-factor in a similar manner as a high-frequency non-dominant (left half-plane) pole. Not only do high-frequency non-dominant poles and parasitic zeros cause the integrator Q-factor to deteriorate, thereby affecting the filter frequency response, but the former will also add extra terms into the denominator and

the latter into the nominator of the filter transfer function. The extra terms will change the desired passband response of the filter if the poles and zeros behind the terms are not located at much higher frequencies compared to the filter passband edge frequency. Hence, parasitic poles and zeros must be taken into consideration, especially when wideband filters are being designed.

So far we have concentrated on the integrator non-idealities related to the finite DC gain and the high-frequency non-dominant poles and parasitic zeros. However, the precision of the unity-gain frequencies or the time constants ( $\omega_{nt} = 1 / \tau_{nt}$ ) of the integrators forming an active filter has a great impact on the filter frequency response accuracy. Depending on the circuit technique used to realize the filter, the integrator time constants are implemented, for example, with  $RC$  products or  $C/gm$  ratios, as will be studied in the following sections. In integrated continuous-time filter circuits, the resistance, capacitance, and transconductance ( $gm$ ) values alter in ways that are unrelated to each other as a result of PVT variations. This leads to uncertainty in the fabricated time constants when they are determined by the absolute values of the components. This is the case in  $RC$  products and  $C/gm$  ratios. As a comparison, in discrete-time SC filters, the time constants are based on an accurate clock frequency and capacitance ratios instead of the absolute values of components. Hence, in those filters, the challenge is related to the high-quality clock signal that is required. In continuous-time filters, some kind of on-chip tuning is obviously needed in order to accurately set the integrator time constants to their designed values and thus, avoid the frequency shift or even the deterioration of the filter frequency response. A presentation on how inaccurate time constants may shift the filter frequency response or cause it to deteriorate is given, for instance, in [7]. Correspondingly, in this thesis, Section 3.5 is devoted to the system-level discussion of automatic on-chip tuning circuits.

It can be concluded from the study presented above that the integrator Q-factor representing the integrator non-idealities is a useful, although theoretical, parameter in the design of active filters. The concepts of the *lossy integrator* and the *integrator quality factor* will play important roles in the filter synthesis presented in Chapter 4. A more practical issue in continuous-time filter design is related to the implementation and the precision of the time constants of the filter integrators.

### 3.2 Opamp-RC technique

The operational amplifier RC (opamp-RC) technique, sometimes called the active-RC technique, is based on the Miller integrator shown in Fig. 3.2a

[3], [10], [16]-[18]. It is one of the most traditional techniques, dating back to the 1950s [17], [19], to realize active filters by using transistors or amplifier circuits. The input voltage is converted into a current with the combination of the input resistor  $R_i$  and the virtual ground at the negative input node of the opamp. Ideally, no current will flow into the opamp input terminals. Instead, the converted current signal flows into the integrating capacitor  $C_i$  placed in the negative feedback path around the opamp. As a result of the signal integration in the feedback capacitor  $C_i$ , there will be a voltage signal present at the circuit output. The transfer function of a lossless, inverting integrator can be expressed as

$$H_{\text{int}}(s) = -\frac{1}{sR_iC_i}. \quad (3.11)$$

A lossy integrator is constructed by connecting an additional resistor in parallel with the feedback capacitor  $C_i$ . Correspondingly, a summing integrator is formed by adding one or more resistors in parallel with the input resistor  $R_i$ . Neither of these modifications requires additional active elements. In a single-ended configuration, an additional inverter is needed to implement a non-inverting integrator. However, in practice, integrated filters are realized as balanced structures. A balanced non-inverting integrator can be implemented without an additional inverter simply by cross-coupling the positive and negative signal wires.

As can be seen in (3.11), the time constant of an opamp-RC integrator is  $\tau_{\text{int}} = R_iC_i$ . When process variations and a typical temperature range, let us say from  $-25^\circ\text{C}$  to  $+70^\circ\text{C}$ , are taken into account, the fabricated RC time constant may vary by  $\pm 50\%$  or even more [6], [11], [12], [20]. Therefore, the time constants must be tuned somehow. In integrated opamp-RC filters, time-constant tuning can be accomplished with digitally controlled switched-capacitor or switched-resistor matrices [20], [21]. Depending on the configuration of the binary-weighted passive elements (i.e. capacitors or resistors) in the matrices, the tuning scheme may be divided into two basic categories. These include so-called direct and inverse quantization schemes, in which the arrays of the binary-weighted elements are implemented differently [21]. The former can be associated with matrices consisting of a parallel combination of capacitors or a series combination of resistors. Correspondingly, the latter can be associated with matrices incorporating a series network of capacitors or a parallel network of resistors. In practice, capacitors connected in parallel and resistors connected in series result in a smaller die area compared to their counterparts. Capacitor matrices with parallel elements, depicted in Fig. 3.2b, are the ones that are used most often, including the experimental opamp-RC filter circuits of this work, as

presented in Chapter 5. This is because the finite (i.e. non-zero) on-resistance of the MOS switches does not directly affect the element values and hence, shift the time-constant value in capacitor matrices, which is the case in resistor matrices. As an indirect second-order effect, the on-resistance of a switch connected in series with a capacitor, as shown in Fig. 3.2b, produces a left half-plane (LHP) zero in the transfer function of the integrator. However, this unavoidable zero can usually be designed to occur at a much higher frequency compared to the filter passband edge frequency, thereby having a negligible effect on the filter frequency response. Alternatively, the LHP zero is sometimes used to compensate for the finite (i.e. limited) unity-gain bandwidth of the opamp in opamp-RC filters [3], [6]. There is also another reason for the preference for the use of capacitor matrices. In [20] it is shown that for the same time-constant setting accuracy, higher filter passband edge frequencies can be realized by means of capacitor matrices consisting of parallel elements when compared to series resistor matrices. The digital control word for the matrices is typically generated on a chip by some kind of calibration circuit, as will be discussed in Section 3.5.

One of the main advantages of the opamp-RC technique is that it enables a rail-to-rail signal swing to take place in the filter integrators. Correspondingly, the dominant noise contribution usually arises from the resistors, since the noise of the opamps can be designed to be low [6], [8], [22], [23]. The resistors in opamp-RC filters tend to be less noisy compared, for example, to the transconductors of gm-C filters, which are typically constructed from several devices [8]. Moreover, the opamp must be capable of driving a resistive load presented by the other opamp-RC integrators which are connected to its output. For that reason, a two-stage opamp is ordinarily employed. A two-stage opamp can be designed to have a high open-loop DC gain, typically, 60 dB at a minimum. On the basis of the feedback theory, the high open-loop DC gain of an opamp operating in a closed-loop connection in an integrator results in a high loop gain:

$$\beta A_{opamp}(s) = \beta \frac{A_{DC,opamp}}{1 + \left( \frac{s}{\omega_{p1,opamp}} \right)} = \beta \frac{A_{DC,opamp}}{1 + \left[ \frac{s}{(\omega_{GBW} / A_{DC,opamp})} \right]}, \quad (3.12)$$

where the term  $\beta A_{opamp}(s)$  is the loop gain,  $\beta$  is the feedback factor,  $A_{opamp}(s)$  is the opamp open-loop gain,  $A_{DC,opamp}$  is the opamp open-loop DC gain,  $\omega_{p1,opamp}$  is the dominant pole frequency of the opamp, and  $\omega_{GBW}$  is the unity-gain bandwidth of the opamp. It should be pointed out here that throughout this thesis the opamp GBW and the opamp unity-gain

bandwidth are approximated as being equal. The former is preferred in order to avoid confusing the latter with the integrator unity-gain bandwidth. In any case, combining the high loop gain of the integrators with the large signal handling capability, an opamp-RC filter can be designed to have excellent linearity and, thus, a high dynamic range, even with low supply voltages. As an example, a fifth-order active-RC filter using a supply as low as 0.5 V is reported in [24]. Considering the frequency dependency of the loop gain, it can be concluded from (3.12) that the opamp needs to have a high GBW concurrently with the high open-loop DC gain in order to achieve a high loop gain and hence, high linearity over a wide bandwidth.

The opamp-RC technique is insensitive to parasitic capacitances as far as the opamp can be considered to be an ideal voltage-controlled voltage source. The parasitic capacitances arising at the output and the negative input of the opamp are not directly connected in parallel with the integrating capacitor placed in the feedback path. Moreover, indirect second-order effects are negligible when an ideal opamp is assumed because the parasitic capacitances either occur at the virtual ground of the opamp input or are driven by a voltage source at the opamp output. In practice, because of the limited open-loop DC gain and unity-gain bandwidth and the non-zero output resistance of the opamp, parasitic capacitances potentially degrade the integrator Q-factors, thereby having a small indirect effect on the filter frequency response, as studied analytically in [6]. The Q-factor of an opamp-RC integrator is considered in more detail in the following paragraph and in Chapter 5.

The integrator DC gain and  $\omega_{p2}$  used in (3.4) are determined by the opamp open-loop DC gain and the opamp unity-gain bandwidth  $\omega_{GBW}$ , respectively. The Q-factor of an opamp-RC integrator usually becomes limited by the opamp GBW, especially in wideband filter designs. This is because in practice it is challenging to design an opamp that has both a high open-loop DC gain and a large GBW simultaneously, but the former is relatively easy to obtain with an opamp. In addition, in high-Q filter designs, the opamp may be required to have a GBW as much as one hundred times larger compared to the bandwidth of the filter [22], [25]. Therefore, the opamp-RC technique is most often used in integrated filters targeted for low- or moderate-speed applications.

In a balanced opamp-RC integrator, the resistors can be replaced with triode-region MOSFET transistors. The modified construction is called the MOSFET-C technique [26], [27]. In this approach, the resistance values of the triode-region transistors can be continuously tuned by means of a



continuous gate control voltage, as opposed to the discrete values of capacitor or resistor matrices.

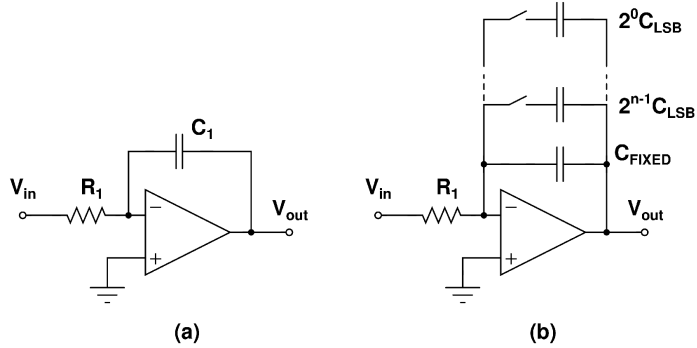


Figure 3.2. (a) Lossless inverting opamp-RC integrator; (b) time-constant tuning using a capacitor matrix with parallel elements.

### 3.3 Gm-C technique

A gm-C integrator consists of a transconductor and a capacitor, as shown in Fig. 3.3a [2], [7], [17], [28]-[30]. The circuit has several differences compared to its opamp-RC counterpart. The most apparent one is that the gm-C integrator is based on an open-loop structure. In a gm-C integrator, the input voltage is first converted into a current by the transconductor. The transconductor is thus a voltage-controlled current source characterized by its transconductance value  $gm$ . The converted current signal is then driven into the integrating capacitor  $C_i$  at the transconductor output, resulting in an output voltage. The transfer function of a lossless inverting integrator can be written as

$$H_{\text{int}}(s) = -\frac{gm}{sC_1}. \quad (3.13)$$

A lossy integrator is formed by connecting an additional transconductor to the integrator output, as shown in Fig. 3.3b. Similarly, additional transconductors placed in parallel with the original transconductor (with their outputs connected together) are needed to construct a summing integrator. As a comparison, instead of adding extra active elements, both of these modifications can be realized with additional passive resistors in the opamp-RC technique, as discussed in the previous section. A balanced gm-C integrator may use either grounded or floating capacitors at the transconductor output, as shown in Fig. 3.4. The latter requires less capacitance and thus, less silicon area, especially in the case of metal-metal

capacitors. The grounded capacitors can be realized with MOS capacitors (based on MOSFET gate capacitance) as well [31]. Since a MOS transistor pair can operate as a balanced transconductor, the gm-C technique enables an (compact) all-CMOS filter implementation to be used when combining such a balanced transconductor with MOS capacitors [32], [33].

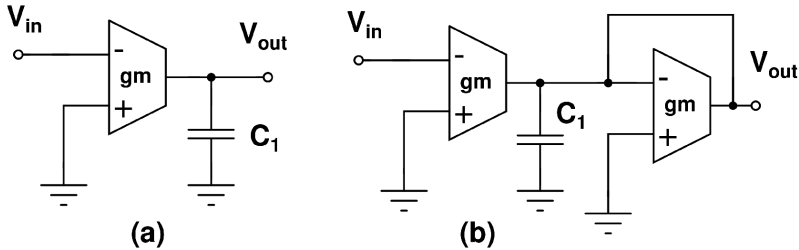


Figure 3.3. (a) Lossless and (b) lossy inverting gm-C integrator.

On the basis of (3.13), the time constant of a gm-C integrator is  $\tau_{int} = C_i/gm$ . Hence, in gm-C filters, the time-constant tuning is either performed with digitally controlled switched capacitor matrices or by varying the  $gm$  of the transconductors [8], [31]. The latter is a more conventional approach. Transconductance tuning can be accomplished, for example, by adjusting the DC bias current of the transconductor or by switching on and off parallel connected unit transconductors [5]-[7], [11], [12], [17], [32], [34].

The previous section showed that the closed-loop performance of an opamp-RC integrator is ideally almost independent of the behavior of the opamp. In contrast, the performance of a gm-C integrator depends directly on the transconductor characteristics, including the integrator transfer function, noise, and linearity. The transfer function of a gm-C integrator is determined by the transconductor  $gm$ , as can be seen in (3.13). Therefore, an accurate  $gm$  value is important for the filter frequency response. The linearity and the dynamic range of gm-C filters tend to be worse compared to their opamp-RC counterparts. This is not only due to the potentially higher noise contribution of the transconductors in the former compared to the resistors in the latter, but is also related to the open-loop operation of the gm-C integrators (i.e. the absence of the feedback) in addition to the non-linear behavior of the  $gm$  of the transconductors. Typically, a transconductor circuit is capable of providing an acceptable linear voltage-current conversion within a limited range of input signal amplitudes. In CMOS implementations, the potentially high threshold voltage  $V_{TH}$  of the input transistors and the low supply voltage, which together reduce the transconductor overdrive voltage ( $V_{GS} - V_{TH}$ ), limit the signal swing at the transconductor input. Correspondingly, the output signal swing becomes

reduced if cascode transistors are used, as they often are, to enhance the transconductor DC gain.

The parasitic input and output capacitances of the transconductors, including the parasitic wiring capacitances, must be taken into account in gm-C filter design. This is because, in contrast to the opamp-RC technique, parasitic capacitances are directly connected in parallel with the integrating capacitors of the filter integrators, thereby increasing the desired capacitance value of the integrating capacitors. The shifting of the time constants as a result of parasitic capacitances is compensated by reducing the capacitance value of the original integrating capacitors accordingly. Since parasitic capacitances tend to be non-linear, there is uncertainty about their value, and they do not match well with the integrating capacitors as a function of PVT variations, it is desirable to try to keep the ratio between the parasitic capacitances and the capacitance value of the original integrating capacitor as low as possible at each filter node. In addition, it is important to try to balance this ratio between each filter node. As an example, according to [5], a 20% ratio can be considered to be tolerable. However, for instance in [35], a viable gm-C filter implementation in which even more parasitic capacitance was allowed has been reported. In wideband gm-C filters whose coefficients (i.e. capacitance values) tend to be initially low, parasitic capacitances potentially require a lot of design effort, as will be studied in more detail in Chapter 6. One alternative way to obtain a parasitic-insensitive integrator is to load the transconductor with the virtual ground of a feedback-connected operational transconductance amplifier (OTA) instead of a passive integrating capacitor [5], [6], [31], [36]-[38]. This type of realization can be called a gm-OTA-C technique.

The DC gain of a transconductor is defined as the ratio of the transconductance and output conductance,  $gm / g_{out}$ , and it determines the integrator DC gain in (3.13) and (3.4). Since the transconductors are usually single-stage circuits, it is not as straightforward to design a transconductor with a high DC gain as it is with opamps. However, at the same time, the non-dominant pole of a transconductor determining the  $\omega_{p2}$  of a gm-C integrator in (3.4) can be designed to lie at a much higher frequency than the  $\omega_{GBW}$  of an opamp. In fact, one can design a transconductor that has no internal poles [35]. Instead, to guarantee the stability of the opamp in the feedback loop, the opamp unity-gain frequency (i.e. the opamp GBW) is designed to occur at a much lower frequency compared to the position of the non-dominant pole determined by the opamp load capacitance. As an advantage, the gm-C technique does not have similar speed limitations to its closed-loop counterparts, the opamp-RC and MOSFET-C techniques.

The gm-C technique is therefore often used in high-frequency applications, including the experimental filter circuits of this work, presented in Chapter 7. The design and implementation of wideband gm-C filters are discussed in more detail in Chapters 4 and 6.

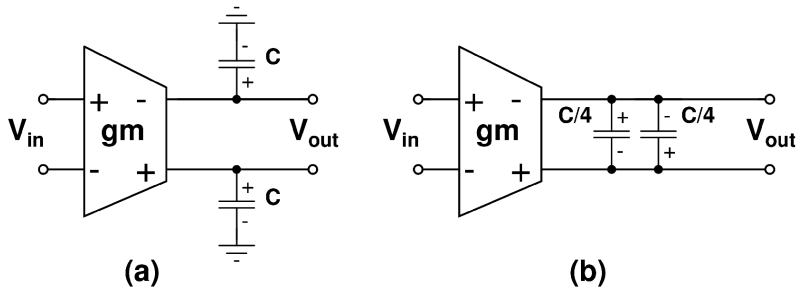


Figure 3.4. Balanced differential gm-C integrator with (a) grounded and (b) floating capacitors.

### 3.4 Other techniques

In this section, two recently proposed circuit techniques to realize integrated continuous-time low-pass filters are briefly introduced. The first one is called the active-gm-RC technique [25]. The basic building block is a biquad consisting of a passive RC pole connected at the input of a following feedback-connected two-stage opamp, as shown in Fig. 3.5. The transconductance of the opamp input stage is adjusted to be inversely proportional to  $R_i$  and the opamp is assumed to have a single-pole frequency response at the frequency range of interest. As a result, the frequency response of the opamp is exploited in the transfer function of the biquad cell. Therefore, the opamp unity-gain frequency can be designed to occur close to the pole frequency of the biquad, which is one of the key features of this structure. Because of the relaxed opamp unity-gain bandwidth requirement compared to the conventional opamp-RC approach, the power consumption of the opamp is reduced. In [25] and [39], the active-gm-RC technique was demonstrated to be suitable for filter implementations over 10 MHz wide. Furthermore, in the active-gm-RC filter reported in [39], a supply as low as 0.55-V was used.

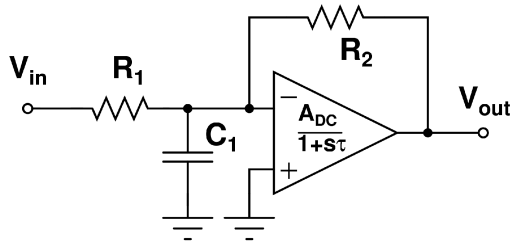


Figure 3.5. Active-gm-RC biquad cell.

Another recently proposed circuit technique is based on source followers [40], [41]. The transfer function of a capacitively loaded source follower is similar to a first-order low-pass filter. In [40], a fully differential single-branch biquad cell is built using two stacked source follower structures, as shown in Fig. 3.6. The complex pole pair of the biquad is synthesized by means of a positive feedback, realized with cross-coupled wires. This is basically the key proposal of the cell. The DC common-mode voltage at the input and output of a high-order cascade filter can be kept constant by alternating NMOS-source-follower-based biquads with their PMOS counterparts.

A modified version of the source-follower-based approach is presented in [41]. A continuous-time low-pass filter is realized as a sequence of positive and negative pseudo-differential first-order cells. The CMOS implementation of a positive and a negative first-order building block is shown in Fig. 3.7. The latter is needed to synthesize the complex poles. Both PMOS and NMOS transistors can be used to construct the cell. The pseudo-differential structure enables a lower supply voltage to be used compared to the original proposal shown in Fig. 3.6. In [41], a sixth-order 280-MHz low-pass filter consisting of cascaded positive first-order NMOS and negative PMOS cells was demonstrated.

It is common to both the source-follower-based filters presented here that there are no internal parasitic poles present in the filter. In addition, high linearity can be obtained even with reduced overdrive voltages ( $V_{GS} - V_{TH}$ ), in contrast to the gm-C technique, as a result of the internal feedback of the source follower circuits. Since a large overdrive voltage is not needed to improve the linearity of the biquads or the first-order cells forming the filter, the power consumption of the filter can be reduced. Similarly to a conventional source follower circuit, a source-follower-based filter ideally has a unity DC gain, but in practice the DC gain tends to be slightly lower. Therefore, in contrary to the conventional active filter techniques, a source-follower-based filter cannot be designed to have a voltage gain.



The block diagram of a master-slave tuning circuit is shown in Fig. 3.8. It consists of the main filter (slave) to be tuned and a typically simplified replica of the main filter (master), the output of which is monitored in order to figure out the corrections that are needed. The master filter may be, for instance, one of the integrators of the main filter or an on-chip oscillator circuit constructed from components similar to the ones used in the integrators of the main filter. The basic principle of the operation is as follows. First, the fabricated time constant(s) is measured. This is accomplished, for example, by applying an accurate reference signal  $V_{REF}$  that has a precise frequency to the master filter input in order to derive a (phase) response at a known frequency from its output. An on-chip or an off-chip crystal oscillator can provide such a reference signal. The error between the fabricated and desired time constants is detected by comparing the (phase) response of the master filter with the reference signal, for example, with a phase detector. Instead of the phase detection concept, another alternative is, for instance, to integrate a reference voltage applied into the input of the test integrator (i.e. the master filter) for a fixed time and compare the output of the test integrator with the reference voltage. The fixed integration time is controlled with an accurate reference clock signal. Typically, such a clock signal is available somewhere on a chip for signal processing. As a result of the comparison, a control signal that aims to reduce the error is generated. The control signal can be either a digital control word or an analog control voltage or current signal. The former can be used to control switched resistor or capacitor matrices or to switch parallel connected unit transconductors on and off. The latter can be used, for example, as a gate control voltage or to adjust the DC bias current or the voltage of the filter transconductors. In any case, the same control signal is used to adjust both the time constant(s) of the master filter and the time constants of the slave filter. Obviously, the scheme described above relies on a good matching between the components realizing the main and the slave filter. Therefore, in alternative realizations, the main filter is directly tuned without any replica integrators. More detailed system-level descriptions are given in, for example, [3], [5], [7], [8], and [17]. It should be pointed out that a similar concept can be used to tune integrator Q-factors as well. It is also worth emphasizing that the accuracy of the automatic tuning circuitry directly affects the filter frequency response accuracy. Automatic tuning circuit implementations utilizing the master-slave time-constant or Q-factor tuning scheme have been reported for opamp-RC filters, for example, in [20], [42], [43] and for gm-C filters in [35], [44]-[50].

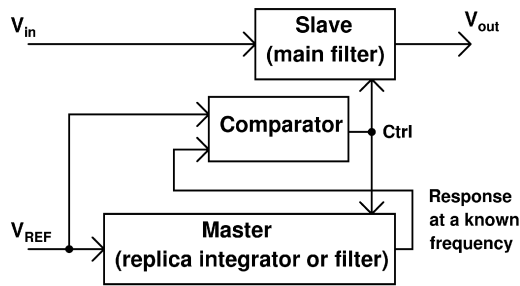


Figure 3.8. Block diagram of an automatic time-constant or Q-factor tuning circuit.

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## 4 Prototype and synthesis of active filters

At the very beginning of the filter design, an appropriate filter transfer function and the order of the filter have to be selected. In radio receivers, the bandwidth and, particularly, the selectivity requirement for channel-select and anti-aliasing filtering are determined by the wireless application being targeted, the specified or expected interferers scenario, and the performance of the ADC, as discussed in Chapter 2. The bandwidth and selectivity requirements of the analog baseband filter further depend on the receiver architecture adopted and the preceding filter stages. The filter transfer function and the order of the filter are then chosen according to the given selectivity requirement. In addition, for example, the passband flatness and phase response characteristics that are required have to be taken into account. In active filter implementations, the minimization of filter stages (i.e. the order of the filter) is typically beneficial in terms of noise, power consumption, and complexity. Therefore, it is important also to consider the feasibility of the active filter realization, as well as the performance requirements set for the filter block, before finally deciding on the filter prototype.

The next step is to synthesize the filter realizing the selected transfer function. Broadly speaking, there are two dominant approaches to synthesizing active continuous-time filters [1]-[3]. Active filters can be realized by biquads connected in a cascade in which each biquad implements a complex pole pair (with or without zeros) of the transfer function. Another approach is to simulate the operation of an LC ladder prototype filter. Lossless doubly terminated LC ladder filters are able to realize a large number of conventional filter transfer functions, such as Butterworth, Chebyshev, and Elliptic approximations. In addition, they are known to have a low sensitivity in their passband frequency response to component value variations [1]-[11]. The operation of LC ladder filters can be simulated with active filter realizations in such a way that a one-to-one correspondence between the reactive elements of the LC ladder and the integrators of the corresponding active realization is maintained [5], [8]. As

a result, these active filters inherit the low-sensitivity behavior [1]-[3], [5], [6], [8], [10]-[13]. Considering the operational simulation of LC ladder filters, the signal flow graph (SFG) method is one of the most widely used techniques to synthesize active filters from the desired LC ladder prototypes [1], [3], [5], [8], [10], [13]-[17]. The active filter realizations that are obtained can be called leapfrog or active ladder filters. Another popular method is to replace the inductors in an LC ladder filter by active circuits, for example, gyrators or general impedance converters (GICs) [1]-[3], [11]. In both cases, the active filter design starts with the selection of a suitable lossless LC ladder prototype. This is sometimes stated to be a drawback in the operational simulation approaches. However, when designing wideband integrated filters targeting an accurate frequency response, it is worth insisting on a low sensitivity to unavoidable component variations. Hence, the SFG method leading to component variation-tolerant leapfrog filter realizations has been used in all the experimental circuits implemented in this work.

In the first section of this chapter, some essential matters related to filter prototype design are briefly reviewed from the literature. These include the pole quality factor, the implementation of a transmission zero, and the extraction of a real pole from a given filter transfer function. They will play an important role in the experimental work presented later on in this thesis. The second section of this chapter deals with filter synthesis with lossy integrators. How the losses of a gm-C low-pass filter with embedded voltage gain can be taken into account in the filter synthesis is shown. In addition, it is presented how a gm-C leapfrog filter constructed from non-ideal finite-DC-gain integrators can be realized with a desired frequency response by predistorting the coefficients of the LC ladder prototype filter according to predefined losses. This is original research work in this thesis, previously published in [18], [19], and [20]. In the presentation in Section 4.2, the most relevant publications describing the work that others have done related to filter synthesis with non-ideal lossy integrators is cited as well.

#### 4.1 Filter prototype

The frequency response magnitude of an ideal brick wall filter is one at certain frequencies in order to pass the desired signal components without any distortion. Correspondingly, it is equal to zero at all other frequencies in order to block unwanted signal components. The frequency range of the former is called the passband and the latter is called the stopband. The transition band between the passband and stopband is zero in the case of an ideal brick wall filter. Since such an ideal frequency response can only be

approximated with a finite number of filter elements, several established transfer functions for practical filters exist, including Butterworth, Chebyshev, and Elliptic approximation. These functions are extensively presented elsewhere [1], [3], [21]-[23] and thus they are not reviewed in this thesis. The transfer function of a real filter can be written as a ratio of polynomials  $N(s)$  and  $D(s)$  [1], [3], [21]-[23]

$$\begin{aligned} H(s) &= \frac{N(s)}{D(s)} = \frac{a_M s^M + a_{M-1} s^{M-1} + \dots + a_0}{b_N s^N + b_{N-1} s^{N-1} + \dots + b_0} \\ &= \frac{a_M (s - z_1)(s - z_2) \dots (s - z_M)}{b_N (s - p_1)(s - p_2) \dots (s - p_N)}, \end{aligned} \quad (4.1)$$

where the coefficients  $a_i$  and  $b_j$  are real numbers and functions of the element values of the filter. The degree of the denominator  $N$  defines the order of the filter. For stability,  $N \geq M$  and all poles  $p_i$  must lie in the left half-plane [1], [22], [23]. Moreover, [19] states that the polynomial  $D(s)$  has all its roots in the left half-plane when its coefficients are positive (i.e.  $b_i > 0$ ). In other words, the denominator coefficients  $b_i$  must be real and positive numbers in order to prevent the oscillation of the circuit [3].

Both the transmission zero  $z_i$  and the pole  $p_i$  can be either a real or a complex number. Complex zeros and poles occur in conjugate pairs. The distance of the filter poles from the imaginary axis is determined by the pole quality factor  $Q_{pole}$  [3], [21], [23]. The higher the value of  $Q_{pole}$ , the closer the poles are to the imaginary axis, which corresponds to a more selective filter frequency response and a higher passband ripple.

#### 4.1.1 Transmission zero

A transmission zero can be added into the stopband of an all-pole low-pass filter. As a consequence, the attenuation of the filter changes more rapidly across the transition band without increasing the filter order. In addition, the stopband rejection of the filter improves in the vicinity of the transmission zero frequency. Thus, it may be advantageous to employ a transmission zero when designing selective active low-pass filters for radio receiver ICs. The attenuation at predetermined stopband frequencies is improved, while the power consumption, the number of noise sources, and the complexity of the filter remain unaffected. A transmission zero has been deployed in the experimental opamp-RC filter circuits presented in Chapter 5, as well as in publications [24] and [25].

Let us, as an example, add a transmission zero into the stopband of a fourth-order all-pole LC ladder prototype filter, shown in Fig. 4.1. The transfer function of the original fourth-order all-pole filter can be written as

$$H(s) = \frac{a_0}{b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \quad (4.2)$$

As presented in [21], a transmission zero locating at  $\omega_{zero}$  can be added into the LC ladder prototype by first placing a capacitor  $C_{zero}$  with a capacitance value of

$$C_{zero} = \frac{1}{\omega_{zero}^2 L_3} \quad (4.3)$$

in parallel with the inductor  $L_3$ . Next, the capacitance value  $C_{zero}$  calculated in (4.3) is subtracted from the capacitance value of the shunt capacitor  $C_4$ . The resulting filter transfer function with two complex-conjugate zeros at  $\pm j\omega_{zero}$  (i.e. at the  $j\omega$ -axis in the  $s$ -domain) can be expressed as

$$H(s) = \frac{a_0(s^2 - \omega_{zero}^2)}{b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \quad (4.4)$$

This example is based on an assumption that

$$\omega_{zero} = \frac{1}{L_3 C_{zero}} \geq \frac{1}{L_3 C_4}, \quad (4.5)$$

which will be the case in the experimental circuits presented in Chapter 5.

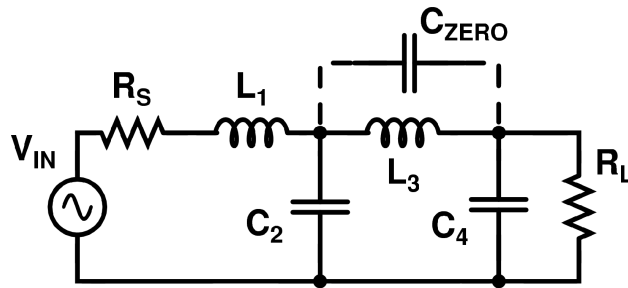


Figure 4.1. Fourth-order LC ladder prototype filter with a stopband transmission zero.

### 4.1.2 Real pole extraction

In addition to one or multiple complex pole pairs, an odd-order low-pass filter transfer function also includes a real pole lying on the real axis in the  $s$ -domain. The real pole can be extracted from the filter transfer function and realized with an RC pole at the filter input, as shown in Fig. 4.2 and formerly presented, for example, in [26]. Obviously, another option is to place an RC pole at the filter output. In the gm-C filter implementations of this work presented in Chapters 6 and 7, a real pole is extracted from a desired odd-order filter transfer function and realized at the filter input with the passive load components of a preceding downconversion mixer [18], [20], [27]. As a consequence, the stopband linearity of the filter increases considerably because the RC pole, hereafter called a passive pole, at the gm-C filter input attenuates out-of-band signals linearly before the signal processing with active devices [28]-[30]. System-level considerations on integrated radio receivers, including a passive pole at the mixer-baseband interface, were given in Section 2.3. It is worth pointing out that a passive RC pole can be implemented at the input of an odd-order or an even-order active low-pass filter as an additional filter stage as well. In that case all the poles (real and complex) of the desired filter transfer function are realized with the active filter and no pole extraction is needed in the filter synthesis. The difference between an extracted passive pole and an added extra passive pole is that the former can be placed at an even lower frequency compared to the passband edge frequency of the active filter without degrading the desired filter frequency response. However, the latter must be located at a much higher frequency compared to the passband edge frequency of the active filter unless the frequency response of the active filter is not predistorted. As a result, the active filter can benefit more from an extracted passive pole when the filter stopband linearity requirement is considered. At the same time, however, it has to be kept in mind that an accurate location of the real pole to be extracted is essential for an undistorted filter frequency response. In contrast, the location of an added extra passive pole is not as critical from an accurate filter frequency response point of view.

Although filter designers are familiar with the real pole extraction, the procedure is reviewed here for the sake of completeness. Without the loss of generality, let us assume a fifth-order low-pass filter transfer function. This corresponds to the filter order of the gm-C filter implementations presented in Chapters 6 and 7. The real pole can be extracted from the filter transfer function by presenting the denominator as a product of two polynomials as [20]



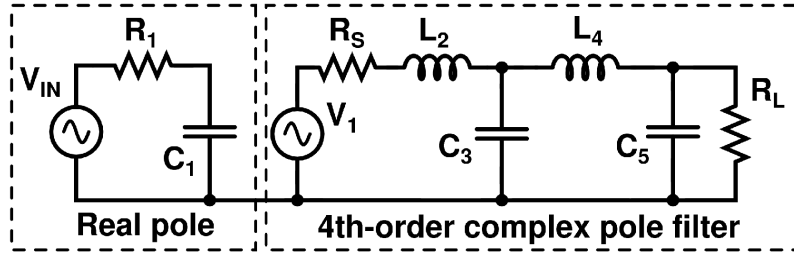


Figure 4.2. Fifth-order LC ladder prototype filter with an extracted real pole.

$$\begin{aligned}
 |S_{21}(s)|^2 &= \frac{G_{real}G_{complex}}{(a_0 - s^2)(b_4s^8 + b_3s^6 + b_2s^4 + b_1s^2 + b_0)} \\
 &= |S_{21}(s)|_{real}^2 |S_{21}(s)|_{complex}^2. \quad (4.6)
 \end{aligned}$$

The gain coefficients in the nominator must be chosen to be such that the separated transfer functions remain passive (i.e. have no gain). For the real pole this leads to the gain coefficient of  $G_{real} = a_0$ . The passivity condition for the transfer function consisting of complex poles is  $G_{complex} < \max(b_4s^8 + b_3s^6 + b_2s^4 + b_1s^2 + b_0)$ . A small  $G_{complex}$  results in a prototype with a low component value spread and a high load resistance. The power delivered to the load resistance is not important in active filter implementations, since the following receiver stage is typically seen as a capacitive load by the filter. However, a lower component value spread is preferable because the accuracy of the filter coefficients is improved. If  $G_{complex}$  is allowed to approach zero, then the load resistance approaches infinity and, hence, can be completely removed. The prototype component values for the transfer function realized by the four remaining complex poles can be calculated by first solving the reflection coefficient at the input port [31], [32]

$$|S_{11}(s)|^2 = 1 - |S_{21}(s)|_{complex}^2. \quad (4.7)$$

The zeros and the poles of  $|S_{11}(s)|^2$  are found using

$$S_{11}(s)S_{11}(-s) = |S_{11}(s)|^2, \quad (4.8)$$

from which the poles in the left half-plane must be chosen, as discussed earlier with (4.1). Having  $S_{11}(s)$ , the input impedance  $Z_{11}(s)$  can be solved from

$$Z_{11}(s) = R_S \frac{1 + S_{11}(s)}{1 - S_{11}(s)}, \quad (4.9)$$

where  $R_S$  is the source resistance. Finally, the component values of an LC ladder prototype filter can be extracted from  $Z_{11}(s)$  by using Causer expansion, as presented, for example, in [33]. This results in a fourth-order LC ladder filter, the transfer function of which can be written as

$$S_{21,complex}(s) = \frac{G_{complex}}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}. \quad (4.10)$$

The schematic of the fifth-order LC ladder prototype filter with the extracted real pole is shown in Figure 4.2.

## 4.2 Filter synthesis with lossy integrators

A filter design approach for continuous-time gm-C low-pass filters is presented in this section. It is original work in this thesis, previously published in [18], [19], and [20]. Therefore, this section is mainly based on the material in these publications<sup>1</sup>. The feasibility of the proposal is demonstrated by means of three gm-C filter implementations presented in Chapters 6 and 7. Although the focus will be on low-pass gm-C filters, the approach can be exploited, for example, in the design of opamp-RC low-pass filters. In addition, it should be sensible also to extend the method to other types of filters, such as band-pass and all-pass filters, but they have not been investigated in this work.

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<sup>1</sup>Portions of this section are taken from [18] (© 2007 IEEE), [19] (© 2007 IEEE) and [20] (© 2009 IEEE).

The conventional approach to designing gm-C filters is to realize the transconductors with a wide bandwidth and high DC gain, thus mitigating their effect on the filter frequency response. The effect of the integrator DC gain and bandwidth (the latter in terms of a parasitic pole) on the integrator Q-factor and the filter frequency response was studied theoretically in Section 3.1. It is generally difficult, however, to implement a transconductor that has both a sufficiently wide bandwidth and high DC gain simultaneously. This trade-off is further exacerbated by the very low supply voltages ( $\approx 1.2$  V) of modern ultra-deep-submicron CMOS technologies. In this work, the focus is particularly on wideband filters, in which the requirements for the bandwidth and DC gain of the transconductors become more demanding compared to their narrowband counterparts. Therefore, the approach proposed here is to accept a low DC gain for the transconductors, but to take the loss into account beforehand in the filter synthesis and predistort the frequency response accordingly [18], [20]. The low DC gain enables a simple transconductor circuit which has no internal bandwidth limitation to be used, as will be presented in Chapter 6. Although the DC gain can be low, it must be accurate with a precision dependent on the Q-values of the poles of the filter and the DC gain itself [34], [35]. All the transconductors in the filter are assumed to have a uniform, although finite, DC gain. Chapter 6 will describe how to adjust the DC gain of the transconductors to a predetermined nominal value, despite PVT variations. In the following, the filter design procedure is presented step by step. For the sake of clarity, the presentation is divided into separate sub-sections.

#### 4.2.1 Lossy LC ladder prototype filter

As discussed in the introduction to this chapter, the basic idea is to use the SFG method to derive an active gm-C leapfrog filter from a desired lossless LC ladder prototype filter. The losses of the gm-C filter integrators, including the finite DC gain of the transconductors, can be mapped to the passive LC prototype filter by placing a series resistor with the inductors and a shunt conductor with the capacitors in the LC prototype filter [19], [20]. This results in a lossy LC ladder prototype filter [31], [36]-[39], as shown in Fig. 4.3 for a fourth-order LC filter. Without any loss of generality, let us continue the study with the fourth-order filter. This corresponds to the filter order of the active gm-C filter implementations presented in Chapters 6 and 7. The V-I equations of the lossy LC prototype filter shown in Fig. 4.3 can be expressed as

$$\begin{aligned}
 I_2 &= \frac{V_1 - V_3}{sL_2 + R_S + R_2} \\
 V_3 &= \frac{I_2 - I_4}{sC_3 + G_3} \\
 I_4 &= \frac{V_3 - V_5}{sL_4 + R_4} \\
 V_5 &= \frac{I_4}{sC_5 + G_L + G_5}.
 \end{aligned} \tag{4.11}$$

Correspondingly, its transfer function can be written as [20]

$$H_{lossy}(s) = \frac{G_{lossy}}{x_4 s^4 + x_3 s^3 + x_2 s^2 + x_1 s + x_0}, \tag{4.12}$$

where the denominator coefficients  $x_0 - x_4$  are functions of the source and the load resistances ( $R_S$  and  $R_L$ ), the prototype component values ( $L_2$ ,  $C_3$ ,  $L_4$ , and  $C_5$ ), and the loss terms ( $R_2$ ,  $G_3$ ,  $R_4$ , and  $G_5$ ), as presented in Appendix A. The lossy LC prototype can be used to predistort the prototype component values ( $L_2$ ,  $C_3$ ,  $L_4$ , and  $C_5$ ) accordingly [20], as will be studied in more detail in Section 4.2.4. However, first the losses of the corresponding active gm-C filter are evaluated in the next sub-section.

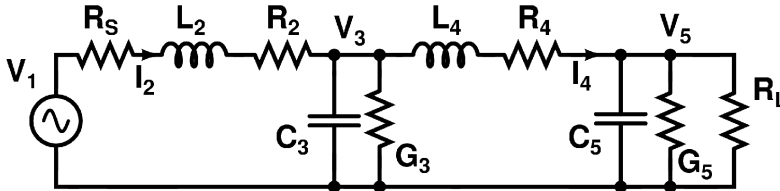


Figure 4.3. Lossy fourth-order LC ladder prototype filter.

#### 4.2.2 Active gm-C leapfrog filter with embedded voltage gain

A single-ended active gm-C filter synthesized from a desired lossless fourth-order passive LC ladder prototype filter by means of the SFG method is shown in Fig. 4.4. In practice, differential active filter topologies are employed in integrated filters, as presented in Chapter 6, but a single-ended counterpart is used in this study for the sake of simplicity. It is also worth pointing out once again that, without any loss of generality, in this study, a fourth-order filter has been selected as an example.

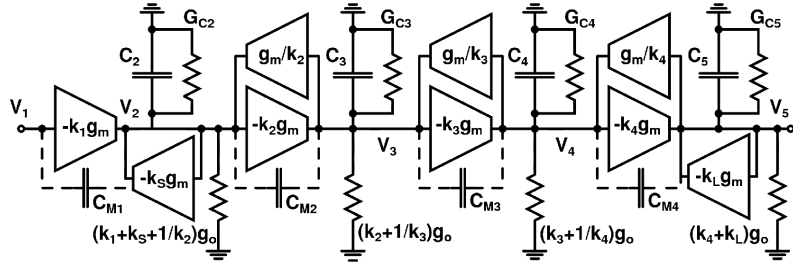


Figure 4.4. Single-ended fourth-order gm-C leapfrog filter with transconductor scaling factors  $k_i$  [20] (© 2009 IEEE).

Since in the proposed filter design approach the filter transconductors are allowed to have a low DC gain, the resulting finite (i.e. non-zero) output conductance ( $g_o$ ) is added at the output of each transconductance ( $gm$ ) element in Fig. 4.4. The finite DC gain of the transconductors can be expressed as

$$A_{DC} = \frac{gm}{g_o}. \quad (4.13)$$

When designing continuous-time low-pass filters for integrated radio receivers, it may be advantageous to embed potentially several decibels of voltage gain into the filter. The experimental gm-C filter circuits presented in this thesis have been designed to have voltage gain. The voltage gain can be implemented in the filter stages by scaling the size of the feedforward and feedback transconductors in opposite directions, as depicted in Fig. 4.4. For example, a gain value of 12 dB corresponds to a transconductor size ratio of 16. It is worth mentioning that in the experimental gm-C filter circuits presented in Chapters 6 and 7, a higher gain value would have been more challenging to implement in practice. The scaling factors  $k_S$ ,  $k_1$ ,  $k_2$ ,  $k_3$ ,  $k_4$ , and  $k_L$  shown in Fig. 4.4 scale the size, and hence the transconductance ( $gm$ ) and the output conductance ( $g_o$ ), of the transconductors with respect to the size of a unit transconductor. The integrator equations of the active filter realization shown in Fig. 4.4 can be written as

$$V_2 = -\frac{k_1 V_1 - \frac{1}{k_2} V_3}{s \frac{C_2}{gm} + k_S \frac{gm}{gm} + \frac{g_o}{gm} \left( k_1 + \frac{1}{k_2} + k_S \right)}$$

$$\begin{aligned}
 V_3 &= -\frac{k_2 V_2 - \frac{1}{k_3} V_4}{s \frac{C_3}{gm} + \frac{g_o}{gm} \left( k_2 + \frac{1}{k_3} \right)} \\
 V_4 &= -\frac{k_3 V_3 - \frac{1}{k_4} V_5}{s \frac{C_4}{gm} + \frac{g_o}{gm} \left( k_3 + \frac{1}{k_4} \right)} \\
 V_5 &= -\frac{k_4 V_4}{s \frac{C_5}{gm} + k_L \frac{gm}{gm} + \frac{g_o}{gm} (k_4 + k_L)}. \quad (4.14)
 \end{aligned}$$

The equations in (4.14) correspond to the V-I equations (4.11) of the passive LC prototype filter when it is taken into account that the former are derived for inverting integrators, while the latter represent non-inverting integrators. The quality factors of the filter integrators can be determined from (4.14) by using the definition (3.3). The effective Q-factors of each stage of the gm-C leapfrog filter determined at a frequency close to the passband edge of the filter become [20]

$$\begin{aligned}
 Q_{1,eff} &= \frac{A_{DC}}{k_S (A_{DC} + 1) + k_1 + 1/k_2} \\
 Q_{2,eff} &= \frac{A_{DC}}{k_2 + 1/k_3} \\
 Q_{3,eff} &= \frac{A_{DC}}{k_3 + 1/k_4} \\
 Q_{4,eff} &= \frac{A_{DC}}{k_4 + k_L (A_{DC} + 1)}, \quad (4.15)
 \end{aligned}$$

where  $Q_{1,eff}$  is a combination of the Q-factors of the lossy and the lossless integrators related to the first stage of the leapfrog filter,  $Q_{2,eff}$  is a combination of the Q-factors of the two lossless integrators related to the second stage of the leapfrog filter etc. In (4.15), the unloaded Q-factor of the gm-C integrators that have no internal poles is approximated to be equal to the DC gain of the transconductors

$$Q_{int}(\omega_{int}) \approx A_{DC} = \frac{gm}{g_o}, \quad (4.16)$$

as presented earlier in (3.5). The effective Q-factors in (4.15) are functions of the DC gain of the transconductors, the scaling factors of the source and the load resistances ( $k_s$  and  $k_L$ ), and the gain scaling factors of the feedforward and feedback transconductors ( $k_i$ ,  $i = 1, 2, \dots$ ). By studying these equations, it can be noted that the Q-factors are maximized when all the gain scaling factors are one, i.e. the filter has no gain. Conversely, it can be observed that the Q-factors decrease from their maximum value when voltage gain is embedded into the filter (i.e.  $k_i > 1$ ). This result clearly demonstrates the effect that embedded gain has on an active filter. A more obvious result is that the Q-factors in (4.15) are directly proportional to the nominal DC gain value of the transconductors and thus a reduced transconductor DC gain leads to a reduced value of the Q-factors.

The loss of a capacitor degrading the capacitor Q-factor can be represented by a shunt conductor with the capacitor, as shown in Fig. 4.4 and discussed in Section 3.1. The Q-factor of the capacitor defined near the passband edge frequency ( $\omega_c = 2\pi f_c$ ) of the filter can be expressed as [40], [41]

$$Q_{cap,n}(\omega_c) = \frac{\omega_c C_n}{G_{Cn}} \Big|_{n=1,2,\dots} \quad (4.17)$$

As discussed in Chapter 3, in active filters, the time-constant tuning of filter integrators can be accomplished with digitally controlled switched capacitor matrices. In all the filter implementations of this work, presented in the following chapters, capacitor matrices are employed to perform the tuning. In switched capacitor matrices, the Q-factor of the capacitors is easily degraded by the finite (i.e. non-zero) on-resistance of the switches. In addition, parasitic wiring resistances between capacitor matrices and filter transconductors may further reduce the Q-factor of the capacitors. When in (4.15) the Q-factor of the capacitors is also taken into account, the effective Q-factors of each leapfrog filter stage become

$$Q_{1,eff} = \frac{A_{DC}}{k_S(A_{DC} + 1) + k_1 + 1/k_2 + \frac{A_{DC}}{Q_{cap,2}}}$$

$$Q_{2,eff} = \frac{A_{DC}}{k_2 + 1/k_3 + \frac{A_{DC}}{Q_{cap,3}}}$$

$$Q_{3,eff} = \frac{A_{DC}}{k_3 + 1/k_4 + \frac{A_{DC}}{Q_{cap,4}}}$$

$$Q_{4,eff} = \frac{A_{DC}}{k_4 + k_L(A_{DC} + 1) + \frac{A_{DC}}{Q_{cap,5}}} . \quad (4.18)$$

It can be concluded in (4.18) that in order to reduce the term  $A_{DC}/Q_{cap,n}$  to zero, the capacitor matrices are required to have a high Q-value.

### 4.2.3 Mapping of non-idealities

Now that the losses of an active gm-C filter have been evaluated in Section 4.2.2, they can be mapped into the lossy LC prototype filter studied in Section 4.2.1 by comparing (4.14) and (4.11) with each other. The comparison results in

$$R_2 = \frac{g_{out}}{gm} \left( k_1 + \frac{1}{k_2} + k_S \right) = \frac{k_S + k_1 + 1/k_2}{A_{DC}}$$

$$G_3 = \frac{g_{out}}{gm} \left( k_2 + \frac{1}{k_3} \right) = \frac{k_2 + 1/k_3}{A_{DC}}$$

$$R_4 = \frac{g_{out}}{gm} \left( k_3 + \frac{1}{k_4} \right) = \frac{k_3 + 1/k_4}{A_{DC}}$$

$$G_5 = \frac{g_{out}}{gm} (k_4 + k_L) = \frac{k_4 + k_L}{A_{DC}} . \quad (4.19)$$

As can be seen in (4.19), the loss terms of the LC ladder prototype filter ( $R_2$ ,  $G_3$ , etc.) are functions of the DC gain of the transconductors, the scaling factors of the source and the load resistances, and the gain scaling factors of the feedforward and feedback transconductors, similarly to the effective Q-factors in (4.15).

If the losses of the capacitors are also taken into account, (4.19) can be rewritten as

$$R_2 = \frac{k_S + k_1 + 1/k_2}{A_{DC}} + \frac{G_{C2}}{gm}$$



$$\begin{aligned}
 G_3 &= \frac{k_2 + 1/k_3}{A_{DC}} + \frac{G_{C3}}{gm} \\
 R_4 &= \frac{k_3 + 1/k_4}{A_{DC}} + \frac{G_{C4}}{gm} \\
 G_5 &= \frac{k_4 + k_L}{A_{DC}} + \frac{G_{C5}}{gm} .
 \end{aligned} \tag{4.20}$$

#### 4.2.4 Predistortion of the filter coefficients

The predistortion of the filter coefficients can be performed analytically by requiring the denominator coefficients of the transfer function of the desired lossless LC prototype filter and of the corresponding lossy LC ladder filter to be equal [20]. A general fourth-order transfer function of a lossless LC prototype filter is shown in, for example, (4.2) or in (4.10). The transfer function of a corresponding lossy LC ladder filter is presented in (4.12). In (4.2) and (4.10), all the denominator coefficients are scalars. In (4.12), the denominator coefficients are functions of scalars ( $R_s$ ,  $R_2$ ,  $G_3$ ,  $R_4$ ,  $G_5$ , and  $R_L$ ) and variables ( $L_2$ ,  $C_3$ ,  $L_4$ , and  $C_5$ ), as presented in Appendix A. The pole quality factors of the desired lossless LC prototype filter set a limit on the amount of the losses allowed in the integrators of the active filter implementation. If the losses in the active filter implementation compared to the Q-values of the poles of the prototype filter are too much, the losses cannot be completely canceled with the predistortion of the filter coefficients. Hence, in the s-plane, the poles of (4.12) cannot be moved precisely onto the poles of the original lossless prototype filter and the desired filter transfer function is either degraded or it cannot be realized at all. If the losses of the active filter implementation cannot be reduced, one can try to optimize the frequency response of the lossy prototype filter only at fixed frequencies in the passband and stopband of the filter according to custom-defined criteria. It also is worth pointing out that the more the filter coefficients have to be predistorted, the more sensitive the filter frequency response becomes to the losses.

When accepting a low, non-ideal value for the DC gain of the filter transconductors, it is practical to choose a uniform DC gain value for each transconductor, as is the case in this filter design approach. During the first design phases, the DC gain of the transconductors is fixed to a certain nominal value. It must be feasible to implement the nominal DC gain value in practice with the transconductor topology adopted and the technology used. As soon as the DC gain of the transconductors is fixed to a certain nominal value, the realizability of the prototype can only be improved by

reducing the passband ripple of the prototype and by minimizing all the other losses in the filter [20]. The first option pushes the poles of the filter transfer function further away from the imaginary axis and thus allows a more lossy filter to be implemented. As a drawback, because of the reduced pole quality factors, the transition band steepness of the filter is degraded. Hence, the filter becomes less selective. (As an interesting historical detail, as early as in the 1960s, Desoer and Mitra found and reported in [37] that a decrease in the passband ripple to improve the passband frequency response of a lossy LC ladder filter is associated with a decrease in the stopband attenuation.) The gain scaling factors play an important role when the other losses in the gm-C filter are being considered, i.e. other than a low DC gain of the transconductors. This is because the voltage gain embedded into the filter stages degrades the Q-factors of the integrators, as studied in Section 4.2.2. Therefore, the predistortion of the filter coefficients becomes more difficult or even impossible in the case of a filter with large amounts of voltage gain compared to a filter with no gain. This effect worsens with a reduction in the DC gain of the transconductors.

It should be pointed out here that lossy LC ladder filters and different kinds of predistortion or precompensation methods have been used in filter design for a long time. Some kinds of predistortion techniques were used to compensate for the losses of reactive elements in passive LC ladder filters, for example, in [37], [43], and [44]. Active RC filters were derived from lossy LC ladder prototype filters, for example, in [6] and [45]. It was proposed and demonstrated with a circuit implementation in [34], [46], [47] that an SC biquadratic filter can be designed using fast amplifiers with a low but precisely controlled gain value if the effect of the low gain value is compensated for in the design phase. In [16], it was proposed, although not shown, that the effect of the finite output conductance of transconductors on the frequency response of a gm-C filter can be corrected by predistortion. In [48], it was proposed and verified with simulations for a BiCMOS continuous-time gm-C biquadratic cell that the effect of a finite impedance at each transconductor output and hence, each filter node can be reduced. This was accomplished by placing a controlled active output load at each filter node and by taking the value of the load into account in the filter design phase. In [35], a gm-C filter was implemented by cascading quadratic sections each constructed from two identical lossy gm-C integrators whose effect was eliminated by controlling the DC gain of the transconductors precisely.

The filter design approach proposed in [48] has some similarities with the filter design approach presented in this thesis. However, to the best of the author's knowledge, in the approach proposed in [48], the idea is to place

such a low-impedance load at the transconductor output that its impedance dominates the overall output impedance of the transconductor over the inherent output impedance of the transconductor. This corresponds to reducing the inherent DC gain of the transconductor, instead of enhancing it. Moreover, considering the design of the biquadratic cell presented in the publication [48], an identical low-impedance load was placed in each filter node instead of adjusting a uniform DC gain for each transconductor in the filter. In the work of this thesis, the losses caused by the embedded voltage gain and non-ideal capacitors in a gm-C leapfrog filter have been taken into account in the filter synthesis, in addition to the finite nominal DC gain that is uniform for each transconductor. Moreover, the effect of the source and load resistances on the filter losses will be studied in Section 4.2.6. Finally, the experimental work will be presented in Chapters 6 and 7.

#### 4.2.5 Design trade-offs

When gm-C leapfrog filters with lossy integrators are being designed, design trade-offs exist that will be discussed in this sub-section by means of a design example. The filter prototype used in the design example is a fifth-order Chebyshev filter with a 0.02-dB passband ripple. In addition, it is assumed that the real pole is extracted from the filter transfer function and realized as a separate filter stage at the input of the prototype filter, as shown in Fig. 4.2. The corresponding active gm-C leapfrog filter of this design example is similar to that shown in Fig. 4.4, except that an additional RC-pole stage is placed at the filter input. The gain partitioning in the gm-C leapfrog filter is assumed to be fixed, e.g. because of the noise and linearity requirements of the filter, in such a way that the gain scaling factors  $k_1$ ,  $k_2$ ,  $k_3$ , and  $k_4$  (Fig. 4.4) are 8, 4, 4, and 1, respectively. The losses of the active gm-C leapfrog filter are mapped into the LC prototype filter, resulting in a lossy LC ladder filter similar to that in Fig. 4.3, except for the additional RC pole at the filter input. Considering the filter order selected, the real pole extracted, and the gain partitioning, this design example is consistent with the gm-C filter implementations presented in Chapters 6 and 7. This sub-section is based on the analysis and simulation results previously published in [19].

In addition to the fixed gain partitioning in the gm-C leapfrog filter, let us assume a 24-dB DC gain for the transconductors and study the component spread and sensitivity as a function of the source resistance. The selected transconductor DC gain value is consistent with the gm-C filter implementations presented in Chapters 6 and 7. The relationship between the component spread and source resistance is shown by the left-hand curve in Fig 4.5. It can be seen in Fig. 4.5 that it is possible to optimize the

component spread of the filter by means of an appropriate selection of the source resistance. The curve on the right-hand side in Fig. 4.5 shows how the sensitivity of the filter to component variations changes with the source resistance. The change in sensitivity is small, implying that the component spread does not have to be traded for sensitivity. The sensitivities of the individual reactive components of the lossy LC ladder filter in Fig. 4.3 vary from 1.4 to 7. The sensitivity of the component  $L_4$  is the largest and the sensitivity of the component  $L_2$  is the smallest.

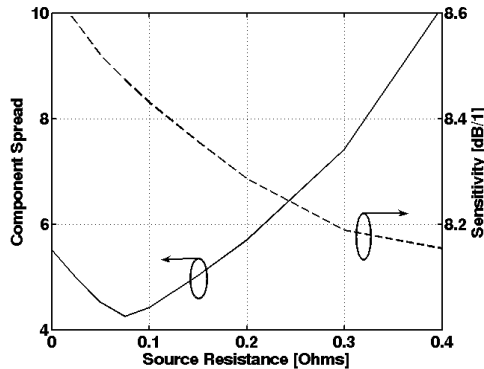


Figure 4.5. Component spread and sensitivity to component variations [19] (© 2007 IEEE).

The optimum source resistance and the corresponding component spread are shown in Fig. 4.6 as a function of the altered DC gain of the transconductors. It can be seen in Fig. 4.6 that a low DC gain value leads to a higher component spread and a lower optimal source resistance value. For the gain scaling factors that were selected, the optimal source resistance will become zero when the DC gain is 23 dB and the filter approaches its realizability limit. The sensitivity of the filter frequency response to the DC gain variation of the transconductors is presented in Fig. 4.7. Fig. 4.7 shows that, e.g. for a DC gain of 25 dB, the simulated gain variation at the passband edge of the filter is 0.7 dB for a DC gain accuracy of 1 dB.

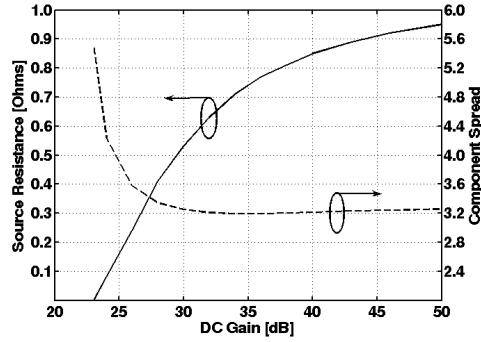


Figure 4.6. Optimum source resistance and component spread [19] (© 2007 IEEE).

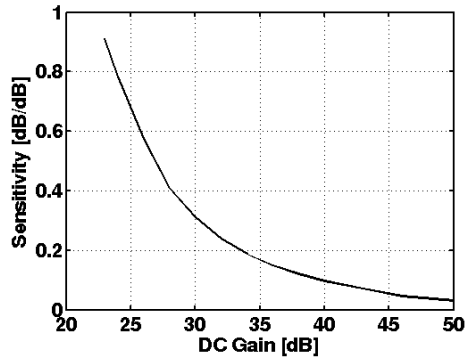


Figure 4.7. Sensitivity to DC gain variation [19] (© 2007 IEEE).

#### 4.2.6 Source and load resistances

Assuming that the DC gain of the transconductors and the gain partitioning in the filter are fixed, the integrator Q-factors in (4.14) can be altered only by scaling the source and load resistances. It can be seen from (4.14) that the integrator Q-factors are increased by setting the source and the load resistances of the prototype filter to zero, i.e.  $k_S = k_L = 0$  [19]. This corresponds to removing the source and the load resistors from the passive LC prototype filter shown in Fig. 4.3 and the related diode-connected transconductors from the first and the last stages of the active gm-C leapfrog filter shown in Fig. 4.4, respectively. Instead of the diode-connected transconductors, the real parts of the poles of the filter transfer function can be realized with the output conductors of the transconductors. The removal of the prototype resistors has substantial benefits when a lossy prototype filter is being synthesized. When the source resistor is removed, the gain of the first stage ( $k_I$ ) has to be made larger to cause an equivalent real factor to the denominator of the first equation in (4.14). If the total gain of the filter is kept constant, then the other gain scaling factors of the filter

are reduced and the corresponding integrator Q-values are improved. Respectively, if a maximal transition band steepness is pursued in the filter transfer function, then the integrator Q-value improvement attained from the removal of the resistors can be used to select a filter transfer function with higher pole quality factors. However, this approach would require the gain scaling factors  $k_l$  and  $k_d$  to be freely selectable, which may not always be the case in a practical gm-C filter implementation. In addition, the filter becomes more sensitive to component variations without the diode-connected transconductors or, at least, it is more challenging to keep the source and load resistances constant without the diode-connected transconductors because of PVT variations. The sensitivity analysis falls outside the scope of this thesis because this thesis concentrates on the design and implementation of wideband continuous-time filters. It should, however, be emphasized that the active gm-C filter implementations presented in Chapters 6 and 7 were synthesized by setting the load resistance of the prototype filter to zero ( $k_L = 0$ ).

#### 4.2.7 Parasitic Miller capacitances

In addition to the losses of the filter integrators, the parasitic Miller capacitances of the transconductors,  $C_M$ , shown with dashed lines in Fig. 4.4, affect the frequency response of this wideband filter by adding high-frequency zeros to the filter integrators. When the effects of the parasitic Miller capacitances are taken into account, the integrator equations in (4.14) can be rewritten as

$$\begin{aligned}
 V_2 &= \frac{(k_1 gm + sC_{M1})V_1 - (gm/k_2 - sC_{M2})V_3}{s(C_2 + C_{M1} + C_{M2}) + k_S gm + (k_1 + k_S + 1/k_2)g_o} \\
 V_3 &= \frac{(k_2 gm + sC_{M2})V_2 - (gm/k_3 - sC_{M3})V_4}{s(C_3 + C_{M2} + C_{M3}) + (k_2 + 1/k_3)g_o} \\
 V_4 &= \frac{(k_3 gm + sC_{M3})V_3 - (gm/k_4 - sC_{M4})V_5}{s(C_4 + C_{M3} + C_{M4}) + (k_3 + 1/k_4)g_o} \\
 V_5 &= \frac{(k_4 gm + sC_{M4})V_4}{s(C_5 + C_{M4}) + k_L gm + (k_4 + k_L)g_o}. \quad (4.21)
 \end{aligned}$$

Because of the parasitic Miller capacitances, the frequency response of the fifth-order prototype resembles the frequency response of a fourth-order prototype when the number of minima and maxima at the passband are considered. According to the Miller theorem, in this gm-C filter, parasitic Miller capacitances can be replaced by grounded capacitors at the input and

output of the transconductors. The effects of these additional input and output capacitances of the transconductors can then be compensated by reducing the value of the original filter coefficients  $C_2$ - $C_5$ , as can be seen in the denominators of (4.21). However, the transmission zeros in the nominators of (4.21) remain uncompensated. Thus, the effects caused by the parasitic Miller capacitances can be compensated, but not completely canceled, by using the Miller theorem.

#### 4.2.8 Summary

As a summary, let us go through the design flow once again. First, a lossless doubly terminated LC ladder prototype filter realizing a desired filter transfer function is synthesized or directly designed by using component value tables available in filter handbooks, such as in [42]. Next, a corresponding active gm-C filter is synthesized from the lossless LC prototype filter. After that, in the passive LC ladder prototype filter, a resistor is placed in series with each inductor and, correspondingly, a conductor in parallel with each capacitor resulting in a lossy LC ladder prototype filter. The losses of the active gm-C filter will be mapped into the passive LC prototype filter by means of these extra components. The losses of the gm-C filter are evaluated next. They include the finite DC gain of the transconductors, the effect of embedded gain in the gm-C filter, and potentially also the losses of the capacitor matrices as a result of the finite (i.e. non-zero) on-resistance of the switches. Once the evaluated losses of the gm-C filter are mapped into the lossy LC prototype filter, the filter coefficients of the prototype filter are predistorted according to the losses in order to realize the desired filter transfer function. The predistortion can be performed either analytically or by using filter frequency response optimization tools. In the former case, the desired filter transfer function (e.g. Butterworth or Chebyshev) can be realized precisely. If the transfer function is not realizable because of too large an amount of losses, the procedure has to be continued, either by reducing the losses or selecting a new filter transfer function with lower pole Q-values. If the aforementioned optimization tools are used, a custom-defined filter frequency response may be found, despite the relatively large amount of losses.

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## 5 Opamp-RC filters for multicarrier WCDMA base-station receivers

This chapter describes the circuit design of two evolution versions of continuous-time opamp-RC low-pass filters that were implemented in this work as a part of two single-chip multicarrier UTRA FDD WCDMA base-station receivers. Hereafter UTRA FDD WCDMA is called simply WCDMA. The two opamp-RC low-pass filters that were designed, implemented, and measured and are included in this chapter are original work in this thesis, previously published in [1] and [2]. The corresponding versions of the multicarrier receiver IC implementations were previously reported with experimental results in [3] and [4]. To the best of the author's knowledge, the former is the first published single-chip multicarrier WCDMA receiver implementation. Since the main interest in this thesis is in the design and implementation of continuous-time low-pass filters for integrated radio receivers, rather than concentrating on stand-alone filter circuits, both multicarrier receiver implementations are also briefly presented in this chapter. Moreover, since the operation of the opamp-RC low-pass filters that were designed being embedded in a single-chip radio receiver affects the overall performance of the receiver, the experimental results of both the low-pass filters and the multicarrier receivers are shown at the end of this chapter. This chapter is mainly based on the contents of the four publications cited above<sup>2</sup>.

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<sup>2</sup>Portions of this chapter are taken from [1] (© 2006 IEEE), [3] (© 2006 IEEE), [4] (© 2006 IEEE), and with permission from Springer Science+Business Media: [2], © 2007 Springer Science+Business Media.

In Section 5.1, the concept of a multicarrier WCDMA receiver is introduced first. The discussion is continued by introducing the requirements of the multicarrier receiver and the low-pass filters in the targeted base-station application. The main differences between the requirements of an integrated receiver in a conventional single-carrier WCDMA handset application and in a multicarrier base-station application are emphasized. In integrated single-chip receivers, a voltage-mode or a current-mode mixer-baseband interface can be used. Circuit techniques to implement both types of interfaces are first briefly reviewed in Section 5.2. One of the design goals in the multicarrier receiver implementations under consideration was to strive for highly linear active downconversion mixers. Since the mixer load and, thus, the mixer-baseband interface that is selected has an influence on the mixer linearity, as well as on the linearity of the following analog baseband circuit, special attention is paid to the implementation of the mixer-baseband interface in the multicarrier receivers that are designed. Design considerations related to the above-mentioned investigation were previously published in [5] and are included in this thesis in Section 5.2. Section 5.3 is devoted to describing the circuit design of the opamp-RC low-pass filters that were implemented. The two multicarrier receiver IC implementations are presented in Sections 5.4 and 5.5 with the experimental results of both the low-pass filters and the whole receivers. The results of the two low-pass filter implementations are summarized and compared to the work of others in Section 5.6.

## 5.1 Multicarrier WCDMA base-station receiver

A single WCDMA base-station (BS) can receive several adjacent channels allocated to one operator simultaneously. In a conventional BS, these channels are received by means of separate parallel receiver chains. By using a single multicarrier IC that does not need parallel blocks, the size and cost of the BS can be reduced [3], [6], [7]. In a multicarrier WCDMA BS transmitter, the parallel channels are combined in the digital domain and transmitted by means of a single analog transmitter chain [7]. Similarly, in a multicarrier receiver, the separation of the adjacent channels received using a single analog receiver chain can be performed in the digital back-end [8]. Since the number of adjacent channels allocated for different operators may vary, it would be advantageous if a single IC could be digitally adjusted to receive from one to multiple WCDMA channels simultaneously, depending on the need [4].

A simplified block diagram of the integrated multicarrier WCDMA receiver under consideration is shown in Fig. 5.1. It consists of a low-noise

amplifier (LNA), quadrature downconversion mixers, a local oscillator (LO) divider, active continuous-time low-pass filters, and ADC buffers. As can be seen in Fig. 5.1, differential signal processing is assumed, which is the usual case in integrated radio receivers. Typically, in analog integrated circuits, including continuous-time low-pass filters, it is preferable to process signals differentially because a larger voltage swing can be achieved at the same time as reduced disturbances, leading to a higher signal-to-noise ratio (SNR) compared to the use of single-ended circuit blocks. A 0.25- $\mu\text{m}$  SiGe BiCMOS technology dedicated to RF and microwave applications was adopted for the receiver design, and for the RF front-end design in particular, in order to meet the challenging performance requirements set by the base-station application. The first evolution version of the multicarrier receiver that was implemented uses a low-IF architecture and can receive four adjacent WCDMA channels simultaneously [3]. The second evolution version of the multicarrier receiver can be programmed to receive from one to four adjacent channels [4]. This receiver uses either direct-conversion or low-IF reception, depending on the number of channels received. Fig. 5.2 shows an example of the downconverted spectrum when the receiver is programmed to receive four adjacent channels. The spectrum consists of two 3.84-MHz-wide downconverted channels centered at the 2.5-MHz (Ch1) and 7.5-MHz (Ch2) intermediate frequencies. Both downconverted channels, Ch1 and Ch2, include two WCDMA channels. The separation of the channels will be performed in the digital domain after the analog-to-digital conversion [8]. As discussed in Section 2.1.3, in low-IF receivers, a successful separation requires sufficiently high I/Q matching. However, it is difficult to achieve sufficiently high I/Q matching in the analog domain. The matching can change during the reception if a programmable gain is implemented in the analog IF or baseband circuit [3]. In the in-band of a multicarrier base-station receiver, the power levels of the adjacent WCDMA channels can be assumed to be almost equal, as will be discussed in Section 5.1.3, alleviating the I/Q matching. Therefore, in the multicarrier receiver implementations of this work, the I/Q calibration was left for the digital back-end and the receivers were designed to drive high-resolution Nyquist-rate ADCs without programmable gain. An example of the targeted ADCs is given in [9] and [10]. The RF pre-select filter preceding the integrated multicarrier receiver, not shown in Fig. 5.1, and the active continuous-time low-pass filters of the receiver provide the required anti-aliasing filtering for the ADCs.

In the design of the analog front-end for a multicarrier WCDMA BS receiver, some requirements differ from the typical requirements of mobile-station (MS) receivers [11]-[14]. The main differences arising from the

multicarrier approach are related to the intermodulation and blocking tests. The requirements of the multicarrier receiver analog front-end under consideration and, particularly, of the continuous-time low-pass filters are introduced in the following sub-sections.

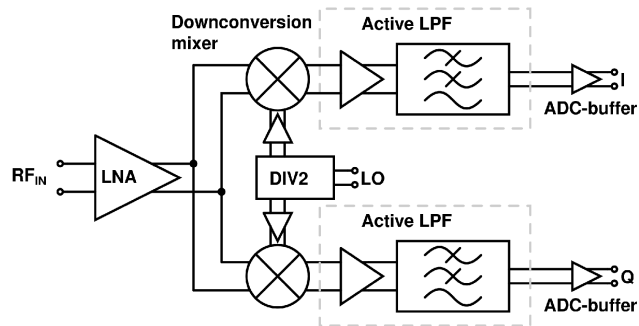


Figure 5.1. Block diagram of a single-chip multicarrier WCDMA receiver with active continuous-time low-pass filters with embedded gain.

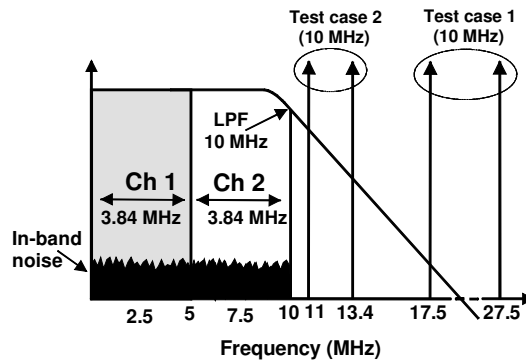


Figure 5.2. Downconverted WCDMA channels and out-of-band interfering signals in the case when the multicarrier receiver is programmed to receive four adjacent channels simultaneously (with permission from Springer Science+Business Media: [2], Fig. 1, © 2007 Springer Science+Business Media).

### 5.1.1 Operating RF band and baseband bandwidth

The operating uplink (i.e. the mobile transmits and the base-station receives) bands of the WCDMA system were presented in Table 2.1 in Section 2.4.1. The targeted operating bands define the operating frequency range of the RF front-end of the receiver. Correspondingly, in the same section, the signal bandwidth and the nominal channel spacing of the WCDMA system were discussed as being 3.84 MHz and 5 MHz, respectively. Hence, when receiving from one to four adjacent WCDMA channels simultaneously is targeted, the  $-3$ -dB bandwidth of the low-pass

filter can be chosen to be programmable from 2.5 MHz to 10 MHz in 2.5-MHz frequency steps [4].

### 5.1.2 Out-of-band linearity requirement

The 3GPP specification defines two types of intermodulation tests, one for wideband out-of-band signals and one for nearby narrowband signals [14]. The location of the intermodulation test tones is illustrated in Fig. 5.2 for the case of four-channel reception. In the first test case, the wideband interfering signals are located at 10-MHz and 20-MHz offsets from the center of the channel Ch2. In the second test case, the narrowband interfering signals are located at 3.5-MHz and 5.9-MHz offsets from the center of the channel Ch2. Although the absolute frequency offset between the center of the received channel and the intermodulation test signals is the same in both multicarrier and single-carrier receivers, the test is more demanding in the case of a multicarrier receiver when the order and prototype of the low-pass filter are the same in both cases. It is shown in Fig. 5.2 that the  $-3$ -dB bandwidth of the low-pass filter can be designed to be 10 MHz when four adjacent WCDMA channels are to be received simultaneously. Thus, relatively, the narrow-band interfering signals are located at 10% and 34% offsets from the 10-MHz filter passband edge. The attenuation of a realistic (let us say a 4th-order or a 5th-order) low-pass filter will be around 10 dB. Therefore, the requirement for the out-of-band linearity of the low-pass filter in the vicinity of the passband edge becomes very high. In a single-carrier WCDMA receiver, the  $-3$ -dB bandwidth of the low-pass filter is approximately 2.5 MHz. In this case, the narrow-band interfering signals are located at 3.5 MHz and 5.9 MHz. Relatively, they are at 40% and 136% offsets from the 2.5-MHz filter passband edge. In this case, the low-pass filter, which has a similar prototype, attenuates the narrowband interfering signals approximately 15-25 dB more than in the multicarrier case under study, leading to a relaxed linearity requirement.

As an example of the out-of-band linearity requirement of the low-pass filter in a receiver, let us assume that the out-of-band IIP<sub>3</sub> of the RF front-end without the low-pass filter is  $-10$  dBm and the low-pass filter is allowed to reduce the out-of-band IIP<sub>3</sub> of the whole receiver to  $-11$  dBm [4]. Moreover, let the voltage gain of the receiver and the low-pass filter be 51.5 dB and 18 dB, respectively [2], [4]. The out-of-band IIP<sub>3</sub> requirement of the low-pass filter can be calculated to be  $-14$  dBV at the receiver input. The corresponding value at the filter input is  $+19$  dBV which is more challenging to achieve with a wideband low-pass filter required in the multicarrier receiver under consideration.



Table 5.1. Blocking performance requirements according to the 3GPP specification [14]

Blocking performance requirement	Interfering signal mean power	Offset at the IF with respect to Ch2
Adjacent channel selectivity	-52 dBm	5 MHz
WCDMA signal	-40 dBm	10 MHz
GMSK modulated signal	-47 dBm	2.7 MHz

In addition to the intermodulation tests, the 3GPP specification defines the blocking performance requirements for the base-station radio reception [14], as presented in Table 5.1. These out-of-band blocking signals, including a narrowband blocking signal located close to the filter passband edge, create additional requirements for the design of the continuous-time low-pass filter. These blockers must be taken into account when the gain partitioning in the filter is being designed in order to avoid the clipping of the blocking signals.

### 5.1.3 In-band linearity

In a multicarrier receiver, an additional in-band linearity requirement may arise if the input powers of the desired in-band signals differ significantly. However, this is not a problem in the multicarrier receiver implementations of this work since the BS controls the powers of the adjacent WCDMA channels. The BS will keep the powers at the antenna input close to each other in order to maximize the system performance [3].

### 5.1.4 Noise requirement

In BS applications, the minimization of the receiver noise figure is one of the key drivers. In a low-IF receiver, the noise generated after the division into the I- and Q-branches is uncorrelated and cannot be removed later in the signal chain with image-reject techniques. Therefore, after the division into the I- and Q-branches, the equivalent noise bandwidth is twice the channel bandwidth, which is 3.84 MHz in WCDMA. This means that in a low-IF receiver the input-referred noise density (in W/Hz) of the circuits following the I/Q division must be half that of the corresponding blocks in a direct-conversion receiver if the NFs of the two receivers are equal [3].

As already pointed out in Section 2.1.2, in direct-conversion and low-IF receivers, the noise of the analog baseband or IF circuit typically has a significant effect on the total NF of the receiver, because of the moderate gain of the RF front-end. When a low NF is being targeted in the multicarrier receiver under consideration, the noise contribution of the low-pass filter has to be as small as possible, on the basis of (2.2). As an

example, let us assume that the NF of the RF front-end in the low-IF mode without the low-pass filter is 2.5 dB and the low-pass filter is allowed to increase the NF to 2.7 dB [4]. The noise density of the low-pass filter referred to the filter input becomes as low as  $8.7\text{-nV}/\sqrt{\text{Hz}}$  when the receiver and the filter voltage gains are the same as in the previous example presented in Section 5.1.1 (i.e. 51.5 dB and 18 dB, respectively). Because of the blocking signals introduced in Table 5.1, the gain of the filter must be distributed between different filter stages, instead of the gain merely being embedded into the first filter stage, which would have been an optimal choice for the noise. Hence, in this application, the noise performance of all the filter stages becomes demanding.

### 5.1.5 Other considerations

Since the operator maintains the input power of the adjacent WCDMA channels at approximately equal levels, a natural choice is to downconvert the adjacent channels in such a way that the in-band signal of the analog low-pass filter consists only of channels belonging to the operator [3]. Then the power of the image channel is approximately equal to the power of the desired channel. This scheme relaxes the requirements of the digital image rejection compared to the case where the image signal is not controlled by the same operator, such as a blocking signal or a WCDMA channel belonging to another operator.

## 5.2 Mixer-baseband interface

In all the receiver implementations presented in this thesis (Sections 5.4 and 5.5, as well as Chapter 7), an active Gilbert cell downconversion mixer precedes the analog baseband (or IF) low-pass filter. The Gilbert cell mixer is one of the most commonly used active mixer topologies in integrated radio receivers, especially, in BiCMOS implementations. It consists of an RF transconductance stage performing the voltage-to-current conversion, an LO switching core performing the mixing, and a load which simultaneously forms the interface to the following receiver stage [5], [15], [16], as shown in Fig 5.3. The signal current from the LO switches in a Gilbert cell-type mixer can be converted into a voltage signal at the mixer output or it can be directly driven into the following analog baseband filter. Depending on whether the output signal of the mixer is voltage or current, it has an effect on the performance of the mixer and the analog baseband filter and, hence, on the performance of the entire integrated receiver. The effects which are considered to be the most important in the receiver ICs

that were implemented and presented in this thesis are briefly discussed in this section. The main emphasis is on the linearity of both the mixer and the baseband filter. A theoretical study is given to support the discussion. It should be pointed out, however, that the purpose of the study is not to try to find a universal solution to the interesting question of which one of the mixer-baseband interfaces, a voltage-mode or a current-mode one, is better from the baseband out-of-band linearity point of view. The following discussion is mainly based on [5]<sup>3</sup>.

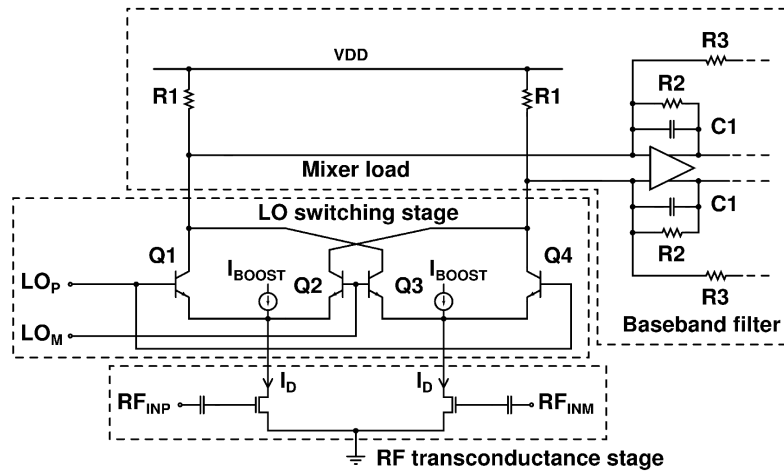


Figure 5.3. Simplified schematic of a double-balanced Gilbert cell downconversion mixer with a current-mode interface to an opamp-RC baseband filter [5] (© 2008 EuMA).

<sup>3</sup>Portions of this section are taken from [5] (© 2008 EuMA)

In the voltage-mode operation of a Gilbert cell downconversion mixer, the output current from the LO switches is typically converted into voltage using a resistive load at the mixer output. There are several alternative ways to realize a resistive load at the balanced output of a Gilbert cell mixer, as shown in Fig. 5.4 [16], [17]. The first stage of the following analog baseband circuit (whether it is the first stage of a continuous-time low-pass filter or a VGA) must have a high input impedance in order not to load the mixer output. In practice, this can be accomplished by placing a transconductor as the first baseband stage in the case of both a following opamp-RC [18] and a gm-C low-pass filter [19]. Therefore, the first baseband stage in Fig. 5.4 is depicted with a transconductor. In addition, in all the resistive load alternatives presented in Fig. 5.4, the mixer is DC-coupled to the baseband, which is the usual case in integrated receivers. The DC offset removal schemes briefly discussed in Chapter 6 also include AC coupling between the downconversion mixer and the analog baseband circuit, leading to high-pass filtering. However, the modulation method used in a certain communication or radio (e.g. radar) system does not necessarily allow any high-pass filtering at the baseband, which is the case when there is not a spectral null at the DC. As a consequence, the mixer has to be DC-coupled to the baseband and the output of the downconversion mixer and the input of the first baseband stage must be designed to share the same DC bias voltage.

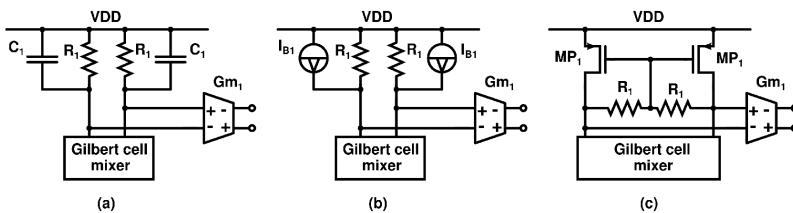


Figure 5.4. Different alternative ways to realize a voltage-mode mixer-baseband interface: a) an RC mixer load, b) a resistor load with a parallel current source to increase the value of the resistive load, and c) floating resistor loads with PMOS current sources which provide a DC bias current for the mixer.

The voltage-mode output signal modulates the collector-emitter voltage of the mixer switching transistors ( $Q_1$ - $Q_4$  in Fig. 5.3), which degrades the linearity of the mixer as presented and compared with a current-mode mixer output in [5]. As a conclusion from [5], the size of the linearity degradation in a Gilbert cell mixer resulting from the voltage-mode operation depends on the supply voltage that is available and the resistance of the load resistors, i.e. the voltage gain of the mixer. Considering the following analog baseband low-pass filter, the load of the mixer can simply

be used as the first filtering stage by adding capacitors in parallel with the load resistors, as shown in Fig. 5.4a. Since the RC pole that is formed is passive, it attenuates the out-of-band interfering signals linearly before the active devices of the baseband filter. Consequently, this additional RC pole at the input of the analog baseband filter considerably increases the filter out-of-band linearity compared to an active filter implementation without a passive pole at the filter input, as already discussed in Sections 2.3 and 4.1.2. Reducing the pole frequency is obviously beneficial from the filter out-of-band linearity point of view. However, if the pole frequency is less than or approximately equal to the baseband bandwidth of the desired signal, the pole also attenuates the high-frequency components of the desired signal. This increases the noise contribution from the following baseband stages. As another option, it was shown in Section 4.1.2 that the real pole of an odd-order low-pass filter prototype can be extracted from the filter transfer function and realized with the passive load components of a preceding voltage-mode Gilbert cell mixer. Thus, instead of an additional RC filtering stage being realized at the mixer output, the passive load of the mixer can be used to implement the real pole extracted from the following baseband low-pass filter [19]-[21]. The pole frequency of the extracted real pole can be less than the passband edge frequency of the low-pass filter.

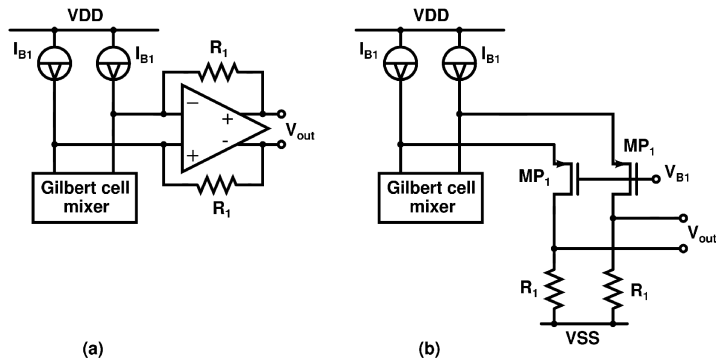


Figure 5.5. Two different alternative ways to implement a low-impedance node at the current-mode mixer-baseband interface: a) the inputs of an opamp or b) folded cascode transistors connected to the mixer output.

In a current-mode mixer-baseband interface, the mixer output current is driven into a low-impedance node. The low-impedance node can simply be implemented by connecting the inputs of an opamp to the mixer output, as shown in Fig. 5.3 and Fig. 5.5a [3], [4], [5], [17]. Alternatively, a low-impedance node can be established by means of folded cascode transistors, as shown in Fig. 5.5b [17], [22]. In an ideal case, owing to the low-impedance node, there is no voltage signal at the mixer output, which

improves the linearity of the mixer [2], [5]. The downconversion mixers of both the multicarrier receiver implementations presented in this chapter have a current-mode output, as was shown in Fig. 5.3.

Let us first review the following linearity analysis from [5] and [17]. A simplified model of the current-mode mixer-baseband interface shown in Fig. 5.3 is shown in Fig. 5.6a. In Fig. 5.6a, the transconductor represents a mixer and the first baseband stage is modeled with a feedback-connected opamp instead of an opamp-RC integrator for the sake of simplicity. The linearity of the feedback-connected opamp shown in Fig. 5.6a can easily be compared to a corresponding baseband structure with a voltage-mode input, shown in Fig. 5.6b. For this comparison, the output signal of the feedback-connected amplifier is approximated using a Taylor series;

$$v_{out}(t) = k_1 v_{in}(t) + k_3 v_3(t)^3, \quad (5.1)$$

where the linear gain is  $k_1$  and  $k_3$  is the third-order non-linear coefficient. The ratio between the third-order non-linear coefficients of the feedback-connected opamp with a current-mode input ( $k_3$ ) and with a voltage-mode input ( $k_3'$ ) can be calculated to be [5], [17]

$$\frac{k_3}{k_3'} \approx \frac{1 + (R_2 / R_1)}{1 + (R_2' / R_1')}, \quad (5.2)$$

when the linear gains of the circuits are assumed to be equal:

$$\frac{k_1}{k_1'} \approx \frac{-gmR_2}{-(R_2' / R_1')} = 1. \quad (5.3)$$

In the case of the current-mode input, the third-order non-linear coefficient ( $k_3$ ) can be diminished without affecting the linear gain ( $k_1$ ) of the amplifier by increasing the resistance value of the mixer biasing resistors ( $R_1$ ) connected between the opamp input and signal ground. Hence, in principle, on the basis of (5.2), a higher linearity can be achieved with the current-mode interface. In practice, there may be additional feedback resistors in the baseband filter, such as  $R_3$ , shown in Fig. 5.3, which limit the achievable improvement in the filter linearity [5], [17].

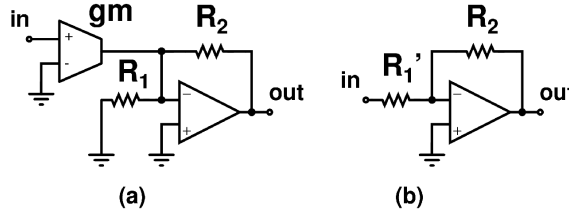


Figure 5.6. Simplified block diagram of a feedback-connected opamp with (a) a current-mode and (b) a voltage-mode input [5] (© 2008 EuMA).

Let us next expand the study. In an IC implementation of the voltage-mode interface, the resistor  $R_1'$  that follows the load of the mixer is typically realized with a voltage-to-current converter. Such converters, like transconductors, tend to be non-linear devices that easily degrade the overall linearity of the analog baseband circuit in which they are employed, especially at low supply voltages. The voltage-to-current converter is depicted as a transconductor with a transconductance of  $gm_i$  in Fig. 5.7. The transconductor with a transconductance of  $gm_{RF}$  represents the transconductance stage and  $Z_L(\omega)$  the load of the mixer, respectively. The load impedance of the mixer can be written as

$$Z_L(\omega) = \frac{R_L}{1 + j\omega R_L C_L}, \quad (5.4)$$

where  $R_L$  represents the mixer load resistor and  $C_L$  is a capacitor connected in parallel with the load resistor, as shown in Fig. 5.4a. In the case of Fig. 5.4b and 5.4c,  $C_L$  represents a parasitic capacitance that is always present at the mixer output. Similarly to (5.1), let us approximate the output signal of the feedback-connected baseband amplifier  $A_2$  with a Taylor series as

$$v_{out} = k_1' (v_1 + \alpha_3' v_1^3), \quad (5.5)$$

where the third-order non-linear coefficient  $k_3'$  of the feedback-connected amplifier with a voltage-mode input is now written by means of its linear gain  $k_1'$  and a relative third-order non-linear coefficient  $\alpha_3'$  as  $k_3' = k_1' \cdot \alpha_3'$ . Similar notation will be used later on in this thesis, in Section 6.6. It can be assumed that the non-linearity of both the transconductor (i.e. its transconductance  $gm_i$ ) and the amplifier  $A_1$  of the feedback-connected amplifier  $A_2$  are referred to the non-linear gain of  $A_2$ . In addition, it should be repeated that the frequency dependency of  $k_1'$  is omitted in this study for the sake of simplicity. A signal consisting of two out-of-band intermodulation test tones can be represented as

$$v_{in} = A[\cos(\omega_1 t) + \cos(\omega_2 t)]. \quad (5.6)$$

When this signal is applied to the input of the circuit in Fig. 5.7, the output signal of the amplifier  $A_2$  becomes

$$v_{out} = -gm_{RF} Z_L(\omega_1) k_1' A \cos(\omega_1 t) + \frac{3}{4} k_1' \alpha_3' [(-gm_{RF}) Z_L(\omega_1) A]^3 \cos[(2\omega_1 - \omega_2)t], \quad (5.7)$$

when only the other fundamental signal tone and third-order non-linear component are of concern.

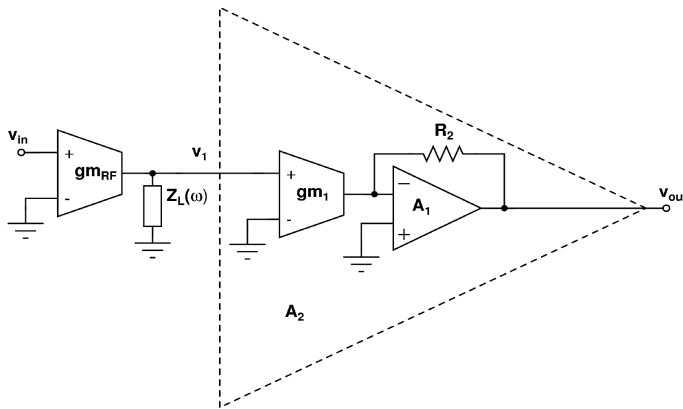


Figure 5.7. Block diagram of a more realistic voltage-mode mixer-baseband interface.

If the same two-tone test signal is applied to the input of the circuit shown in Fig. 5.6a, its output signal, including only the frequency components of interest, can be expressed as

$$v_{out} = k_1 A \cos(\omega_1 t) + \frac{3}{4} k_1 \alpha_3'' A^3 \cos[(2\omega_1 - \omega_2)t]. \quad (5.8)$$

The output signal of the circuits shown in Fig. 5.7 and 5.6a for a small single-tone in-band input signal, represented as

$$v_{in} = B \cos(\omega_3 t), \quad (5.9)$$

can be written as



$$v_{out} = -gm_{RF}Z_L(\omega_3)k_1'B \cos(\omega_3 t) \quad (5.10)$$

and

$$v_{out} = k_1 B \cos(\omega_3 t), \quad (5.11)$$

respectively. On the basis of (5.10) and (5.7), the signal-to-distortion ratio at the output of the circuit shown in Fig. 5.7 can be expressed as

$$\begin{aligned} \frac{S_{out,in-band}}{D_{out,imd3}} &= \frac{|-gm_{RF}Z_L(\omega_3)k_1'B|}{\left| (3/4)k_1'\alpha_3' [(-gm_{RF}Z_L(\omega_1)A)]^3 \right|} \\ &= \frac{4}{3} \frac{R_1}{gm_{RF}^2 |Z_L^3(\omega_1)|} \frac{B}{\alpha_3' A^3}, \end{aligned} \quad (5.12)$$

where it is approximated that  $Z_L(\omega_b) \approx R_i$  in the in-band (i.e. close to the DC). Correspondingly, on the basis of (5.11) and (5.8), the signal-to-distortion ratio at the output of the circuit shown in Fig. 5.6a can be written as

$$\frac{S_{out,in-band}}{D_{out,imd3}} = \frac{|k_1 B|}{\left| (3/4)k_1 \alpha_3'' A^3 \right|} = \frac{4}{3} \frac{1}{\alpha_3''} \frac{B}{A^3}. \quad (5.13)$$

The signal-to-distortion ratios at the output of the first stage of a baseband circuit in the case of a voltage-mode ( $SDR_v$ ) and a current-mode ( $SDR_i$ ) mixer-baseband interface can now be compared with each other. The following result is obtained:

$$\frac{SDR_v}{SDR_i} = \frac{\alpha_3''}{\alpha_3'} \frac{R_1}{gm_{RF}^2 |Z_L^3(\omega_1)|}. \quad (5.14)$$

On the basis of (5.2), in the case of the current-mode input, the third-order non-linear coefficient and, thus,  $\alpha_3'$ , can be diminished by increasing the mixer biasing resistance ( $R_i$ ), as stated above. Conversely, the non-linear voltage-to-converter needed in the voltage-mode mixer-baseband interface easily increases the value of the relative third-order non-linear coefficient  $\alpha_3''$ . However, the out-of-band attenuation provided by the RC pole at the voltage-mode mixer-baseband interface may significantly compensate for the impact of  $\alpha_3''$  on the signal-to-distortion ratio. It may be concluded that the overall performance, including the power dissipation,

and the application being targeted determine whether it is preferable to use a voltage-mode or a current-mode mixer-baseband interface. Moreover, it is likely that the choice between the two alternatives is not a straightforward one. However, it seems that in the recent receiver publications, the trend is towards current-mode mixer-baseband interface. In both multicarrier receivers that are under consideration in this thesis, a current-mode mixer-baseband interface was chosen because it significantly increased the linearity of the mixers. As a consequence, a high current consumption was needed in the baseband filters to meet the stringent linearity requirements set by the design choice made at the system level.

### 5.3 Circuit design

The circuit design of both evolution versions of the continuous-time opamp-RC low-pass filters is described in this section. Since the low-pass filters was required to provide anti-aliasing filtering for the ADCs together with the RF pre-select filter, a fourth-order Chebyshev prototype with a 0.1-dB passband ripple was selected for them. The  $-3$ -dB bandwidth of the first low-pass filter version is fixed to 10 MHz but the second filter version can be programmed to four different bandwidths: 2.5 MHz, 5 MHz, 7.5 MHz, and 10 MHz. Both filters were designed to drive a high-resolution Nyquist-rate ADC. Such an ADC is capable of handling high-frequency signals with a wide dynamic range. To achieve a sufficient attenuation at the sampling frequency of the ADC, a transmission zero was implemented at 65 MHz in both filter versions. In practice, the transmission zero was added into the Chebyshev prototype filter, as described in Chapter 4. The transmission zero enables the filter order to be reduced from five to four, leading to lower in-band noise. Considering the second filter version, the transmission zero is utilized only in the case of the 10-MHz bandwidth. It is switched off in the other three filter bandwidths, because the attenuation in the filter stopband is adequate without it.

The leapfrog topology, shown in Fig. 5.8, was chosen because of its low sensitivity to component value mismatches. The voltage gain of the first filter version is fixed. Conversely, the voltage gain of the second version can be digitally altered between three different gain settings with 6-dB steps. The gain steps were implemented in the second stage of the filter (R3 and R4 in Fig. 5.8) to compensate for possible process variations (i.e. gain variation) of the RF front-end. A drawback of this compensation is that the non-linear on-resistance of the NMOS switches connected in series with the poly-resistors of the resistor matrices R3 and R4 degrades the linearity of the second filter version. Thus, attention needs to be paid to the design of

the switches in the capacitor and resistor matrices of a filter in order to minimize the linearity degradation in the filter as a result of the nonlinearities of the switches. Typically, in the capacitor and resistor matrices, the switches are placed at the input of the opamp, as was shown in Fig. 3.2. This is because the voltage swing is much lower at the input of the opamp as a result of the virtual ground compared to the opamp output. In addition, a part of the parasitic capacitances associated with the switches is then connected to the virtual ground. When the time constants formed by the on-resistance of the switches connected in series with the capacitors in a capacitor matrix are being considered, the usual practice is to design the switches with binary-weighted sizes according to the binary-weighted capacitors in such a way that the time constants formed are independent of the digital control word.

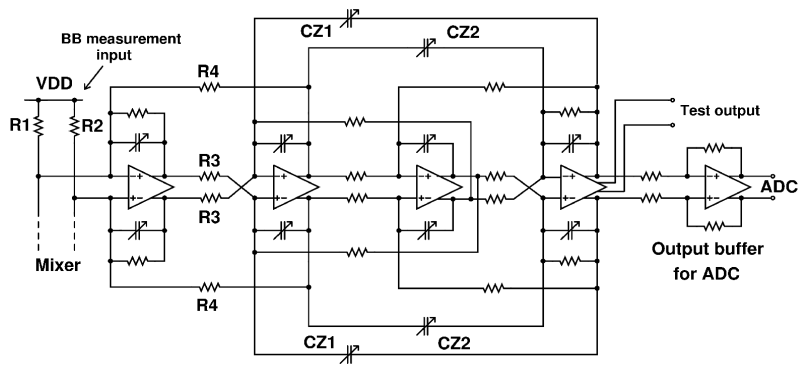


Figure 5.8. Fourth-order low-pass filter implemented with the ADC buffer [3] (© 2006 IEEE).

In both filter implementations, the resistors R1 and R2 were connected to the supply voltage when the filter was embedded into the receiver. Correspondingly, for test purposes, the signal was driven through these resistors and the filter input was externally matched to 50  $\Omega$ .

### 5.3.1 Operational amplifier

There are a number of different operational amplifier topologies with different modifications that have been presented and published in the literature. Therefore, this section concentrates exclusively on the two-stage modified Miller-compensated operational amplifier (opamp) designed and implemented in this work. The schematic of the opamp is shown in Fig. 5.9. To minimize the design effort, the same opamp was used in the ADC buffer and in the first three filter stages. As can be seen in Fig. 5.8, the bipolar

transistor option of the BiCMOS technology adopted in the receiver design was also utilized in the opamp design. The BiCMOS opamp includes separate common-mode feedbacks for both opamp stages. The separate common-mode feedbacks were implemented to achieve fast settling, which is required in the ADC buffer when driving the input sampling capacitors of the ADC. The common-mode feedback of the first opamp stage is formed by connecting the collector of the transistor Q1 to the base of the transistor Q3 and the collector of Q2 to the base of Q4, respectively. In the second opamp stage, the common-mode feedback with resistive and capacitive sensing is performed locally by the transistors Q7 and Q8. In order to realize a well-defined common-mode output voltage in the absence of high loop gain, a replica circuit, together with a differential stage, was used to set the bias voltages for Q7 and Q8. The bias voltages Vb1-Vb4 in Fig. 5.9 come from PMOS current mirrors. Both the ADC buffer opamp and the filter opamp need a high-gain bandwidth product (GBW). The ADC buffer opamp requires a high GBW because of the high sampling rate of the ADC. In addition to the high open-loop DC gain, the filter opamp requires a high GBW in order to achieve high linearity over a wide bandwidth and an accurate filter frequency response.

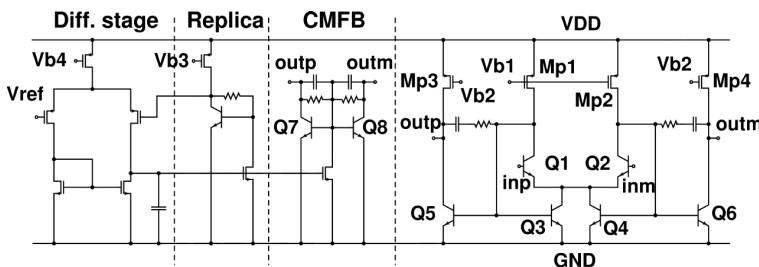


Figure 5.9. Schematic of the opamp that was implemented and utilized in the first three filter stages and in the output buffer (with permission from Springer Science+Business Media: [2], Fig. 5, © 2007 Springer Science+Business Media).

The relative transfer function magnitude error of an LC ladder filter can be approximated with (3.8), presented in Chapter 3. In active filters which are based on signal flow graph (SFG) LC ladder simulation, the inductor and capacitor  $Q_s$  of the passive prototype have a one-to-one correspondence with the  $Q$ -factor of the integrators that are used to simulate them. In the opamp-RC filters of this work, the most challenging requirement for the  $Q$ -factor of the integrators occurs when the filter  $-3$ -dB bandwidth is 10 MHz. If the relative transfer function magnitude error at the passband edge frequency (i.e. at 8.2 MHz) of a fourth-order Chebyshev with a 0.1-dB passband ripple is required to be smaller than 0.2 dB, the  $Q$ -

factor of the integrators has to be at least 191. On the basis of (3.4), the inverse Q-factor of an opamp-RC integrator can be presented as

$$\frac{1}{Q_{\text{int}}(\omega_{\text{int}})} \approx \frac{1}{A_{DC}} - \frac{\omega_{\text{int}}}{\omega_{GBW}}, \quad (5.15)$$

where  $\omega_{\text{int}}$  and  $\omega_{GBW}$  are the unity-gain frequency of the integrator and the opamp, respectively, and  $A_{DC}$  is the open-loop DC gain of the opamp. From (5.15), the simulated 2-GHz GBW and 60-dB open-loop DC gain of the opamps result in an adequate integrator Q-factor of 250. On the basis of the well-known feedback theory, the distortion voltage at the output of an amplifier is reduced by a factor equal to the loop gain. To obtain a high loop gain over a wide bandwidth, the opamp is required to have a high GBW, as discussed in Section 3.2. In the opamp-RC filters of this work, the most challenging linearity requirement occurs when the filter has the widest 10-MHz bandwidth, as discussed in Section 5.1.2. Considering the second filter version, the simulated out-of-band IIP<sub>3</sub> of the whole filter with the opamps having a 2-GHz GBW is +19 dBV. This is actually dominated by the distortion of the switches in the resistor matrices. The simulation result corresponds to the value calculated as an example in Section 5.1.2.

The opamp designed in this work has a potential start-up problem. During the start-up, the bias currents fed by the transistors Mp1 and Mp2 can flow to the bases of the transistors Q3–Q6. Therefore, no DC current flows through the transistors Q1 and Q2 and the first opamp stage does not bias correctly. In addition, as a result of the large base bias current of Q5 and Q6, the DC common-mode voltage at the opamp output is close to 0 V, instead of 1.2 V, as is desired. The start-up problem was solved by switching on the bias current of the output stage before the input stage. The delay was implemented with an RC time constant in the gate of Mp1 and Mp2.

A single opamp consumes 17 mA, which is acceptable because of the BS application. A high ratio of the DC and signal currents in the opamp output stage is used to achieve high linearity. Hence, in this work, the high current consumption of the opamps is justified. The bipolar input transistors Q1 and Q2 were designed to have a high transconductance, while the PMOS load transistors Mp1 and Mp2 were designed to have a low transconductance in order to reduce the noise contribution of the opamps in the filter. According to simulations, the total noise contribution of the opamps to the filter noise in both designs is only 9%.

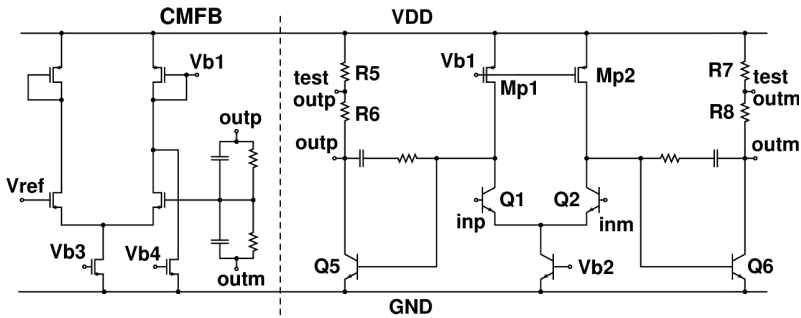


Figure 5.10. Schematic of the fourth opamp, in which the filter test output is implemented (with permission from Springer Science+Business Media: [2], Fig. 6, © 2007 Springer Science+Business Media).

To implement a resistive high-linearity test output (Fig. 5.8), which is matched to 50- $\Omega$  measurement equipment, the transistors Mp3 and Mp4 were replaced with four resistors R5-R8 in the fourth filter opamp, as shown in Fig. 5.10. In addition, a conventional common-mode feedback circuit is utilized in this opamp, since the fast settling required in the ADC buffer is not critical in the filter opamps.

### 5.3.2 Frequency response tuning

It was discussed in Chapter 3 that in opamp-RC filters, it is a common practice to tune the integrator time constants and hence the filter frequency response with capacitor matrices. In addition to that, in the second filter version of this work, capacitor matrices were used for the tuning in order to obtain a constant in-band noise density (Fig. 5.2) and thus, a constant signal-to-noise ratio regardless of the filter bandwidth. When the bandwidth of the second filter version is reduced from 10 MHz to 2.5 MHz, the bandwidths of all the integrators are also reduced by the same factor of four. One integrator can be considered as a single-pole low-pass filter and therefore, its integrated output noise is  $kT/C$ . This result includes the assumption that the noise contribution of the operational amplifier is low compared to the  $kT/C$  noise. Let us denote the integrated output noise of one integrator as  $kT/C_o$  in the case of the 10-MHz filter bandwidth. When the filter bandwidth is tuned from 10 MHz to 2.5 MHz only by capacitor matrices, the capacitances of the filter capacitors are increased by a factor of four and thus the integrated output noise of one integrator becomes  $kT/(4C_o)$ . The integrated output noise is four times lower in the case of a bandwidth that is four times narrower and thus the in-band noise density remains constant.

In principle, all four filter bandwidths of the second filter version could be implemented with four parallel 5-bit capacitor matrices. However, this would lead to a large chip area. In this work, the number of unit capacitors was minimized by merging the separate matrices. In the final design, the frequency response is tuned with 10-bit binary-weighted switched-capacitor matrices, as shown in Fig. 5.11. The filter bandwidth is selected by changing the fixed capacitance. The fixed capacitor  $C_0$  corresponds to the 10-MHz bandwidth of the filter. The fixed capacitance is increased and hence the filter bandwidth is reduced by switching on the band-select capacitors  $C_n$  in parallel with  $C_0$ . Thus three bits are used for the bandwidth selection. The frequency response is tuned with the binary-weighted capacitors  $C_k$  [23]. Depending on the filter bandwidth, five of the remaining seven bits are selected for the 5-bit frequency response tuning.

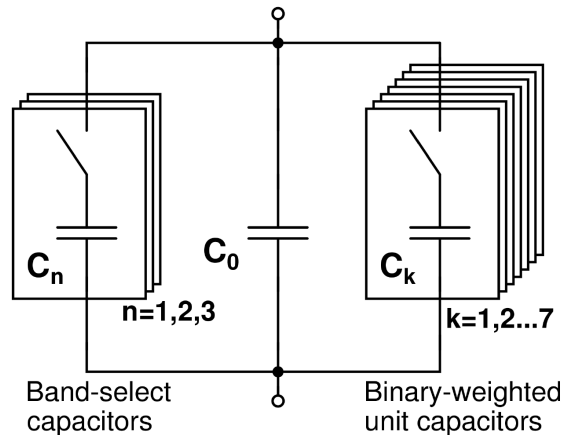


Figure 5.11. Simplified schematic of the 10-bit capacitor matrix (with permission from Springer Science+Business Media: [2], Fig. 3, © 2007 Springer Science+Business Media).

### 5.3.2.1 Transmission zero and capacitor CZ

The first active opamp-RC leapfrog filter version was synthesized from its fourth-order LC prototype filter counterpart via the SFG method. As a result of the SFG synthesis, the first opamp-RC version includes two capacitors,  $C_{Z1}$  and  $C_{Z2}$ , which implement the transmission zero, as shown in Fig. 5.8. Their capacitance values are 68 fF and 135 fF, respectively [3]. However, later on it was found that only one  $C_Z$  is needed to generate the transmission zero. Therefore, in the second filter version, only  $C_{Z2}$  was employed to implement the transmission zero, and the smaller one,  $C_{Z1}$ , was removed. The transmission zero is switched on only in the case of the 10-MHz filter bandwidth in the second filter version, as already mentioned.

The notch frequency of the transmission zero must be tuned with the same accuracy as the poles of the filter with the 10-MHz bandwidth in order to meet the anti-aliasing requirements. Thus, capacitor  $C_Z$  includes a 5-bit control despite to their low capacitance value. The schematic of the capacitor matrix  $C_Z$  is shown in Fig. 5.12. It is original work in this thesis. The binary-weighted unit capacitors are implemented using T-connection because of the small capacitance value and transistor  $Mn1$  in T-connection is implemented to avoid charge accumulation. The equivalent capacitance value of the unit capacitor is  $C_x / (2+K_i)$  [3]. Hence, to meet the tuning requirements, the smallest equivalent capacitance values of the unit capacitor are 1.8 fF in  $C_{Z1}$  and 3.6 fF in  $C_{Z2}$ . The implementation of the small unit capacitors demanded careful layout design in order to minimize the parasitic capacitances.

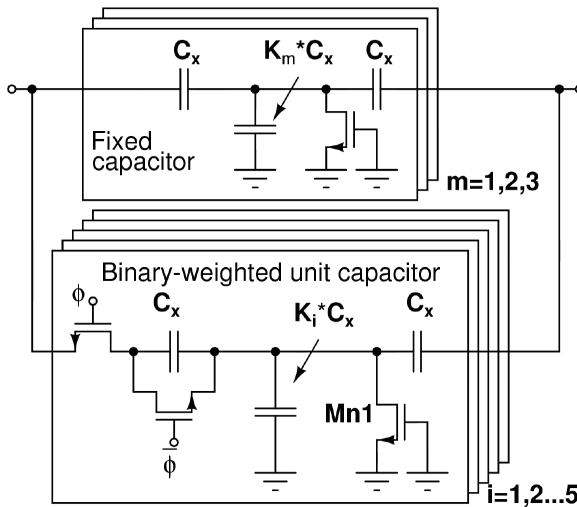


Figure 5.12. Schematic of capacitor matrix  $C_Z$  (with permission from Springer Science+Business Media: [2], Fig. 4, © 2007 Springer Science+Business Media).

### 5.3.3 Other issues

To reduce the noise, the gain should be placed as close to the filter input as possible. However, in these designs, the gain had to be distributed between the first three filter stages to avoid the saturation of the first two filter stages as a result of the out-of-channel blocking and interfering signals described in Section 5.1.2. The simulated voltage gains of the filter stages are 2.3 dB, 8.3 dB, 1.3 dB, and 0 dB in the first filter version and 9.4 dB, 8.3 dB, 1.3 dB, and 0 dB in the second filter version, when the signal is driven through resistors  $R_1$  and  $R_2$ . The noise of the polysilicon resistors dominates the in-band noise of the filter, regardless of the bandwidth of the



filter. The dominant noise contribution arises from the biasing resistors R1 and R2. However, resistors are less noisy than PMOS current sources and, therefore, resistive biasing is used for the mixer.

Because of the low voltage gain of the filter, the DC offsets at the input of the baseband circuit do not saturate the filter. Thus, no DC offset compensation is implemented in this design. However, the DC offset at the filter output reduces the available dynamic range of the filter and the following ADC. As presented in [4], the measured DC offset at the filter output is around 10 mV, which has no practical effect on the performance of the receiver.

#### 5.4 Experimental circuit I: WCDMA multicarrier receiver for base-station applications

The multicarrier receiver IC described in this section and shown in Fig. 5.13 receives four adjacent WCDMA channels simultaneously in order to reduce the component count of a base-station. The receiver uses a low-IF architecture and it is fabricated in a 0.25- $\mu\text{m}$  SiGe BiCMOS process to meet the high performance requirements set by the base-station application. The receiver consists of a dual-input LNA, quadrature downconversion mixers, an LO divider, IIP2 calibration circuits, and two 10-MHz low-pass filters with ADC buffers. The receiver noise figures, measured over the downconverted WCDMA channels centered at the 2.5-MHz and 7.5-MHz intermediate frequencies, are 3.0 dB and 2.6 dB, respectively. The receiver achieves 47 dB of voltage gain and -12 dBm out-of-band IIP3. The circuit consumes 535 mW from a 2.5-V supply. This section is based on [3] and [1].

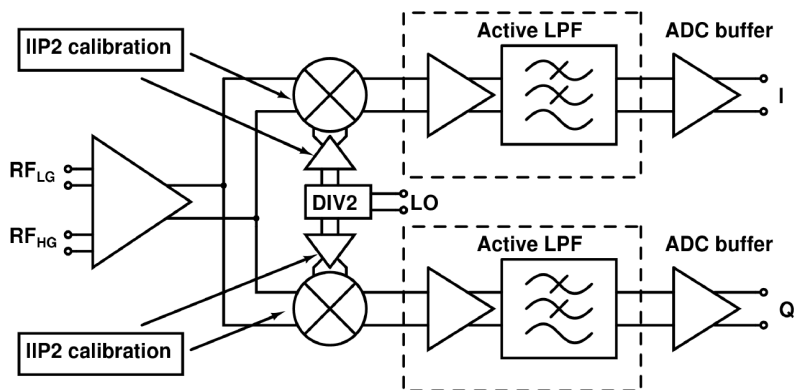


Figure 5.13. Block diagram of the multicarrier receiver [3] (© 2006 IEEE).

### 5.4.1 RF front-end

The LNA shown in Fig. 5.14 includes two inductively degenerated common-emitter cores with cascode transistors for high- (HG) and low-gain (LG) modes. In the high-gain mode, the input of the receiver can be connected to the pre-select filter. Correspondingly, in the low-gain mode, an off-chip LNA with a high dynamic range can be connected between the antenna and the receiver. By using separate cores, the need for gain setting switches in the signal path, which could cause the LNA performance to deteriorate, is avoided. Thus, the two different cores can be optimized separately and a low NF is achieved in both modes. The load of the LNA is a resonator tuned at 2 GHz and it combines the two signal paths in order to avoid an additional on-chip inductor and dual-input mixers. The measured gain difference between the two modes is 14.8 dB. The simulated NF in HG and LG modes is 0.9 dB and 3.2 dB, respectively.

The downconversion mixer, shown in Fig. 5.15, is based on the Gilbert cell topology. The mixer includes an inductively degenerated NMOS input stage, bipolar switches, and current boosting for the input stage. The mixer drives the virtual ground of the first operational amplifier (opamp) of the 10-MHz low-pass filter. The bias currents of the mixer are controlled with 6-bit current D/A converters (IDAC) to improve the IIP<sub>2</sub> of the receiver. In addition to the IIP<sub>2</sub> calibration circuits in the mixer input stage, similar 6-bit IDAC IIP<sub>2</sub> calibration circuits were also implemented in the LO buffers. These tuning circuits can be used separately to improve the receiver IIP<sub>2</sub>. The output of the mixer is connected to the input of the first opamp of the lowpass filter, which acts as a low-impedance load for the mixer because of its virtual ground. The voltage swing at the output of the mixer is thus very small. Therefore, the output signal does not modulate the collector voltages of the switches, thus improving the IIP<sub>3</sub> of the mixer compared to a mixer with a high-impedance load. The resistors R<sub>1</sub> and R<sub>2</sub> between the mixer output and the supply voltage are used for biasing and setting the common-mode level to 1.2 V. The simulated effective transconductance and IIP<sub>3</sub> of the mixer are 5.9 mS and +15 dBm, respectively. According to simulations, the inductive degeneration of the input stage, the optimized bias current of the switching stage, and the low-impedance load of the mixer improve the overall IIP<sub>3</sub> by 7 dB compared to a voltage-mode Gilbert cell mixer, which has the same current consumption and appropriate voltage headrooms for all transistors.

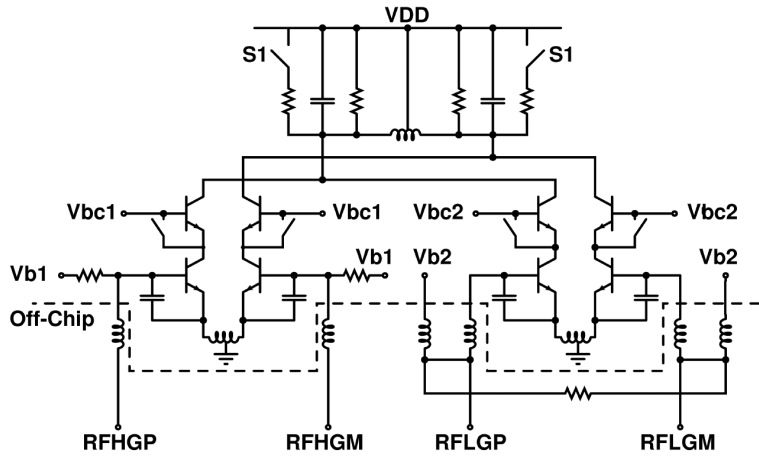


Figure 5.14. Low-noise amplifier [3] (© 2006 IEEE).

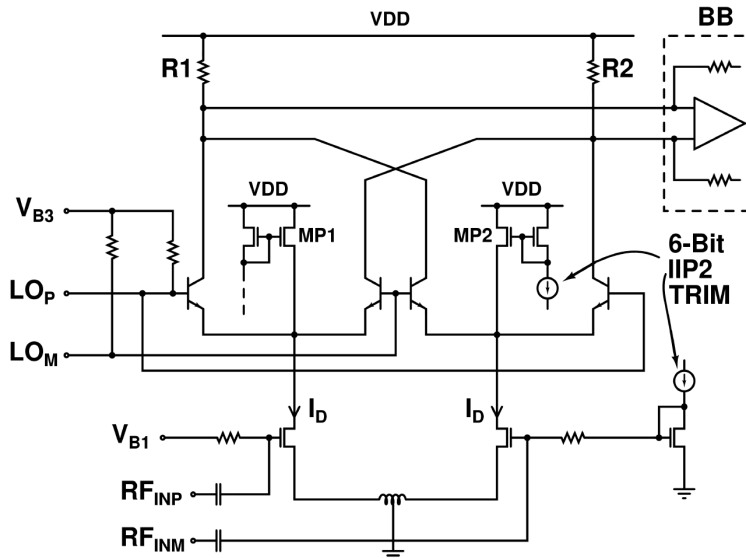


Figure 5.15. Downconversion mixer [3] (© 2006 IEEE).

#### 5.4.2 Experimental results of receiver

The receiver was fabricated in an STMicroelectronics 0.25- $\mu\text{m}$  SiGe BiCMOS process and the chips were bonded directly onto a printed circuit board (PCB). A micrograph of the receiver is shown in Fig. 5.16. The measurements were performed using the test output of the low-pass filter, except the voltage gain, which was measured from the output of the ADC buffer. Fig. 5.17 shows the measured and simulated voltage gains of the receiver as a function of the LO frequency in the HG and LG modes. The simulated gain in both gain modes is scaled to match the measurement

results at 2 GHz. The measured  $-1$ -dB gain bandwidths, which correspond well to the simulations, are 280 MHz and 720 MHz in the HG and LG modes, respectively. The use of the dual-input LNA leads to a challenging PCB design. However, a sufficient input matching of better than  $-10$  dB is achieved within the  $-1$ -dB gain bandwidths.

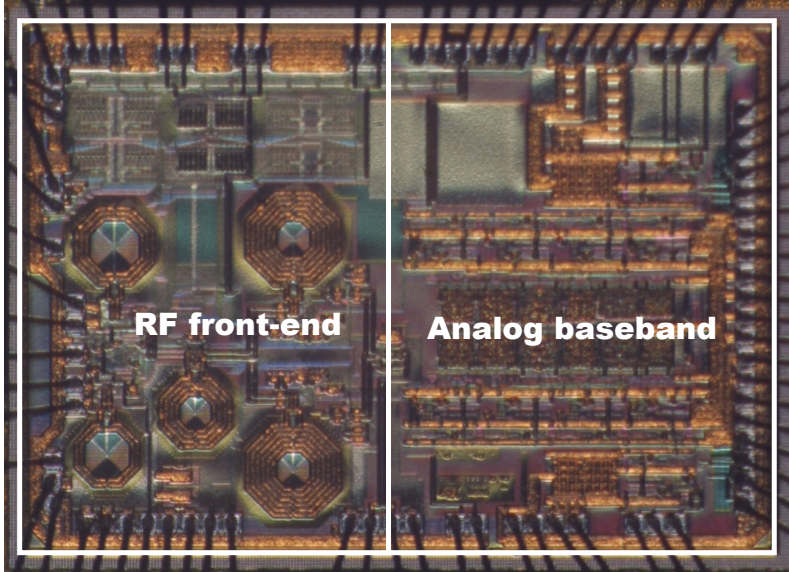


Figure 5.16. Chip micrograph of the multicarrier receiver [3] (© 2006 IEEE).

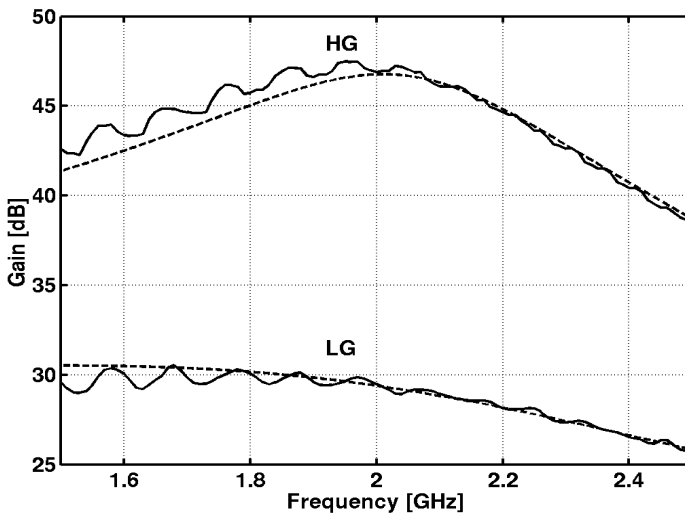


Figure 5.17. Measured (solid) and simulated (dashed) voltage gains of the receiver as a function of the LO frequency in high- and low-gain modes [3] (© 2006 IEEE).

The NF of the low-IF multicarrier receiver was measured within the two channels centered at 2.5 MHz and 7.5 MHz by integrating the output noise from the 4.6848-MHz band (1.22\*3.84 MHz) for both channels. The coefficient 1.22 corresponds to the unity-gain bandwidth of a root-raised-cosine filter with a roll-off factor of 0.22, which is used in the digital back-end of WCDMA receivers [17], [24], [25]. A complete receiver which includes the digital back-end would remove the LNA noise from the image band. Since this receiver does not include the digital back-end, the NF of the LNA has to be measured in order to be able to calculate the NF of the receiver. The NF of the LNA is

$$NF_{LNA} = 10 \log \left[ \frac{V_{out,nom}^2 - V_{out,noLNA}^2}{2kTBWR_S A_{V,RX}^2} \right], \quad (5.16)$$

where  $BW$  is the channel bandwidth of 4.6848 MHz,  $V_{out,nom}$  is the total integrated output noise when the LNA is biased on,  $V_{out,noLNA}$  is the total integrated output noise when the LNA is biased off,  $k$  is the Boltzmann's constant,  $T$  is the temperature,  $R_S$  is the source resistance (100  $\Omega$  because of a balanced input), and  $A_{V,RX}$  is the voltage gain of the receiver. The worst-case measured NFs of the LNA are 1.0 dB and 3.5 dB in the HG and LG settings, respectively, which match well with the simulation results given in Section 5.4.1. The NF of the low-IF NF can be calculated as

$$NF_{Low-IF} = 10 \log \left[ 10^{NF_{LNA}/10} + \frac{V_{out,noLNA}^2}{kTBWR_S A_{V,RX}^2} \right]. \quad (5.17)$$

The NF of each sample was calculated by using the integrated output noise averaged from several measurements. The worst-case NF results are collected in Table 5.2, along with the other receiver parameters. The difference in the NF between the channels centered at 2.5 MHz and 7.5 MHz is due to the flicker noise, which increases the noise in the lower channel. As a comparison, if this receiver were used as a DCR with a signal band equal to twice the equivalent noise bandwidth of the lowpass filter, the worst-case NF would be 1.8 dB.

The IIP<sub>3</sub> of the receiver was measured using different test tones. The most stringent is Case 2 shown in Fig. 5.2, where the downconverted signals are located at 11 MHz and 13.4 MHz. When the LO is at 4.0 GHz and the test signals are at 2.011 GHz and 2.0134 GHz, the IIP<sub>3</sub> of the receiver in the HG and LG modes is -12 dBm and -1 dBm, respectively, and it is limited by the RF front-end.

The compression of an in-band signal was measured in a blocker test. The LO is at 4.0 GHz, the reference signal at 2.005 GHz, and the blocker at 2.0102 GHz. The in-band signal compressed by 1 dB when the input power of the blocker was  $-34$  dBm in HG mode and  $-23$  dBm in LG mode, leaving more than 10 dB of headroom to the specification [14]. In this case, the linearity is limited by the low-pass filter. With the use of an out-of-band blocker at 2.05 GHz, the compression is caused by the RF front-end and the measured values are  $-24$  dBm and  $-15$  dBm in the HG and LG modes, respectively.

Table 5.2. Summarized performance of the receiver [3] (© 2006 IEEE).

	High gain	Low gain	
$A_v$ @ 2GHz	46.9	32.1	dB
S11	-10	-16	dB
NF*	3.0/2.6	13.7/12.2	dB
NF (DCR)	< 1.8	na	dB
IIP3**	-12	-1	dBm
IIP2***	> 24	> 44	dBm
ICP @ 10.2-MHz blocker	-34	-23	dBm
Filter -3-dB frequency	9.8	9.8	MHz
LO @ RF input	< -90	< -90	dBm
I <sub>dd</sub>	214	208	mA
V <sub>dd</sub>	2.5		V
Chip area	5.7		mm <sup>2</sup>
Technology	0.25- $\mu$ m SiGe BiCMOS		

- \* For channels centered at 2.5 MHz and 7.5 MHz
- \*\* Downconverted tones at 11 MHz and 13.4 MHz
- \*\*\* Nominal

### 5.4.3 Experimental results of low-pass filter

A micrograph of the low-pass filter with the ADC buffer is shown in Fig. 5.18. The active silicon area of the low-pass filter, including the ADC buffer, is 0.90 mm<sup>2</sup>. The measurement results were obtained from the test output of the low-pass filter, except the voltage gain, which was measured from the ADC buffer output. The test signals were fed into the filter through the biasing resistors R1 and R2 (Fig. 5.8).

The measured and simulated frequency responses of the channel-select filter, which are normalized to the ideal Chebyshev response at 100 kHz, with minimum, maximum, and typical tuning codes, are shown in Fig. 5.19. A measured response is a combination of separate curves, which are measured at different power levels to expand the dynamic range of the

measurement. The measured  $-3$ -dB frequency with the typical tuning code is 9.8 MHz. The measured responses match the simulated ones well and the implemented transmission zero moves correctly with different codes. In the response, only a slight difference is observed at the passband edge, which is at least partially due to unmodeled routing resistance in the capacitor matrices. The measured and simulated input-referred noise voltages from 10 kHz to 20 MHz are shown in Fig. 5.20. The measured integrated input-referred noise from 10 kHz to 20 MHz is 35.2  $\mu$ Vrms, which corresponds to an input-referred noise density of 11.2 nV/ $\sqrt{\text{Hz}}$  with a  $-3$ -dB bandwidth of 9.8 MHz.

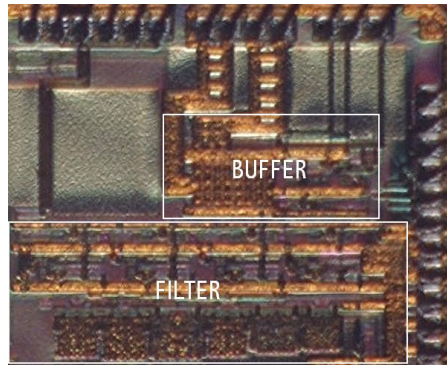


Figure 5.18. Chip micrograph of the filter [1] (© 2006 IEEE).

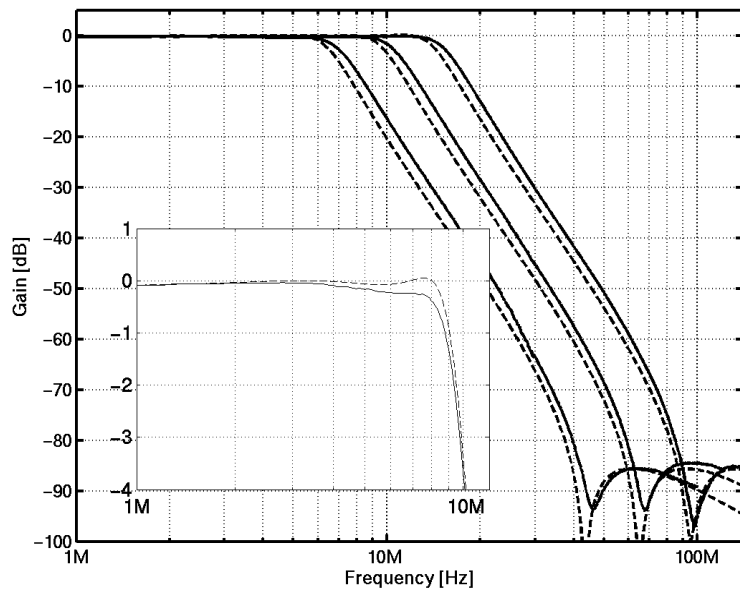


Figure 5.19. Measured (solid) and simulated (dashed) frequency responses of the filter [1] (© 2006 IEEE).

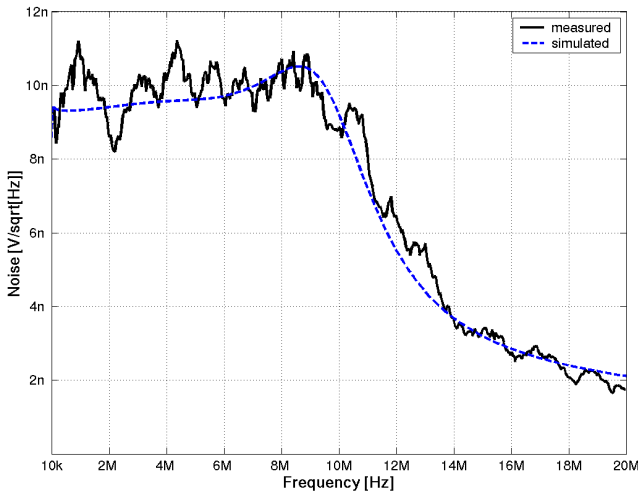


Figure 5.20. Measured (solid) and simulated (dashed) input-referred noise [1] (© 2006 IEEE).

External passive low-pass and high-pass filters were used to minimize the IMD3 caused by the measurement setup itself (for example signal generators). The in-band IIP3 was measured with 4.5-MHz and 8.5-MHz test signals and the out-of-band IIP3 with 11-MHz and 20.5-MHz test signals. As shown in Fig. 5.21, the measured in-band and out-of-band IIP3 of the filter are +25 dBV and +37 dBV, respectively. The measured current consumption of the filter, including the ADC buffer, is 87 mA. The measured performance results are collected in Table 5.3.

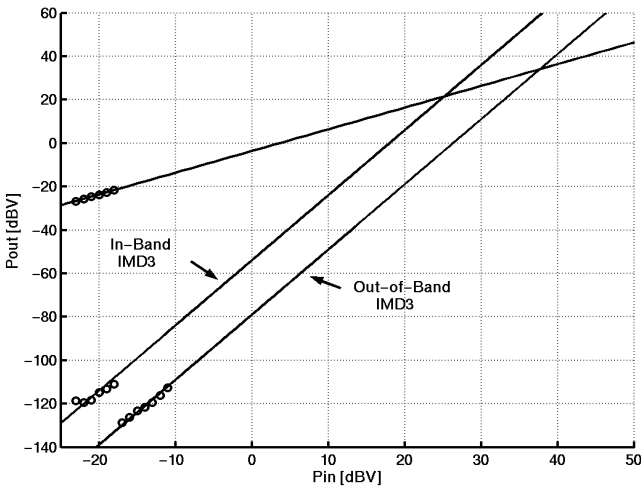


Figure 5.21. Measured in-band (dashed) and out-of-band (solid) linearities [1] (© 2006 IEEE).



Table 5.3. Performance summary [1] (© 2006 IEEE).

Technology	0.25- $\mu$ m SiGe BiCMOS
Supply voltage	2.5 V
Filter order	4
Voltage gain *)	11 dB
-3-dB frequency	9.8 MHz
Input-referred noise **)	35.2 $\mu$ V <sub>RMS</sub>
Input-referred noise density ***)	11.2 nV/ $\sqrt$ Hz
IIP3 (in-band)	+25 dBV
IIP3 (out-of-band)	+37 dBV
In-band SFDR	+76 dB
Current consumption *)	87 mA

\*) Including unity-gain ADC buffer

\*\*) Integrated from 10 kHz...20 MHz

\*\*\*) 9.8-MHz bandwidth used

## 5.5 Experimental circuit II: A 1-to-4 channel receiver for WCDMA base-station applications

A base-station receiver which is capable of receiving from one to four adjacent WCDMA channels is described in this section. The multicarrier receiver uses either a direct-conversion or low-IF topology, depending on the number of channels received. If two or four channels are received, it uses the low-IF architecture and if it is used to receive one or three channels, it uses direct conversion for the center channel and low-IF for other channels. The receiver is designed to operate in the frequency bands I-III determined in the 3GPP specifications, i.e. between 1.7 GHz and 2.0 GHz, as shown in Table 2.1 in Chapter 2. The receiver is designed to drive high-resolution Nyquist-rate A/D converters. The low-IF NF is 2.7 / 3.0 dB for the channels centered at 7.5 MHz and 2.5 MHz, respectively. The measured IIP<sub>3</sub> of the receiver varies from -10 dBm to -8 dBm, depending on the number of channels received. The receiver is fabricated in a 0.25- $\mu$ m SiGe BiCMOS process. The power consumption is 542.5 mW from a 2.5-V supply. This section is based on [4] and [2].

The block diagram of the receiver, consisting of an LNA, I/Q downconversion mixers, an LO generation circuit, and two adjustable low-pass filters with ADC buffers, is shown in Fig. 5.22. The receiver includes two gain settings in the RF front-end. It can be connected directly to the antenna in the high-gain (HG) mode or a separate LNA can be used prior to the receiver in the low-gain (LG) mode. Compared to the first multicarrier receiver implementation described in Section 5.4, this receiver includes the capability to alter the number of channels received with the adjustable low-

pass filters, and single-input operation using a wideband LNA covering the WCDMA frequency bands I-III. In addition, combined degeneration inductance in the I/Q mixers reduces the chip area without performance degradation. In the HG mode, the IIP<sub>3</sub> of the RF front-end is improved by 4 dB without any deterioration of the noise performance. In the LG mode, the dynamic range of the receiver is improved and the LNA does not require any external components, as in the first multicarrier receiver implementation.

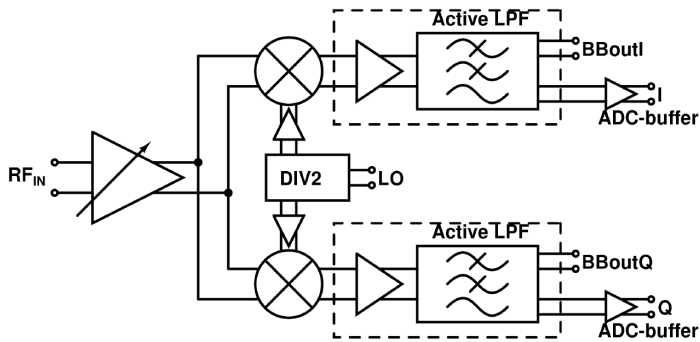


Figure 5.22. Block diagram of the receiver [4] (© 2006 IEEE).

### 5.5.1 RF front-end

A fully differential LNA, shown in Fig. 5.23, is based on the inductively degenerated common-emitter topology and it includes two gain settings. In the HG mode, the main design goal was to minimize the NF. Correspondingly, in the LG mode, a high IIP<sub>3</sub> was the main design criterion. As a comparison, in the first multicarrier receiver implementation, the LNA uses two parallel LNA cores to meet these requirements. In this design, because of the single-input operation, the only external components are the DC-blocking capacitors and the input inductors, which are implemented using bonding wires. However, compared to the dual-input structure, the optimization of both gain modes cannot be performed independently, which exacerbates the LNA core design.

The LNA uses a shunt-peak load to cover the WCDMA frequency bands I-III instead of a resonator, as in the first multicarrier receiver implementation. In the LG mode, the LNA gain is reduced by using the current-steering topology and a switched load. This is a compromise between the NF of the LNA and the ratio between the switched load impedances. Because of the shunt-peak load, the change in the load impedance requires an additional on-chip inductor and capacitor to meet the required load bandwidth.

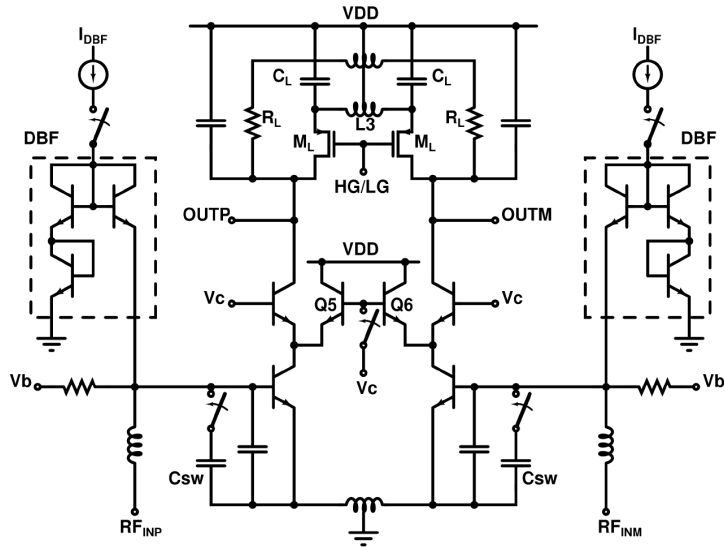


Figure 5.23. Simplified schematic of the single-input LNA [4] (© 2006 IEEE).

The I/Q mixers that were implemented are based on the modified double-balanced Gilbert cell topology. A simplified schematic of the mixers, including the mixer core and the mixer-baseband interface, is shown in Fig. 5.24. NMOS transistors are preferred in the input gm stage because of their better linearity compared to bipolar transistors. Conversely, bipolar transistors are chosen for the switching stage because of their good flicker noise properties.

With inductive degeneration, high linearity can be achieved, while the increase in the NF is almost insignificant. The linearity of the switching stage depends on the current through the switching transistors. Therefore, the current is optimized to be as low as possible for a low NF, but high enough to keep the adequate linearity of the switching stage from limiting the mixer linearity. A current-mode interface is implemented between the mixer and the baseband, which results in a high IIP<sub>3</sub>, as in the first multicarrier receiver implementation. In addition, the degeneration inductor does not cause a DC voltage drop, which is important in this design because of the 1.2-V output common-mode voltage required by the following low-pass filter. To reduce the chip area, both the I- and Q-branches use the same degeneration inductance. As a result of this arrangement, the total chip area of the I/Q mixers is reduced by approximately 40% compared to the first multicarrier receiver implementation.

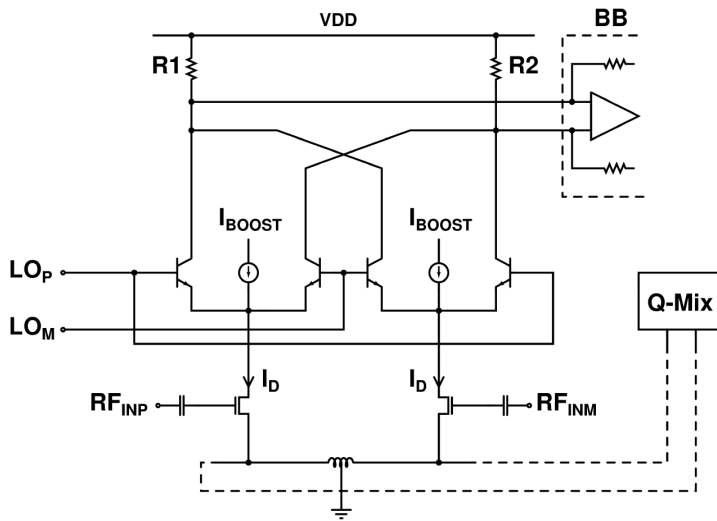


Figure 5.24. Schematic of the quadrature mixer [4] (© 2006 IEEE).

### 5.5.2 Experimental results of receiver

The chip was fabricated in an STMicroelectronics 0.25- $\mu\text{m}$  SiGe BiCMOS process. The total chip area, including the bonding pads, is 6.9 mm<sup>2</sup>. The chips were directly bonded onto a PCB and all the measurements were performed from the test output of the low-pass filter, except the gain, which was measured from the ADC buffer output. A micrograph of the single-chip receiver is shown in Fig. 5.25. The measured voltage gain, NF, and IIP<sub>3</sub> of the receiver are 51.5 dB, 3.0 dB, and -10 dBm, respectively.

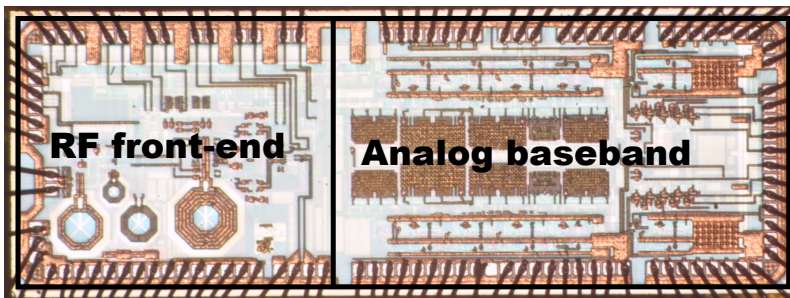


Figure 5.25. Chip micrograph of the multicarrier receiver [4] (© 2006 IEEE).

The measured voltage gain is 51.5 dB at 1.92 GHz in the HG mode and 34.2 dB in the LG mode. The measured gain variation within the WCDMA frequency bands I-III is less than 1 dB. The measured input matching is better than -10 dB over the desired bandwidth in both gain modes and the maximum operating frequency of the frequency divider is 2.5 GHz.

The ICP was measured using two different blocker tones. In the worst case the receiver is in the four-channel mode and the blocker at a 2.7-MHz offset from the center of the outermost channel, which results in a  $-37$ -dBm ICP, leaving 10 dB of headroom for the specifications. In order to measure the ICP of the RF front-end the out-of-band blocker was set far away from the in-band and the measured ICP was  $-22.5$  dBm in the HG mode. The corresponding values in the LG mode are  $-20$  dBm and  $-8.6$  dBm with 2.7-MHz and 40-MHz blocker frequency offsets, respectively.

The out-of-band IIP<sub>3</sub> of the receiver was measured with interfering signals located at offsets of 3.5 MHz and 5.9 MHz from the center of the channel [14], which are the worst-case test tones for this receiver, as discussed in Section 5.1.2. In the four-channel case the linearity of the low-pass filter affects the overall linearity of the receiver, resulting in a  $-10$ -dBm IIP<sub>3</sub> in the HG mode. In one-channel reception, the linearity is limited by the RF front-end and the measured IIP<sub>3</sub> was  $-8$  dBm in the HG mode. In the two- and three-channel cases the IIP<sub>3</sub> in the HG mode is between  $-10$  and  $-8$  dBm. In the LG mode the IIP<sub>3</sub> is  $+5$  dBm, regardless of the number of channels received.

The measured noise data are filtered mathematically using a bandpass RRC function with a roll-off factor of 0.22 and a  $-3$ -dB bandwidth of 3.84 MHz. Normally, this filtering would be performed by the DSP. The low-IF NF of the receiver is calculated by integrating the RRC-filtered output noise for the two WCDMA channels centered at 2.5 MHz and 7.5 MHz. To measure the NF in the direct conversion, only a single channel is received and the output noise is filtered with a 1.92-MHz-wide low-pass RRC filter with a roll-off factor of 0.22. The measured performance results are collected in Table 5.4.

Table 5.4. Measured performance of the receiver [4] (© 2006 IEEE).

	HG	LG	
Voltage gain	51.5	34.2	dB
S <sub>11</sub>	-15	-15	dB
NF low-IF *)	3.0 / 2.7	16.6 / 15.7	dB
NF DCR	2.2	12.1	dB
IIP <sub>3</sub>	-10	+5	dBm
ICP *)	-37 / -22.5	-20 / -8.6	dBm
Filter $-3$ -dB frequency	2.6 / 5.2 / 7.7 / 10.2		MHz
Current consumption	217	229	mA
Supply voltage	2.5	2.5	V

\*) For WCDMA channels centered at 2.5 and 7.5 MHz

### 5.5.3 Experimental results of low-pass filter

A micrograph of the filter is shown in Fig. 5.26. The active silicon area of the low-pass filter, including the ADC buffer, is 1.2 mm<sup>2</sup>. Although the filter has a wide set of bandwidths in this design, the chip area is only 30% larger compared to the first filter version. The measurement results were obtained from the test output of the filter, except the voltage gain, which was measured from the output of the ADC buffer. The test signals were fed into the filter through the biasing resistors R1 and R2 (BB test input in Fig. 5.7) and a nominal 18-dB gain setting was used.



Figure 5.26. Chip micrograph of the filter [2] (with permission from Springer Science+Business Media: [2], Fig. 7, © 2007 Springer Science+Business Media).

The measured and simulated frequency responses for all four frequency bands of the filter are shown in Fig. 5.27. The measured  $-3$ -dB frequencies with the typical tuning codes are 2.6 MHz, 5.2 MHz, 7.7 MHz, and 10.2 MHz. The measured responses match well with the simulated ones, except for the gain drooping at the passband edge. This is mainly caused by the routing resistances of the capacitor matrices. The routing resistances were not accurately modeled before the chip fabrication. However, with a more accurate model, the matching between the measurements and simulations was achieved. The output noise voltages of the filter for all four frequency bands are measured and simulated from 10 kHz to 20 MHz. These noise voltages are referred to the filter input by dividing them by the DC gain of the filter and the result is shown in Fig. 5.28. When the filter bandwidth is 10 MHz, the measured integrated input-referred noise from 10 kHz to 20 MHz is 27 mV<sub>rms</sub>, which corresponds to a 8.5-nV/ $\sqrt{\text{Hz}}$  input-referred noise density with the measured  $-3$ -dB bandwidth of 10.2 MHz. The noise measurement results for all the bandwidths of the filter are collected in Table 5.5. A constant measured input-referred noise density, which is essential in a multicarrier application, is achieved.

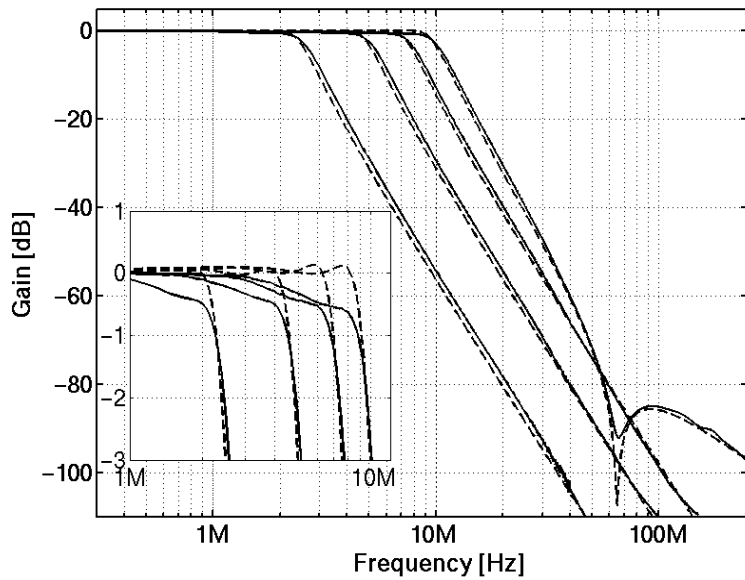


Figure 5.27. Measured (solid line) and simulated (dashed line) frequency responses of the filter (with permission from Springer Science+Business Media: [2], Fig. 8, © 2007 Springer Science+Business Media).

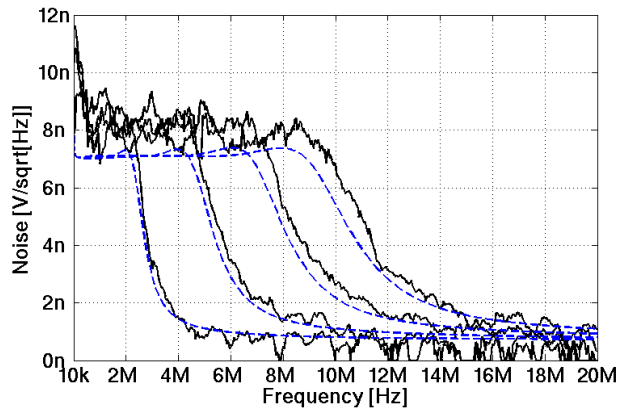


Figure 5.28. Measured (solid line) and simulated (dashed line) filter noise voltages divided by the DC gain of the filter for all four frequency bands (with permission from Springer Science+Business Media: [2], Fig. 9, © 2007 Springer Science+Business Media).

External passive low-pass and high-pass filters were used to minimize the IMD<sub>3</sub> caused by the measurement set-up itself (for example, the signal generators). Because of the limited number of available external passive filters, the out-of-band IIP<sub>3</sub> was measured with 11-MHz and 20.5-MHz test signals, which are not exactly the same as in Fig. 5.2. As shown in Fig. 5.29, the measured out-of-band IIP<sub>3</sub>s of the filter are +20 dBV, +25 dBV,

+30 dBV, and +38 dBV in the case of the 10-MHz, 7.5-MHz, 5-MHz, and 2.5-MHz filter bandwidths, respectively. The in-band IIP<sub>3</sub> was measured only in the case of the 10-MHz bandwidth of the filter because of the limitations of the measurement setup. The measured in-band IIP<sub>3</sub> is +9.7 dBV with 4.5-MHz and 8.5-MHz test signals. Thus, the in-band spurious free dynamic range of the filter with the 10.2-MHz bandwidth is 67 dB. The filter degrades the linearity of the whole receiver by 2 dB at the maximum. The measured current consumption of the filter, including the ADC buffer, is 85 mA. The measured performance results are collected in Table 5.5.

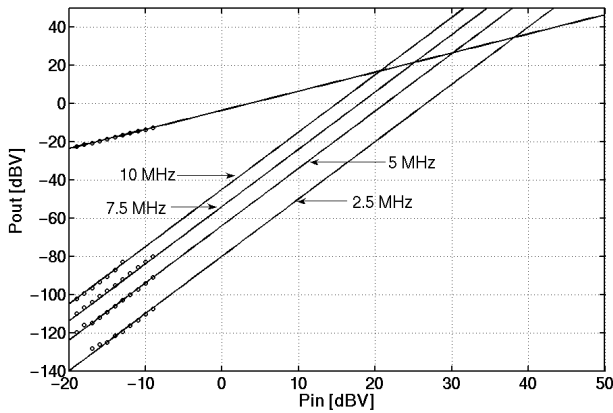


Figure 5.29. Measured out-of-band linearities with 11-MHz and 20.5-MHz test signals for all four frequency bands. The fundamental curve is measured at 11 MHz and the four IMD<sub>3</sub> curves are measured at 1.5 MHz (with permission from Springer Science+Business Media: [2], Fig. 10, © 2007 Springer Science+Business Media).

Table 5.5. Performance summary [2] (with permission from Springer Science+Business Media: [2], Table II, © 2007 Springer Science+Business Media).

Technology	0.25- $\mu$ m SiGe BiCMOS	
Filter order	4	
Supply voltage*	2.5	V
Voltage gain*	12 / 18 / 24	dB
-3-dB frequency	10.2 / 7.7 / 5.2 / 2.6	MHz
Input-referred noise**	27 / 22.7 / 19.6 / 14.2	$\mu$ V <sub>rms</sub>
Input-referred noise density***	8.5 / 8.2 / 8.6 / 8.8	nV/ $\sqrt$ Hz
IIP <sub>3</sub> (in-band)	+9.7 / - / - / -	dBV
IIP <sub>3</sub> (out-of-band)	+20 / +25 / +30 / +38	dBV
In-band SFDR	67 / - / - / - / -	dB
Current consumption*	85	mA

\* Including ADC buffer

\*\* Integrated from 10 kHz ... 20 MHz

\*\*\* Measured -3-dB bandwidths used



## 5.6 Summary and comparison with other published filters

The design and implementation of two evolution versions of continuous-time opamp-RC low-pass filters were described in Section 5.3 and their measurement results were presented in Sections 5.4.3 and 5.5.3. Both fourth-order 10-MHz low-pass filters are capable of handling up to four adjacent WCDMA channels simultaneously while meeting the stringent in-band noise and out-of-band linearity requirements set by the targeted multicarrier WCDMA base-station application. In the first 10-MHz opamp-RC filter, attention was paid to optimization of the performance of the high-speed BiCMOS opamps. Their high DC gain, GBW, and current consumption improve the linearity of the filter. Similar high-speed BiCMOS opamps were also used in the second filter version. However, as a result of the programmability that was implemented, the second filter version does not achieve as high measured in- and out-of-band dynamic ranges as the first filter version. It is worth pointing out that although both experimental opamp-RC filter circuits were designed according to the specifications of the targeted multicarrier base-station application, they can be utilized in other wideband applications as well.

The measured performance of the opamp-RC low-pass filters of this work is compared to recently published low-pass filters with a bandwidth of approximately 5 MHz-20 MHz in Table 5.6. It can be observed that the spurious-free dynamic range of the opamp-RC filters of this work compares favorably with the work of others. As a matter of fact, the first filter version of this work achieves a state-of-the-art performance in terms of the spurious-free dynamic range. However, it should be pointed out that the filter implementations in Table 5.6 are designed for different applications. Therefore, the requirements of the filters may considerably differ from each other. In this work, the filter requirements differ, for example, from those set by mobile-station applications because of the multicarrier BS approach. The blocking and interfering signals are located very close to the passband edge of the low-pass filter, which corresponds to a high in-band linearity requirement.

Two evolution versions of a single-chip multicarrier WCDMA receiver were presented in Sections 5.4 and 5.5. The first receiver to be designed and implemented includes an RF front-end, an LO divider, IIP2 calibration circuits, and two active low-pass filters with ADC buffers. The LNA includes two amplifier cores to optimize the performance in the two different gain modes. In the downconversion mixers the required high linearity with a low NF is achieved by using an inductively degenerated input stage and exploiting the low input impedance of the first opamp of the low-pass filter. In addition, IIP2 calibration circuits were implemented in the mixer input

stage and LO buffers because of the low-impedance mixer load. The second version is a programmable 1-to-4-channel multicarrier WCDMA receiver consisting of an RF front-end and two active low-pass filters with ADC buffers. The high dynamic range in the RF front-end is achieved by using an inductively degenerated single-input LNA, which was optimized to operate in two different gain modes. The I/Q mixers using combined inductive degeneration offer high linearity and a compact chip area. The measurement results of both RF receivers demonstrate that it is possible to implement a multicarrier WCDMA receiver for BS applications with a sufficient performance on a single chip.

Table 5.6. Comparison of low-pass filter implementations.

Ref.	Year	Technology	Topology	Proto/Order	$f_{-3dB}$ [MHz]	Gain [dB]	Noise (1) [nV/√Hz]	IIP3 (2) [dBm]	$V_{DD}/P_D$ [V]/[mW]	Area (3) [mm <sup>2</sup> ]	SFDR (4) [dB]
[26]	2003	0.18- $\mu$ m CMOS	gm-C	El / 6	1.5-12	0	174 (5)	+9.3 (6)	1.8 / 10 (7)	0.83	41 (6)
[27]	2004	0.18- $\mu$ m CMOS	gm-C	Bu / 4	0.5-12	0	254 (8)	+9.4 (6)	1.8 / 4.5 (7)	0.125	39 (9)
[1]/[3]	2006/06	0.25- $\mu$ m BiCMOS	op-RC	Ch / 4	9.8	11	11.2	+38	2.5 / 218	0.9	76
[4]/[2]	2006/08	0.25- $\mu$ m BiCMOS	op-RC	Ch / 4	2.6-10	18	8.8	+22.7	2.5 / 213	1.2	67
[28]	2006	0.13- $\mu$ m CMOS	a-gm-RC	Be / 4	2.1-11	4	10.9 (10)	+21	1.2 / 14.2	0.9	65
[29]	2006	0.12- $\mu$ m CMOS	op-RC	Ch/5 (11)	5-10	= 0	143 (12)	+ 21	1.0 / 4.6	0.17	50 (13)
[30]	2006	0.13- $\mu$ m CMOS	op-RC	Be / 4	2.5-11	8	54 (14)	+21.3	1.2 / 5.6	0.8 (15)	56
[31]	2006	0.18- $\mu$ m CMOS	s-f-b	Be / 4	10	-3.5	7.5	+17.5	1.8 / 4.1	0.26	65
[32]	2007	0.35- $\mu$ m CMOS	gm-C	El / 5	30	= 0	21 (16)	na	3.3 / 85	1.4	65 (17)
[33]	2007	0.13- $\mu$ m CMOS	a-gm-RC	Bu/6 (18)	0.35-23.5	0	25.8 (19)	+20 (20)	1.2 / 15 (21)	0.52 (22)	57
[34]	2007	0.13- $\mu$ m CMOS	op-RC	Ch / 5	19.7	2	30	+18.3 (23)	1.5 / 11.3	0.2	55
[35]	2008	0.13- $\mu$ m CMOS	gm-C	Bu / 2	0.1-20	0	5.6 (24)	+20 (25)	1.2 / 14.2 (26)	0.5	66
[36]	2009	0.13- $\mu$ m CMOS	op-RC	Ch/5 (27)	1-20	= 0	52	+26	1 / 7.5	1.53	57
[37]	2009	0.18- $\mu$ m CMOS	gm-C	Bu / 3	0.5-20	0	12	19	1.2 / 11.1	0.23	61
[38]	2009	0.5- $\mu$ m CMOS	gm-C	Ch / 3	6-12	= 0	64 (28)	+33	5 / 180 (29)	1.5	62
[39]	2010	90-nm CMOS	gm-C	Bu / 6	8.1-13.5	= 0	75	+22	1 / 4.35	0.239	53

Ref.	Year	Proto	$V_{DD}$ [V]	FoM1 (30) [nJ]	FoM2 (31) [fJ]	FoM3 (32) [fJ] / ranking	FoM4 (33) [fJ mm <sup>2</sup> ] / ranking
[26]	2003	El	1.8	0.17	13.2	13.2	11.0
[27]	2004	Bu	1.8	0.11	14.2	14.2	1.77
[1]/[3]	2006/06	Ch	2.5	5.56	0.14	0.04 / 1	0.04 / 3
[4]/[2]	2006/08	Ch	2.5	5.33	1.06	0.13 / 5	0.16 / 10
[28]	2006	Be	1.2	0.32	0.10	0.06 / 3	0.06 / 5
[29]	2006	Ch	1.0	0.09	0.92	0.92	0.16 / 10
[30]	2006	Be	1.2	0.13	0.32	0.13 / 5	0.10 / 8
[31]	2006	Be	1.8	0.10	0.03	0.05 / 2	0.01 / 1
[32]	2007	El	3.3	0.57	0.18	0.18	0.25
[33]	2007	Bu	1.2	0.11	0.21	0.21	0.11 / 9
[34]	2007	Ch	1.5	0.11	0.36	0.29	0.06 / 5
[35]	2008	Bu	1.2	0.36	0.09	0.09 / 4	0.04 / 3
[36]	2009	Ch	1	0.08	0.15	0.15	0.23
[37]	2009	Bu	1.2	0.19	0.15	0.15	0.03 / 2
[38]	2009	Ch	5	5.00	3.15	3.15	4.73
[39]	2010	Bu	1	0.05	0.27	0.27	0.06 / 5

a-gm-RC = active-gm-RC, op-RC = opamp-RC, s-f-b = source-follower-based, Be = Bessel, Bu = Butterworth, Ch = Chebyshev, El = Elliptic

- (1) Input-referred noise density in the case of the max. bandwidth
- (2) In-band linearity in the case of the max. bandwidth. It should be noted that the in-band IIP3 of a low-pass filter depends on the test tone frequencies selected.
- (3) Active chip area
- (4) In-band SFDR calculated from the in-band noise and IIP3 in the case of the max. bandwidth using (2.15)
- (5) Calculated from the SFDR (41 dB) and FoM (0.35 fJ) values reported for the 10-MHz bandwidth setting in the publication
- (6) Reported value for the 10-MHz bandwidth setting

- (7) Reported power dissipation for the 10-MHz bandwidth setting
- (8) Calculated from the FoM (2.3 fJ) and in-band IIP<sub>3</sub> (+9.4 dBm) values reported for the 10-MHz bandwidth setting in the publication
- (9) Calculated from the FoM value of 2.3 fJ reported for the 10-MHz bandwidth setting
- (10) Calculated from the reported 36- $\mu\text{V}_{\text{rms}}$  integrated input-referred noise value
- (11) Includes also an Elliptic prototype as an option, but the stopband attenuation of the Chebyshev prototype is more comparable with [1] and [2]
- (12) Calculated from the reported 453- $\mu\text{V}_{\text{rms}}$  integrated output noise value
- (13) SFDR = 50 dB is calculated from the in-band IIP<sub>3</sub> (+21 dBm) and integrated output noise (453  $\mu\text{V}_{\text{rms}}$ ) values reported for the 10-MHz Chebyshev filter in the publication. (SFDR = 69 dB is reported in the publication.)
- (14) Calculated from the reported 447- $\mu\text{V}_{\text{rms}}$  integrated output noise value (includes the noise of a DAC as well)
- (15) Including a DAC
- (16) Calculated from the reported 115- $\mu\text{V}_{\text{rms}}$  integrated output noise value
- (17) Reported SFDR value used because the in-band IIP<sub>3</sub> not given in the publication
- (18) Includes also a selectable filter order
- (19) Calculated from the 125.3- $\mu\text{V}_{\text{rms}}$  integrated input-referred noise value that is reported in Fig. 9 in the publication
- (20) Calculated from the reported 9.96-dBV<sub>p</sub> value
- (21) Power dissipation is calculated from the current consumption value of 12.5 mA that is shown in Fig. 9 in the publication in the case of the 125.3- $\mu\text{V}_{\text{rms}}$  integrated input-referred noise value and 23.5-MHz bandwidth
- (22) The active chip area of one LPF estimated to be 0.52 mm<sup>2</sup> on the basis of Fig. 6 and the 1.56-mm<sup>2</sup> value which are reported in the publication for the I–Q channels of both the LPF and VGA
- (23) Calculated from the reported 5.2-V<sub>pp</sub> value
- (24) Calculated from the reported 25- $\mu\text{V}_{\text{rms}}$  integrated noise value
- (25) Calculated from the reported 10 dBV<sub>p</sub> value
- (26) Power dissipation is calculated from the current consumption value of 11.85 mA that is reported in the publication for the 20-MHz bandwidth setting
- (27) Includes also an Inverse Chebyshev prototype as an option and a selectable filter order
- (28) Equivalent input noise reported at 1 MHz
- (29) Calculated from the reported power per pole value of 60 mW
- (30) Calculated from (2.19)
- (31) Calculated from (2.20)
- (32) Calculated from (2.21)
- (33) Calculated from (2.22)

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## 6 Gm-C filters for CMOS direct-conversion receivers

The purpose of this chapter is to give a detailed description of circuit techniques that were used in this work in the three gm-C filter implementations, of which the experimental results are presented in Chapter 7. Consequently, the focus is on circuit techniques that are suitable for use when designing and implementing low-voltage wideband analog low-pass filters with programmable voltage gain in standard ultra-deep-submicron ( $< 0.2\text{-}\mu\text{m}$ ) or nanoscale (sub-100-nm) CMOS technologies. The low supply voltage ( $\approx 1.2\text{ V}$ ) of the modern CMOS technologies limits the voltage swing and, thus, the dynamic range in analog integrated circuits. The voltage headroom can be increased by reducing the number of stacked transistors. Therefore, in this work, the functionality of the main signal processing circuits was improved by employing parallel-connected control circuits instead of using, for example, cascode transistors or other conventional circuit solutions previously utilized with higher supply voltages. Some of the circuit techniques that are presented in this chapter have been developed in this work. Parts of them are improved or modified versions of circuits previously proposed by others that were tailored in this work to fulfill the needs determined by the low-voltage wideband receiver applications adopted in this work. This chapter is mainly based on the contents of publications [1] and [2]<sup>4</sup>.

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<sup>4</sup>Portions of this chapter are taken from [1] (© 2009 IEEE) and [2] (© 2007 IEEE).



It is worth emphasizing that the experimental gm-C filter circuits of this work were implemented as a part of a single-chip radio receiver. It was discussed in Chapter 2 that the analog baseband circuit preceding the ADC is typically required to have an adjustable gain control. This is especially the case in direct-conversion receivers. The baseline for the design of the gm-C filter circuits was to partially merge the filters together with a programmable gain amplifier, in addition to embedding several decibels of voltage gain into the low-pass filters. This design approach makes it possible to perform both the filtering and signal amplification with a single analog integrated circuit, potentially leading to a compact and power-efficient realization with reduced noise contribution.

This chapter is organized as follows. In Section 6.1, one alternative way to implement a differential or pseudo-differential high-order gm-C low-pass filter for an integrated radio receiver is discussed at the circuit block level. Section 6.2 is devoted to describing a simple pseudo-differential transconductor with a common-mode feedforward (CMFF), common-mode feedback (CMFB), mirror error compensation, and a DC gain control circuit. The transconductor that is presented has no bandwidth limitations and hence it is suitable for use in wideband gm-C filters. Two different alternative ways to realize a gain and cutoff frequency control in a differential or pseudo-differential gm-C filter are described in Sections 6.3 and 6.4, respectively. Chapter 6.5 briefly reviews the DC offset compensation schemes that are most frequently used in the analog baseband circuits of integrated radio receivers. Finally, in Section 6.6, a theoretical non-linearity analysis for a pseudo-differential gm-C low-pass filter is presented.

## 6.1 Balanced high-order gm-C low-pass filter

Fig. 6.1 shows a differential fourth-order gm-C leapfrog filter that is derived from its single-ended counterpart presented earlier in Fig. 4.4 in Chapter 4. Similarly to Chapter 4, without the loss of generality, the discussion of high-order gm-C low-pass filters is continued in this chapter by concentrating on the fourth-order gm-C filter shown in Fig. 6.1. This corresponds to the filter order of the two experimental gm-C filter circuits that were implemented in this work as a part of two evolution versions of the integrated UWB radio receivers. The gm-C leapfrog filter shown in Fig. 6.1 may also represent a pseudo-differential realization, depending on whether balanced differential or balanced pseudo-differential transconductors are employed. In addition to the fourth-order active gm-C filter, the circuit presented in Fig. 6.1 also includes a passive RC pole at the active filter input, increasing the overall

filter order by one. The implementation and benefits of a passive RC pole preceding an active low-pass filter were discussed in Sections 2.3, 4.1.2, and 5.2. In all the experimental gm-C filters of this work, the real pole was extracted from the fifth- and third-order filter transfer functions that were adopted in those designs. The real pole was implemented at the gm-C filter input with the passive load components of the preceding Gilbert cell downconversion mixers, as described in Section 5.2. In general, the resistor and capacitor at the gm-C filter input in Fig. 6.1 could also represent the resistive load of a preceding active downconversion mixer and a parasitic capacitance present at the mixer output, respectively. In that case, the high-frequency parasitic RC pole that is formed is not considered to increase the filter order.

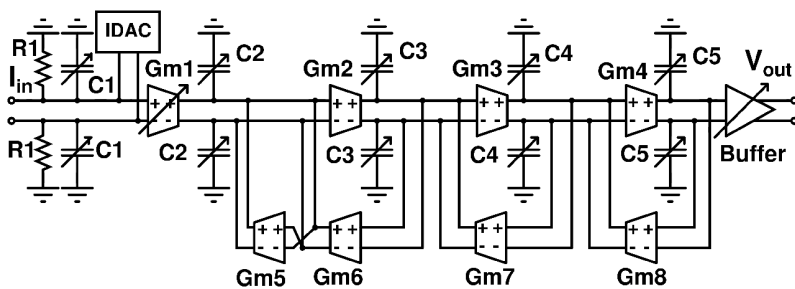


Figure 6.1. Fourth-order active gm-C low-pass filter and a passive RC pole with an IDAC and an output buffer [1] (© 2009 IEEE).

The circuit block named *IDAC* in Fig. 6.1 stands for a current-steering digital-to-analog converter. Such a circuit was designed and implemented for all the experimental gm-C filter circuits of this work to compensate for the DC offset, which is unavoidable in integrated radio receivers and analog baseband circuits, as discussed previously in this thesis. Different DC offset removal schemes will be discussed briefly in Section 6.5. In general, IDAC, in Fig. 6.1, could be considered to represent any of those schemes.

The last circuit block at the gm-C filter output in Fig. 6.1 is a buffer amplifier that may be needed to drive the capacitive input impedance of a following ADC or limiting amplifier chain, which was the case in all the experimental gm-C filter circuits of this work. Considering the trade-off between the noise and linearity in analog baseband circuits, for the noise, the gain should be implemented at the input, while for the linearity, it is usually desirable to implement the gain at the output of the circuit. Therefore, in radio receiver applications, the buffer amplifier in Fig. 6.1 is more likely to be a variable or programmable gain amplifier (PGA) instead of a pure unity-gain buffer. In the experimental circuits of this work, the output buffers were designed to have a digitally controlled programmable

gain, as will be described in more detail in Section 6.3. Moreover, the first transconductor of both the experimental 240-MHz filter circuits implemented for UWB radio receivers,  $G_{m1}$  in Fig. 6.1, was constructed from parallel-connected binary-weighted unit transconductors with a digital control. This corresponds to merging a programmable gain amplifier at the input of the analog baseband circuit together with the continuous-time low-pass filter. Hence, it is worth comparing the analog baseband circuit of Fig. 6.1, constructed from a passive pole, an active low-pass filter, and two PGAs, with the one shown in Fig. 2.5.

## 6.2 Transconductor

Section 3.3 showed that transconductors are essential building blocks in continuous-time gm-C filters and the overall performance of a gm-C filter, including the filter frequency response, noise, linearity, and power consumption, is determined by the characteristics of the transconductors. A wide variety of CMOS transconductor structures have been presented in the literature. Most of them use a supply of over 1.2 V. Owing to the low supply voltage of the ultra-deep-submicron CMOS technologies adopted in this work, combined with the wide bandwidth targeted, the number of viable transconductor topologies becomes limited. This section concentrates on the transconductor structure that was used in the experimental gm-C filter circuits of this work. A review of CMOS transconductance amplifier circuits is presented in, for example, [3]. In addition, other alternative transconductor realizations are described in the gm-C filter publications cited in Section 7.5.

### 6.2.1 Pseudo-differential structure

The core of the transconductor used in the experimental filter circuits of this work is a pseudo-differential structure with an NMOS input transistor pair and PMOS current source loads as shown in Fig. 6.2 [4]-[7]. This simple structure has no internal poles, which is an advantage in wideband filter design. Considering the low supply voltage, the lack of cascode and tail transistors is important for increasing the output voltage range and for minimizing the noise from the load transistors. Furthermore, NMOS input transistors are used instead of PMOS transistors in order to minimize the parasitic input capacitance of the transconductor.

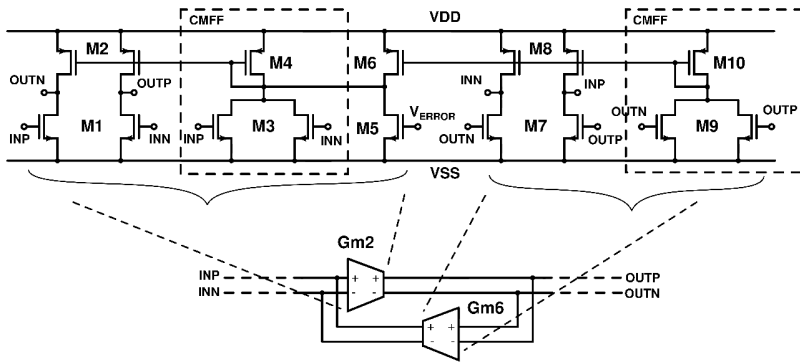


Figure 6.2. Pseudo-differential transconductor with the CMFF and CMFB circuits [1] (© 2009 IEEE).

The turn-on voltage ( $V_{GS} - V_{TH}$ ) determines the linearity of the transconductor. On the basis of linearity simulations, a 700-mV common-mode bias voltage was chosen in the experimental filter circuits. The threshold voltage ( $V_{TH}$ ) of the core transistors that were used was around 400 mV. Low- $V_{TH}$  transistors were not available (at that time) in the CMOS processes that were adopted in this work. The resulting nominal (i.e. unscaled) transconductance of the transconductors was in the range of 850–900  $\mu\text{S}$  in all three implementations of this work. The capacitance values of the filter coefficients were determined according to that transconductance value. The DC gain and the current consumption of the transconductor, as well as mismatches in its transconductance, depend on the gate-source voltage and the channel length of the transistors. In addition, the minimization of the transconductor parasitic capacitances is important in wideband filter designs. Transistors with a channel length of 0.25- $\mu\text{m}$  were used in the transconductors that were designed for the 240-MHz filter implementations. With a transistor channel length of 0.25  $\mu\text{m}$ , the unity current gain frequency  $f_t$  of the transconductor, simulated by shorting the transconductor output to AC ground, is over 50 times higher than the passband edge frequency of the 240-MHz experimental filters. It was observed that the DC gain of the transconductor does not increase considerably with higher transistor channel lengths.

The price paid for a simple transconductor structure is that pseudo-differential integrated circuits inherently have a poor common-mode rejection and they are also known to be prone to power supply rail and ground line disturbances. The effect of the lack of an input common-mode rejection of a pseudo-differential gm-C filter in a receiver will be studied in Section 6.6. The input common-mode rejection of a pseudo-differential transconductor can be improved with circuit techniques that are described in the next sub-section. In the 1-GHz filter implementation, the channel

length of the transistors was reduced to  $0.18\ \mu\text{m}$  to speed up the operation of the common-mode cancellation circuits.

### 6.2.2 Transconductor with CMFF and CMFB circuits

To obtain input common-mode rejection and hence, to increase the IIP2 of the whole receiver, the transconductor core is followed by a common-mode feedforward (CMFF) circuit, as shown in Fig. 6.2 [4],[5]. It replicates the common-mode current and subtracts it from the transconductor output by means of the transistors M3 and M4, respectively. The transconductance of the pseudo-differential transconductor depends on the common-mode bias voltage. To achieve an accurate filter frequency response, the common-mode voltage is not allowed to vary between the different filter nodes. The CMFF circuit cannot fix the output common-mode voltage of the transconductor. To establish the 700-mV common-mode level at the transconductor output, the complete transconductor also includes a common-mode feedback (CMFB) circuit [6]-[8].

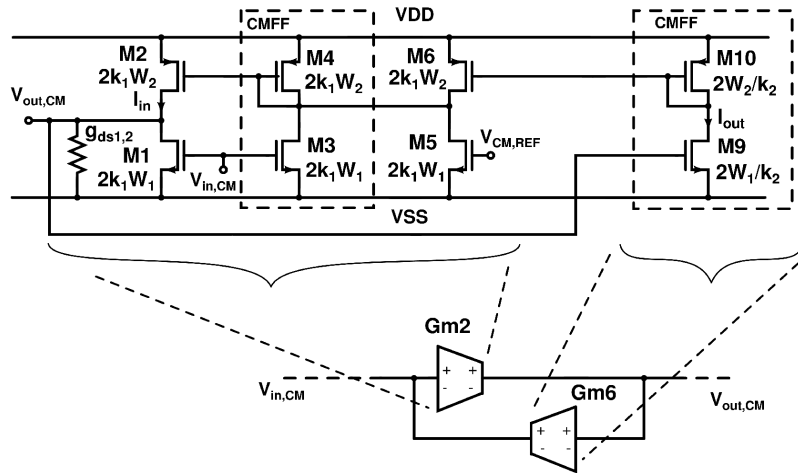


Figure 6.3. Equivalent circuit of the pseudo-differential transconductor when only CM signals are of concern.

The CMFB circuit reuses the common-mode signal generated by the CMFF of the following transconductor, M9 and M10. In this work, the transistor M5, which has a fixed common-mode gate bias voltage, introduces the CM reference signal for the circuit. The output common-mode signal that is detected is fed back to the preceding transconductor by the transistor M6 and compared with the fixed reference current of M5, as shown in Fig. 6.2. This leads to the DC common-mode rejection being limited by the accuracy of the PMOS current mirror in the CMFF circuit. The detailed schematic of the pseudo-differential transconductor can be

simplified to an equivalent circuit presented in Fig. 6.3 when only common-mode signals are of concern. In Fig. 6.3, the scaling factors  $k_i$  correspond to the gain scaling factors presented in Fig. 4.4 in Section 4.2. If voltage gain is to be implemented, the size of the feedforward and feedback transconductors is scaled in opposite directions and thus,  $k_2$  is chosen to be equal with  $k_1$ . As discussed in Chapter 4, in the gm-C filter implementations of this work, transconductor size ratios of 16 at the maximum were realized. A higher gain value would have been more challenging to implement in practice.

The CMFB circuit can be considered as a shunt-series feedback amplifier. The open-loop DC gain of the current amplifier can be expressed as

$$A_i = \frac{I_{out}}{I_{in}} = \frac{-gm_9 \cdot \left( \frac{1}{g_{ds1,2}} \right) \cdot I_{in}}{I_{in}} = \frac{-gm_9}{g_{ds1,2}}, \quad (6.1)$$

where  $g_{ds1,2}$  is the output conductance of the transconductor Gm2 (i.e. the drain-source conductance of the transistors M1 and M2). The feedback factor is

$$\beta = \frac{-gm_6}{gm_{10} + g_{ds9,10}} \cdot \frac{-gm_2}{gm_4 + g_{ds3,4,5,6}}, \quad (6.2)$$

where  $g_{ds9,10}$  is the drain-source conductance of the transistors M9 and M10. Correspondingly,  $g_{ds3,4,5,6}$  is the drain-source conductance of the transistors M3-M6. Since the input resistance  $R_{in}$  of the current amplifier is inversely proportional to the output conductance of the transconductor Gm2,  $R_{in} = 1/g_{ds1,2}$ , on the basis of (6.1) and (6.2), the input resistance of the shunt-series feedback amplifier can be written as

$$R_{if} = \frac{R_{in}}{1 + \beta A_i} = \frac{\left( \frac{1}{g_{ds1,2}} \right)}{1 + \left( \frac{-gm_9}{g_{ds1,2}} \right) \left( \frac{-gm_6}{gm_{10} + g_{ds9,10}} \right) \left( \frac{-gm_2}{gm_4 + g_{ds3,4,5,6}} \right)}. \quad (6.3)$$

Thus, the common-mode voltage gain from the input to the output of the transconductor Gm2 at DC is

$$A_{CM} = \frac{V_{out,CM}}{V_{in,CM}}$$

$$= \frac{gm_1 - \left( \frac{gm_3 gm_2}{gm_4 + g_{ds3,4,5,6}} \right)}{g_{ds1,2} - gm_9 \left( \frac{-gm_6}{gm_{10} + g_{ds9,10}} \right) \left( \frac{-gm_2}{gm_4 + g_{ds3,4,5,6}} \right)}. \quad (6.4)$$

If it is assumed that  $g_{ds3,4,5,6}$  to be negligible compared to  $gm_4$ , the DC common-mode voltage gain diminishes to zero when simultaneously  $gm_1 = gm_3$  and  $gm_2 = gm_4$ . This condition cannot be met without  $M_5$ , which is the case in an almost identical transconductor presented in [6]. It has a CMFB circuit which refers to the CM level at the transconductor input instead of a fixed reference signal. Therefore, any common-mode voltage error at the input of such a transconductor can accumulate in the following filter stages.

In this work, the dominant pole frequency of the CMFB circuit of the 240-MHz filter implementations was simulated to be around 190 MHz. Although the pole lies at a relatively high frequency, the simulated phase margin of the CMFB loop is as high as  $80^\circ$  to guarantee the stability of the circuit. The bandwidth of the common-mode response of the 1-GHz filter design was simulated to be approximately 600 MHz. In the circuits that were implemented, the gain of the CMFB is relatively low and, therefore, the bias generation of the transconductor has to be accurate. A systematic error in the PMOS current mirror of the transconductor is canceled by predistorting the CM reference current of  $M_5$ , as is discussed in more detail in the next sub-section.

### 6.2.3 Mirror error compensation circuit

A systematic error exists in the PMOS current mirror of the transconductors presented in Section 6.2.1 as a result of the finite (i.e. non-zero) output conductance of the transistors. The amount of the error is not constant for different process corners and temperatures. The mirror error can be modeled as a small common-mode current that is injected into the transconductor output. Since the CMFB of the transconductor is not capable of suppressing the error adequately, the injected common-mode current will be summed with the drain current of the NMOS input transistors of the transconductor,  $M_1$  in Fig. 6.2. The injected common-mode current can be written as

$$I_{error} = \alpha \frac{1}{2} gm_1 (V_{GS} - V_{TH}), \quad (6.5)$$

where  $gm_t$  is the transconductance of the NMOS input transistor M1 and  $\alpha$  is the ratio of the error current and the drain current. Let us study how the error current that is injected affects the output common-mode voltage of the transconductor. Similarly to Section 6.2.2 and Fig. 6.3, the CMFB circuit is again considered to be a shunt-series feedback amplifier. Since the input resistance of the shunt-series feedback amplifier, on the basis of (6.1)-(6.3), is  $R_{if} \approx 1/(\beta \cdot gm_9)$ , the error current that is injected converts to an error voltage at the transconductor output

$$V_{error} = R_{if} \cdot I_{error} = \frac{1}{\beta \cdot gm_9} \cdot \left[ \alpha \frac{1}{2} gm_1 (V_{GS} - V_{TH}) \right]. \quad (6.6)$$

When it is taken into account that in the transconductors designed for the 240-MHz gm-C low-pass filters of this work  $gm_t = k_1 \cdot k_2 \cdot gm_9$  and  $\beta = k_1 \cdot k_2$ , as can be concluded in Fig. 6.3, equation (6.6) can be rewritten as

$$V_{error} = \alpha \frac{1}{2} (V_{GS} - V_{TH}). \quad (6.7)$$

This leads to a shift in the output common-mode voltage of the transconductor. Because of the potentially high voltage gain of an active filter, which is the case in the 240-MHz low-pass filters of this work, the common-mode error will be accumulated in the filter. Since the transconductances of the pseudo-differential transconductors are dependent on the input common-mode level, the error current causes the filter frequency response to deteriorate. Owing to the low supply voltage, the cascode transistors typically utilized in conventional gm-C filters to improve mirroring accuracy cannot be used in the low-voltage application under consideration here. Hence, the systematic common-mode level error is canceled by a bias circuit. As a matter of fact, two almost identical bias circuits were designed and implemented in this work, one for the feedback transconductors, Gm5-Gm8 in Fig. 6.1, and the other one for the feedforward transconductors, Gm1-Gm4. The principle of the operation in both circuits is to add the common-mode error with reverse polarity to the related transconductors.



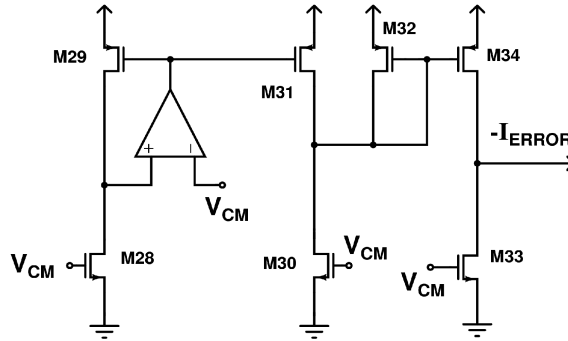


Figure 6.4. Bias circuit for the mirror error compensation in feedback transconductors.

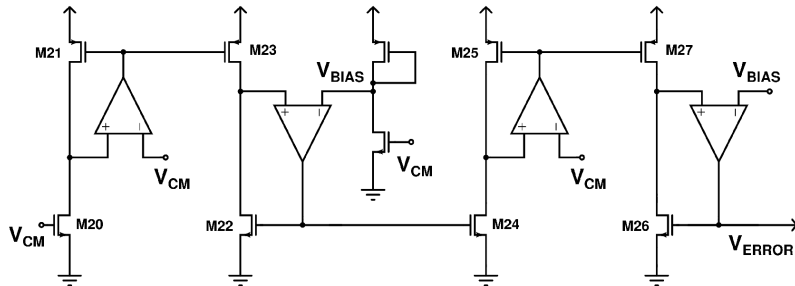


Figure 6.5. Bias circuit for the mirror error compensation in feedforward transconductors [1] (© 2009 IEEE).

The bias circuits are shown in Fig. 6.4 and 6.5. Each circuit generates the replica of the mirror-error and subtracts it from the transconductor. In the circuit shown in Fig. 6.4, the transistors  $M_{28}$ - $M_{29}$  and  $M_{30}$ - $M_{31}$  are copies of the transconductor core and the CMFF circuit, respectively. In Fig. 6.5, the transistors  $M_{20}$ - $M_{21}$  and  $M_{24}$ - $M_{25}$  are copies of the transconductor core and the transistors  $M_{22}$ - $M_{23}$  and  $M_{26}$ - $M_{27}$  are copies of the CMFF circuit. Bias voltages similar to those of the original transconductor are set by differential stages. The differential stages are depicted by operational amplifier blocks in Fig. 6.4 and 6.5. Thus, an error current identical with the error current of the original transconductor is generated. In the feedback transconductors, the error current that is generated is directly connected with reverse polarity to the common drain of  $M_9$  and  $M_{10}$  (see Fig. 6.2). In the feedforward transconductors, the error current that is generated is subtracted from the transconductor by connecting the gate of the transistor  $M_{26}$  to the gate of the transconductor transistor  $M_5$ . This leads to a correctly predistorted common-mode reference current of  $M_5$ . Since the CM signal path of the feedforward transconductors includes two PMOS current mirrors because of the CMFB circuit, an error current that is twice as large compared to the feedback transconductors has to be generated.

Therefore, a two-stage bias circuit is needed for the feedforward transconductors. With the circuit, the output common-mode voltage of the transconductor is simulated to shift less than 0.5%. In the layout design, attention must be paid to matching the transconductors with the corresponding bias circuits in order to achieve the simulated improvement.

#### 6.2.4 DC gain control in transconductors

In gm-C filter implementations, negative resistance circuits can be used to cancel the finite output conductance (i.e. non-zero) of the transconductors and hence to enhance the DC gain of the transconductors [9]-[12]. The method is suitable for wideband filter design since it does not add internal poles in the transconductor, contrary to, for example, cascode transistors. The idea behind the filter design approach presented in Chapter 4 was to accept a low DC gain for the transconductors which enables a simple transconductor circuit to be used, for example, the one described in Section 6.2.1. However, although the DC gain of the transconductors can be low, it must be accurate. Moreover, the filter synthesis that was presented was based on the assumption that all the transconductors in the gm-C filter to be synthesized have a uniform nominal DC gain value. Therefore, the DC gain of the filter transconductors must somehow be controlled against PVT variations and the DC gain control in transconductors is of importance in this work.

In the experimental gm-C filter circuits implemented in this work, the negative resistance circuit presented in Fig. 6.6 was connected to the output of each transconductor to control their DC gain. Without any DC gain control, the DC gain of the transconductors shown in Fig. 6.2 was simulated to be around 20 dB and to vary by approximately 4 dB for different process corners and temperatures. It is worth emphasizing that the DC gain of the transconductors under consideration is determined by the intrinsic gain of the NMOS input transistors. Thus, the simulated 20-dB DC gain value indicates a ratio of 1/10 between the output conductance and transconductance of the transistors fabricated in ultra-deep-submicron CMOS technologies. On the basis of the simulated value, a nominal gain of 22-26 dB was selected for the transconductors in each gm-C filter implementation of this work. Hence, the negative resistance circuit was required to enhance the transconductor DC gain by 5-9 dB in order to achieve the nominal DC gain value that was chosen. Because of this narrow required tuning range, there were no instability problems with the negative resistance circuit that was used.

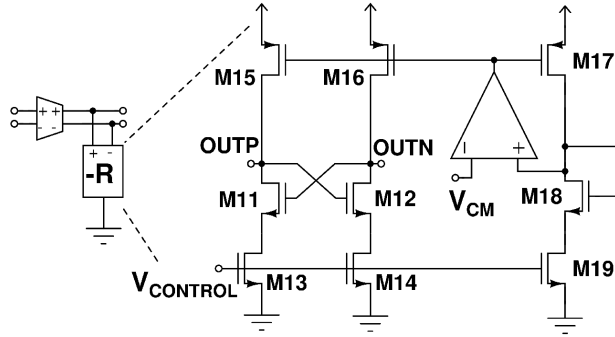


Figure 6.6. Negative resistance circuit [2] (© 2007 IEEE).

The core of the negative resistance circuit consists of the NMOS transistors  $M_{11}$ - $M_{14}$ . The tuning of the negative resistance and, consequently, the DC gain of the transconductors is accomplished by controlling the gate-source voltage of the degeneration transistors  $M_{13}$  and  $M_{14}$ .  $V_{CONTROL}$  is equal for all negative resistance loads. It is worth mentioning that in all the experimental filter circuits of this work, the value of the analog control voltage  $V_{CONTROL}$  was set manually. The transistors  $M_{15}$ - $M_{19}$  and a differential stage generate an accurate bias voltage for the circuit.

A parallel negative conductance  $G_{neg} = 1/R_{neg}$  reduces the finite output conductance  $g_{out} = 1/r_{out}$  of the transconductor. Therefore, the output resistance,  $r_{out}'$ , which is increased, enhances the DC gain of the transconductor

$$A_{v,transconductor} = gm_1 \cdot \frac{1}{g_{out} + G_{neg}} = gm_1 \cdot r_{out}' \quad (6.8)$$

As a drawback, the output conductance of the transconductor becomes more non-linear. The output conductance dominated the transconductor linearity at frequencies much lower than the transconductor unity-gain frequency (i.e. in the in-band) when the transconductor was simulated as a stand-alone circuit in the open loop. The in-band linearity of the transconductor with the negative resistance circuit connected at its output connection was simulated to decrease by 5 dB in the open loop. However, the non-linear transconductance of the transconductors was found to dominate both the in-band and the out-of-band linearity of the fourth-order 240-MHz leapfrog filter circuits.

### 6.3 Filter gain control

This section describes two different ways to control the gain of a gm-C filter. Both the methods described were used in the gm-C filter implementations of this work. In this work, the voltage gain of both 240-MHz low-pass filters that were designed for UWB radio receivers was implemented to be adjustable with a gain range of 34 dB in 1-dB gain steps. To achieve an accurate filter frequency response, the transconductances and the associated parasitic capacitances of the filter building blocks cannot be varied. The only exception is the first transconductor,  $G_{m1}$  in Fig. 6.1, the transconductance of which can be controlled without affecting the filter frequency response. Therefore, in the 240-MHz filter implementations,  $G_{m1}$  includes five 6-dB gain steps. Fine 1-dB gain steps were implemented in the output buffer to keep the complexity and the parasitic capacitances of  $G_{m1}$  reasonable.

#### 6.3.1 Transconductance control

It was discussed in Section 3.3 that the transconductance of a transconductor can be controlled by switching on and off parallel connected unit transconductors. In this work, the 6-dB gain steps were realized by dividing  $G_{m1}$  into six parallel binary-weighted transconductors, the inputs of which can be individually disconnected from the leapfrog filter input with CMOS switches  $S_{w1}$ , as shown in Fig. 6.7 and 6.8. Dummy transconductors, biased at zero current, are switched in place of the actual transconductors to keep the frequency of the passive pole unchanged. The outputs of the disconnected transconductors remain connected to the filter, while their inputs are connected to the common-mode bias voltage to keep the source impedance seen by the rest of the leapfrog filter unaffected. This corresponds to a constant value of  $Q_{1,eff}$  in (4.18) with all gain settings. However, owing to parasitic Miller capacitances, shown in Fig. 4.4, the input impedance of the disconnected transconductor affects its output impedance and thus, the filter source impedance. To diminish this undesirable effect considerably, the differential NMOS switch  $S_{w3}$  short-circuits the signal path at the input of the disconnected transconductor. In addition to  $S_{w3}$ , the minimum-size switches  $S_{w2}$  are needed to bias the disconnected transconductor.

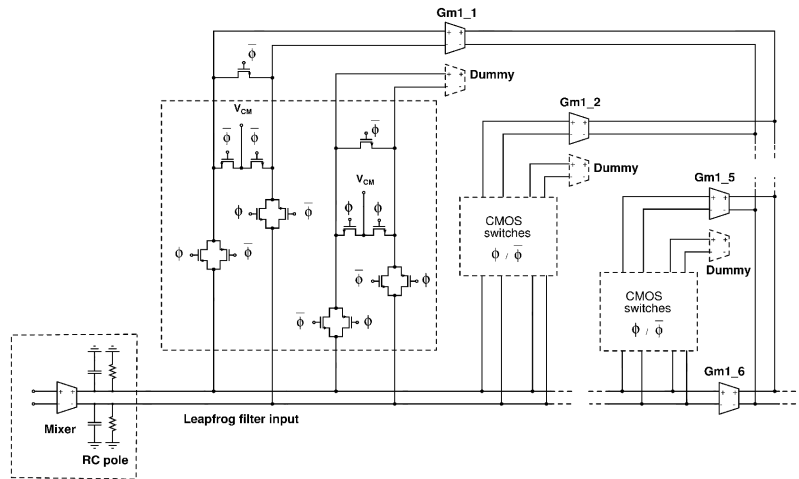


Figure 6.7. Transconductance control in transconductor  $G_{m1}$ .

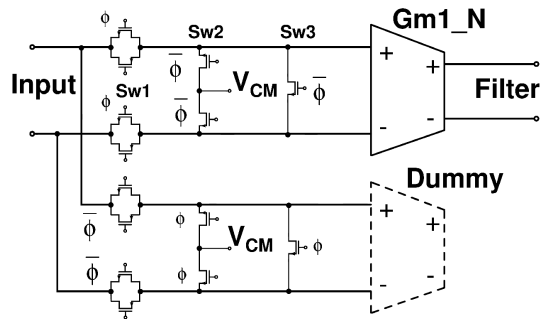


Figure 6.8. Gain control slice from the input of transconductor  $G_{m1}$  [1] (© 2009 IEEE).

### 6.3.2 Switched-resistor load

In some cases, it is possible to include the input capacitance of the following ADC as a part of the load capacitance of the last filter integrator. However, in the 240-MHz filter circuits that were implemented in this work, the input capacitance ( $\approx 400$  fF) of the following ADC, similarly to that in [13], is of the same order of magnitude as the load capacitor of the last filter stage. Hence, a pseudo-differential output buffer, shown in Fig. 6.9, was added between the filter and the ADC. The buffer consists of an NMOS input transistor pair and a resistive load. The resistive load was used to improve the linearity of the buffer compared to its active load counterpart. The nominal voltage gain of the output buffer, determined by the transconductance of  $M_1$  and the load resistance  $R_1$ , was designed to be 5 dB. The fine 1-dB gain steps from 0 dB to 5 dB were accomplished by switching the resistive load of the output buffer,  $R_2$ . To keep the size of the parasitic

output capacitance (i.e. the bandwidth) and the chip area of the output buffer reasonable, a combination of parallel resistors and series resistors was used, as shown in Fig. 6.10. When Sw1 is switched on, the voltage gain of the output buffer decreases by 1 dB, from 5 dB to 4 dB. Correspondingly, if Sw5 is switched on (i.e. one switch is hot at a time), the voltage gain is reduced by 5 dB, from 5 dB to 0 dB. Because the following ADC in the UWB radio receivers was designed to operate with a 700-mV common-mode bias voltage, the output buffer also includes a  $V_{CM}$  control circuit at its output, as shown in Fig. 6.9.

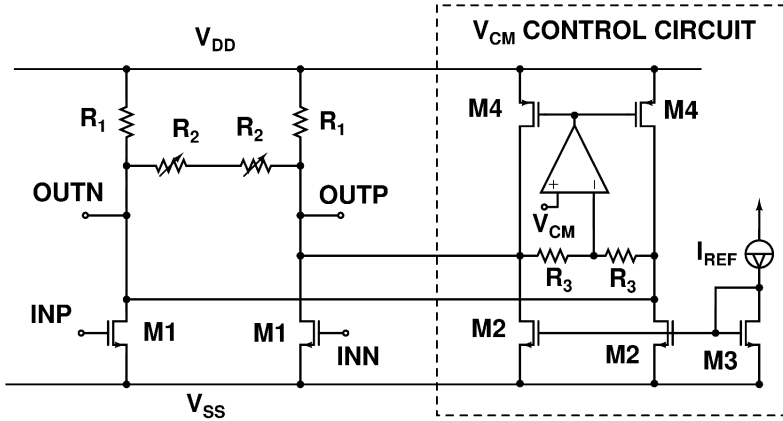


Figure 6.9. Output buffer with the switched-resistor load and  $V_{CM}$  control circuit.

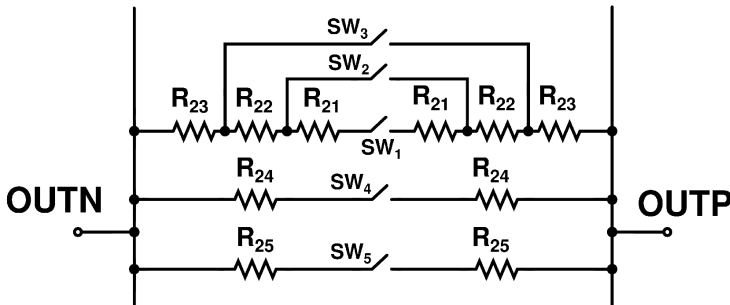


Figure 6.10. Switched resistor load of the output buffer.

### 6.4 Filter cutoff frequency control

It was discussed in Section 3.3 that fundamentally there are two different alternative ways to tune the cutoff frequency of a gm-C low-pass filter against PVT variations, either by means of capacitor matrices or by somehow controlling the transconductance of the transconductors. This

section describes one way to implement a capacitor matrix with metal-metal capacitors and one way to realize transconductance tuning in a pseudo-differential transconductor operating with a low supply voltage. Both the implementations that are described were used in the experimental gm-C filter circuits of this work.

#### 6.4.1 Switched-capacitor matrix

In the 240-MHz filter implementations of this work, the corner frequencies of the passive pole and the 4th-order leapfrog filter were controlled separately with 5-bit switched capacitor matrices,  $C_1$ - $C_5$  in Fig. 6.1. The separate controls are required because the corner frequency of the passive pole is dependent on the source resistance, which is the load of the preceding mixer, while the corner frequency of the leapfrog filter is proportional to the transconductance of the transconductors. The schematic of the capacitor matrices implemented in this work, including a fixed capacitor ( $C_0$ ) and five binary-weighted switched capacitors ( $C_k$ ), is shown in Fig. 6.11.  $C_k$  could be switched on and off with the NMOS switches  $S_{w4}$ . However, the finite on-resistance of the switches degrades the Q-factor of the capacitor matrix. To design small on-resistance with reasonably sized switches, a differential binary-weighted NMOS switch  $S_{w5}$  is added to the circuit.

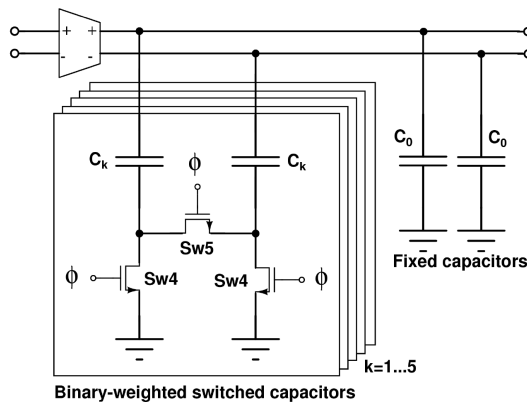


Figure 6.11. 5-bit switched capacitor matrix [1] (© 2009 IEEE).

In general, the loss of a capacitor degrading the capacitor Q-factor can be represented by a shunt conductor, as shown in Fig. 4.4. In (4.18) the Q-factor of the capacitors is also taken into account. It was concluded in Section 4.2.2 that in order to reduce the factor  $A_{DC}/Q_{cap,n}$  to zero, the capacitor matrices are required to have a high Q-value. In Fig. 6.11,  $C_k$  is a metal-metal capacitor. In the experimental 240-MHz filter implemented in

a 0.13- $\mu\text{m}$  CMOS technology [2], metal-insulator-metal (MIM) capacitors were available, while in the experimental 240-MHz filter realized in a 65-nm CMOS technology [1], metal finger capacitors were used.  $C_o$  consists partially of a metal-metal capacitor  $C_{o,metal}$  and partially of the parasitic input and output capacitance of the transconductors, including parasitic wiring capacitances. From the Q-factor point of view, the worst case arises when each  $C_k$  are switched on by  $S_{w5}$ . The smaller the on-resistance of  $S_{w5}$  is designed, the higher the Q-factor of the capacitor matrix is, but the larger the parasitic capacitance of  $S_{w5}$  also becomes. When  $S_{w5}$  is switched off, its parasitic capacitance  $C_{Sw5,k}$  is connected in series with  $C_k$ . Therefore, part of  $C_k$  will remain connected and the remainder can be represented by

$$C_{k,off} = \frac{C_k C_{Sw5,k}}{C_k + C_{Sw5,k}}. \quad (6.9)$$

$C_{k,off}$  increases with the size of  $S_{w5}$ . The required frequency tuning range of the filter integrators sets the requirement for both the minimum and the maximum capacitance values of the capacitor matrix. The capacitor matrix has its minimum value when each  $C_k$  are unconnected. The maximum value is achieved, when each  $C_k$  are switched on. As a result of the minimum capacitance requirement, the fixed capacitor  $C_o$  has to be reduced by  $\sum_{k=1}^5 C_{k,off} \leq C_{o,metal}$ . Correspondingly, because of the maximum capacitance requirement, every  $C_k$  has to be increased by  $C_{k,off}$ . Hence,  $C_o$  decreases and  $C_k$  increases with an increase in the size of  $S_{w5}$ . Simultaneously, the Q-factor of the capacitor matrix decreases because more and more capacitance is moved from the fixed part to the series with the on-resistance of  $S_{w5}$ . As a trade-off result, the size of  $S_{w5}$  is dimensioned in such a way that  $\sum_{k=1}^5 C_{k,off} = C_{o,metal}$ . With this selection, the required frequency tuning range is achieved and the simulated Q-factor of the capacitor matrices was around 100, which causes negligible error in the filter frequency response.

In the capacitor matrices of the first 240-MHz filter implementation, the capacitance value of the fixed capacitor  $C_o$  is 60 % of the nominal capacitance values  $C_{nom} = C_0 + C_2 + C_3$ . Approximately 63 % of the fixed capacitance  $C_o$  consists of controlled parasitic capacitance that includes the parasitic input and output capacitance of the transconductors and of the negative resistance circuit that are connected to the corresponding filter node as well as parasitic wiring capacitance at the corresponding filter node. In this work, the term *controlled parasitic capacitance* means that the parasitic input and output capacitances of the transconductors and of





## 6.5 DC offset compensation

The importance of compensating for the DC offset in integrated radio receivers, and direct-conversion receivers in particular, was briefly discussed in Section 2.2.5. A 6-bit current-steering DAC (IDAC) that was designed and implemented both in 0.13- $\mu\text{m}$  and 65-nm CMOS technologies to compensate for DC offset in the experimental gm-C filter circuits of this work is shown in Fig. 6.13. It uses rather a conventional structure in which the output DC current from LSB to MSB is generated by means of binary-weighted PMOS current sources, M1-M6, and a current-steering array constructed from binary-weighted PMOS switch pairs. The DC current that is generated is injected into the input of the low-pass filter through an output stage with a CM control circuit. The placement of the IDAC in the low-pass filter was shown in Fig. 6.1. In this work, the LSB DC current was selected to be 1  $\mu\text{A}$ . It results in a 0.5-mV voltage difference between the balanced output branches of a preceding downconversion mixer owing to the 500- $\Omega$  load resistor of the mixer used in each experimental receiver circuit that are presented in Chapter 7. Correspondingly, a 40- $\mu\text{A}$  DC current was selected for  $I_{\text{BIAS1}}$  and  $I_{\text{BIAS2}}$  to guarantee the correct operation of the circuit with all the DC current differences generated between the differential output nodes of the circuit by means of the current steering.

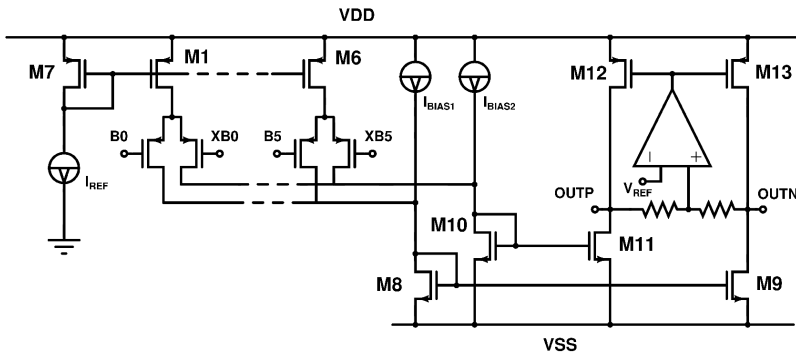


Figure 6.13. 6-bit current-steering DAC.

In addition to the employment of an IDAC, the other most frequently used DC offset compensation schemes include AC coupling, a DC feedback loop, and a feedforward DC offset removal scheme. The AC coupling is implemented by placing a series AC coupling capacitor at the mixer-baseband interface, between the output of the downconversion mixer and the input of the following analog baseband circuit, as discussed and used in, for example, [14] and [15], respectively. The DC feedback loop typically consists of a low-pass pole sensing the DC offset at the circuit output and a

subtractor removing the DC offset at the circuit input. A DC offset that is sensed at the circuit output is fed back into the circuit input with reverse polarity in order to remove the DC offset from the input signal of the circuit. The DC offset loop is discussed and used in, for example, [16]-[17] and [18]-[19], respectively. In the feedforward DC offset removal scheme, the DC offset is sensed at the circuit input with a low-pass pole. The DC offset that is sensed at the input is connected to the circuit output for subtraction by means of a feedforward path parallel to the main signal path [20]. The AC coupling and DC feedback loop schemes correspond to a high-pass filtering of the spectrum of the signal that is received. Several modulation schemes used in wireless communication systems, and potentially also in other radio systems (e.g. radar applications), have a significant signal content at DC. In those radio systems, any high-pass filtering will lead to a loss of information and cause severe degradation in BER. A general-level discussion of the long time constants typically related to DC offset compensation schemes in integrated radio receivers is given in, for example, [21].

## 6.6 Common-mode induced even-order distortion

In this section, the effect of the lack of an input common-mode rejection of a pseudo-differential gmC-filter in a direct-conversion receiver is studied. The system that is studied consists of a differential mixer and a gm-C baseband filter with a passive pole at the input. In addition to the basic second-order non-linearity resulting from mismatch, two additional error mechanisms specific to pseudo-differential circuits are found and analyzed. Even-order distortion in the common-mode signal, which is due to the mixer, is found to leak back to the differential path. Furthermore, an interfering signal in the filter common-mode input will, even under perfect matching, produce signal distortion by modulating the transconductance. This section is based on [22] and thus, it is original work in this thesis<sup>5</sup>.

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<sup>5</sup>This section is based on [22] (© 2007 IEEE).

### 6.6.1 Introduction

One of the most limiting problems in direct-conversion receivers is the envelope distortion resulting from the even-order non-linearities [23]. The even-order non-linearities, together with mismatches in the RF front-end, produce even-order intermodulation distortion and DC offset at the input of the following low-pass filter. Because of the nature of the even-order distortion, the polarity information of the phase is removed and hence the distortion is common-mode. Generally, a common-mode signal at the input of the low-pass filter is not a problem as long as the common-mode rejection ratio of the filter is sufficiently high. However, when designing wideband gm-C filters using modern deep-submicron CMOS technologies with low supply voltages, a favourable choice is to utilize pseudo-differential transconductors [24]. The inherent common-mode rejection of a pseudo-differential transconductor is poor [5]. Thus, if the filter has a finite common-mode rejection ratio, the effect of a common-mode input signal on the even-order intermodulation distortion of the filter may not be negligible. Furthermore, it may not always be possible to eliminate interfering signals with filtering. This is the case, for example, in an ultra-wideband (UWB) receiver where some, potentially high-power, interferers are located very close to the receive band.

The intermodulation distortion of gm-C filters has been analyzed in the literature [25], [26]. The distortion analysis that is presented typically focuses on odd-order non-linearity. However, in certain applications, such as direct-conversion radio receivers, the even-order non-linearity plays a crucial role and, thus, cannot be neglected. Obtaining high even-order linearity typically relies on differential signals and balancing the signal paths. However, this does not eliminate the distortion but merely restricts it to a common-mode signal component, which is of no consequence if it is assumed that the preceding stage can reject it. Clearly, a pseudo-differential transconductor that has no inherent common-mode rejection may pose a problem in this case.

### 6.6.2 System scenario

Fig. 6.14 shows a block diagram of a direct-conversion receiver. The most dominant second-order distortion source in the RF front-end is the downconversion mixer [23]. The real pole between the mixer and the low-pass filter implemented with passive components will attenuate out-of-band interfering and blocking signals, thus improving the stopband linearity of the filter compared to a fully active implementation. For the sake of simplicity, the first transconductor  $G_{m1}$  is assumed to dominate the

second-order distortion of the filter.  $Gm_1$  is assumed to have an ideal common-mode feedback circuit and hence the common-mode voltage gain of  $Gm_1$  is close to zero. Therefore, no common-mode signal at the input of the filter is present at the output of  $Gm_1$  any longer. This is, of course, not the case, but even some amount of common-mode rejection will significantly reduce the effect of the following stages, thus justifying the simplification.

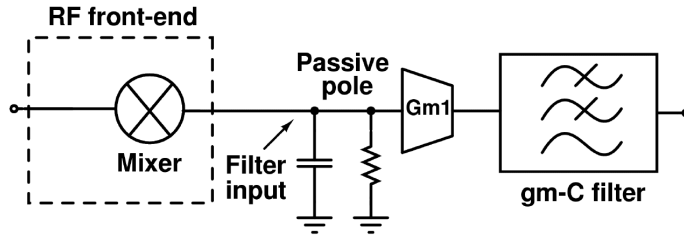


Figure 6.14. Block diagram of a direct-conversion receiver [21] (© 2007 IEEE).

The analysis presented in this section is based on the scenario where the input of the gm-C filter is presented with a differential two-tone signal in the stopband and a common-mode signal in the passband of the filter. The linearity results obtained with a two-tone signal can be related to any amplitude-varying modulation [27]. The common-mode signal is assumed to originate from a varying amplitude blocker distorted by the preceding mixer.

### 6.6.3 Mismatch model for the transconductor

The schematic of the pseudo-differential transconductor  $Gm_1$  with an ideal common-mode feedback circuit is shown in Fig. 6.15. The transconductor can be modeled with a voltage-controlled current source (VCCS). The dominant non-linearity source in  $Gm_1$  is assumed to be its transconductance  $gm_t$ . This is not generally valid as a result of the non-linear output conductance  $g_o$  of  $Gm_1$ , but it can be assumed that all the significant non-linearities of  $Gm_1$  can be referred to its transconductance  $gm_t$ . A similar approach has been used to characterize the fundamental non-linearity of a transconductance mixer in [23]. Since the second-order non-linearities are assumed to dominate the even-order non-linearities in the filter, the non-linear VCCS is represented as

$$i_{OUT}(t) = I_{DC} + gm_t \left[ v_{IN}(t) + \alpha_2 v_{IN}^2(t) \right], \quad (6.10)$$

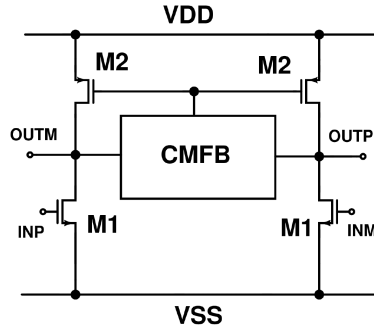


Figure 6.15. Schematic of the pseudo-differential transconductor Gm1 [22] (© 2007 IEEE).

where  $\alpha_2''$  is the relative second-order non-linear coefficient. Its value can be predicted by the simulations from a single-ended output of Gm1 by applying only a single-ended signal to the input [23].

Assuming the transistor drain current follows the basic square law, its transconductance is given by

$$gm = \beta(V_{GS} - V_{TH}), \quad (6.11)$$

where  $\beta = \mu C_{ox} W / L$  is the current factor. The standard deviation of  $gm$  can be calculated from the variance of the current factor and of the threshold voltage [28]

$$\begin{aligned} \sigma(\Delta gm) &= \sqrt{\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{\sigma^2(\Delta V_{TH})}{(V_{GS} - V_{TH})^2}} \\ &= \sqrt{\frac{A_\beta^2}{WL} + \frac{A_{VTH}^2}{WL(V_{GS} - V_{TH})^2}}. \end{aligned} \quad (6.12)$$

In (6.12)  $A_\beta$  and  $A_{VTH}$  are process-related constants. It should be noted that deep-submicron transistors can deviate quite significantly from (6.11), which means that the results obtained from (6.12) are only suggestive.

## 6.6.4 Even-order distortion analysis

### 6.6.4.1 Two-tone differential input signal and IMD2

In the first case that was studied, the low-pass filter is assumed to suffer from mismatch and to have a two-tone differential input signal. This will cause second-order intermodulation distortion at the output of the input transconductor Gm1. Furthermore, Gm1 is assumed to dominate the stop-

band linearity of the filter. The differential IF input signal of a two-tone test coming from the preceding mixer can be represented as

$$v_{in}(t) = A_{IF} [\cos(\omega_{IF1}t) + \cos(\omega_{IF2}t)]. \quad (6.13)$$

Mismatches between the positive and negative signal paths in the RF front-end cause amplitude and phase imbalance between the positive and negative input signals of the filter. However, in this analysis, the signal imbalance is treated as a non-zero common-mode component. Therefore, the positive and negative input signals of the filter,  $+(1/2)v_{in}$  and  $-(1/2)v_{in}$ , are considered to be amplitude- and phase-balanced. The assumption of phase balance implies that the common-mode signal is in phase with the differential signal. This is not necessarily the case, but it was found to have a negligible effect on the results. The transconductance of Gm1 can be given as  $gm_{1P} = gm_1(1 + \Delta gm_1 / 2)$  and  $gm_{1M} = gm_1(1 - \Delta gm_1 / 2)$  for the positive and negative signal paths, respectively. The relative second-order non-linear coefficients  $\alpha_2''$  of  $gm_{1P}$  and  $gm_{1M}$  are assumed to be equal. The gain (i.e. attenuation) of the real pole is represented by the coefficient  $G_{RC}(\omega)$ , which is assumed to be equal for both signal paths. When only the other fundamental signal tone and the second-order non-linear components around the DC are considered, the positive output current of Gm1 becomes

$$\begin{aligned} i_{OUTP}(t) &= gm_{1P} \frac{1}{2} A_{IF} G_{RC}(\omega_{IF1}) \cos(\omega_{IF1}t) \\ &+ gm_{1P} \alpha_2'' \frac{1}{4} A_{IF}^2 G_{RC}^2(\omega_{IF1}) \cos(\omega_{imd2}t) \\ &+ I_{DC} + gm_{1P} \alpha_2'' \frac{1}{4} A_{IF}^2 G_{RC}^2(\omega_{IF1}). \end{aligned} \quad (6.14)$$

The negative output current can be expressed in a similar way. In (6.14), the low-frequency beat is denoted by  $\omega_{imd2} = \omega_{IF1} - \omega_{IF2}$ . The differential output current, including only the frequency components of interest, is

$$\begin{aligned} i_{OUT}(t) &= i_{OUTP}(t) - i_{OUTM}(t) \\ &= gm_1 A_{IF} G_{RC}(\omega_{IF1}) \cos(\omega_{IF1}t) \\ &+ gm_1 \Delta gm_1 \alpha_2'' \frac{1}{4} A_{IF}^2 G_{RC}^2(\omega_{IF1}) \cos(\omega_{imd2}t) \\ &+ gm_1 \Delta gm_1 \alpha_2'' \frac{1}{4} A_{IF}^2 G_{RC}^2(\omega_{IF1}). \end{aligned} \quad (6.15)$$

In order for the IIP2 of the filter to be calculated, the  $imd2$  term in (6.15) has to be referred to the input of the filter by  $gm_i$  and by the transfer function of the real pole

$$v_{imd2,in}(t) = \Delta gm_1 \alpha_2'' \frac{1}{4} A_{IF}^2 \frac{G_{RC}^2(\omega_{IF1})}{G_{RC}(\omega_{imd2})}. \quad (6.16)$$

The in-band gain of the real pole is assumed to be one (i.e.,  $G_{RC}(\omega_{imd2}) = 1$ ). The IIP2 can then be calculated from the fundamental term of the original input signal in (6.13) and the input-referred  $imd2$  term in (6.16) as

$$\begin{aligned} IIP2[dBV] &= 2P_{FUND,IN}[dBV] - P_{IMD2,IN}[dBV] \\ &\Leftrightarrow 20 \log\left(\frac{iip2}{\sqrt{2}}\right) = 2 \cdot 20 \log\left(\frac{|\alpha_1| A_{IF}}{\sqrt{2}}\right) - 20 \log\left(\frac{|\alpha_2| A_{IF}^2}{\sqrt{2}}\right) \\ &\Leftrightarrow iip2 = \frac{|\alpha_1|}{|\alpha_2|} = \frac{4}{\Delta gm_1 \alpha_2'' G_{RC}^2(\omega_{IF1})}. \end{aligned} \quad (6.17)$$

This is a peak voltage value, which is usually stated as  $IIP2[dBV] = 20 \log(iip2 / \sqrt{2})$  in the filter design.

#### 6.6.4.2 Common-mode input signal and IMD2

In this subsection, the common-mode-to-differential conversion of the filter suffering from mismatch is studied. As a result, the second-order intermodulation distortion at the output of Gm1 will increase. The RF front-end produces a common-mode even-order  $imd2$  term at the output of the mixer [23]. Thus, the common-mode signal coming from the mixer can be represented as

$$v_{CM,IN} = A_{CM} \cos(\omega_{imd2}t). \quad (6.18)$$

Similarly to (6.14) and (6.15), the differential output current of Gm1 can be represented as

$$\begin{aligned} i_{OUT}(t) &= i_{OUTP}(t) - i_{OUTM}(t) \\ &= gm_1 \Delta gm_1 A_{CM} \cos(\omega_{imd2}t) \\ &\quad + gm_1 \Delta gm_1 \alpha_2'' \frac{1}{2} A_{CM}^2, \end{aligned} \quad (6.19)$$

when only the second-order non-linear components around the DC are considered. The  $imd2$  term in (6.19) can be referred to the input of the filter by  $gm_i$  and by the transfer function of the real pole



$$v_{imd2,in}(t) = \Delta gm_1 A_{CM} \cos(\omega_{imd2} t) . \quad (6.20)$$

Equation (6.20) represents the input-referred  $imd2$  term, which is produced as a result of the mismatches in the NMOS input transistor pair of Gm1 when a common-mode signal is applied to the input. However, the mismatches in the PMOS load pair will also produce a differential output current, because the PMOS transistors are in the common-mode signal path. Since Gm1 is assumed to have an ideal common-mode feedback circuit, the common-mode input signal at the gate of the PMOS transistors is

$$v_{CM,IN,PMOS} = \frac{gm_1}{gm_2} v_{CM,IN} . \quad (6.21)$$

Thus, the differential output current of Gm1 as a result of the PMOS transistor pair suffering from the mismatch is

$$\begin{aligned} i_{OUT}(t) &= i_{OUTP}(t) - i_{OUTM}(t) \\ &= gm_2 \Delta gm_2 \frac{gm_1}{gm_2} A_{CM} \cos(\omega_{imd2} t) \\ &\quad + gm_2 \Delta gm_2 \alpha_2 \frac{1}{2} \left( \frac{gm_1}{gm_2} \right)^2 A_{CM}^2 . \end{aligned} \quad (6.22)$$

When the  $imd2$  term in (6.22) is referred to the input of the filter by  $gm_i$  and by the transfer function of the real pole, it can be written

$$v_{imd2,in}(t) = \Delta gm_2 A_{CM} \cos(\omega_{imd2} t) . \quad (6.23)$$

As can be seen from (6.20) and (6.23), the input-referred  $imd2$  term is a function of the mismatch of  $gm_i$  and  $gm_2$ . The standard deviation for these two independent mismatch sources is

$$\sigma(\Delta gm_{tot}) = \sqrt{\sigma^2(\Delta gm_1) + \sigma^2(\Delta gm_2)} . \quad (6.24)$$

and hence the input-referred  $imd2$  term can be rewritten as

$$v_{imd2,in}(t) = \Delta gm_{tot} A_{CM} \cos(\omega_{imd2} t) . \quad (6.25)$$

This term will be summed with the  $imd2$  term in (6.15) and the IIP2 of the filter can then be calculated by (6.16). The  $imd2$  term in (6.25) can be compared to the “conventional”  $imd2$  term of (6.16) by means of a ratio expressed as

$$\frac{imd2_{CM-to-diff}}{imd2_{two-tone}} = \frac{4 \cdot \Delta gm_{tot} A_{CM}}{\Delta gm_1 \alpha_2'' A_{IF}^2 G_{RC}^2(\omega_{IF1})}. \quad (6.26)$$

In Section 6.6.5, (6.26) is used to estimate the significance of the  $imd2_{CM-to-diff}$  term when compared with the  $imd2_{two-tone}$  term.

#### 6.6.4.3 Common-mode input signal and modulation

In the last case that was studied, an interfering signal is present at the filter common-mode input, which will, even under perfect matching, produce signal distortion by modulating the transconductance of Gm1. The input signal of the filter consists of a potentially large common-mode signal and a weak desired differential signal:

$$\begin{cases} v_{INP}(t) = A_{CM} \cos(\omega_{imd} 2t) + \frac{1}{2} A_{BB} \cos(\omega_{BB} t) \\ v_{INM}(t) = A_{CM} \cos(\omega_{imd} 2t) - \frac{1}{2} A_{BB} \cos(\omega_{BB} t) \end{cases}, \quad (6.27)$$

where the  $BB$  term represents a weak desired in-band signal. The real pole does not attenuate either of these in-band components. Studies have already been performed of how the mismatches, in addition to the fundamental even-order non-linearity of Gm1, affect the input-referred  $imd2$  term when a differential or a common-mode signal is present at the input of the filter. Therefore, now the positive and negative signal paths of Gm1 are assumed to be fully balanced (i.e. no mismatch is present). The differential output current of Gm1 becomes

$$i_{OUT}(t) = gm_1 \left[ 1 + 2\alpha_2'' A_{CM} \cos(\omega_{imd} 2t) \right] \cdot A_{BB} \cos(\omega_{BB} t). \quad (6.28)$$

Hence, the common-mode signal modulates the transconductance  $gm_1$  seen by the desired differential signal.

### 6.6.5 Numerical examples

As an example, a pseudo-differential transconductor of Fig. 6.15 is simulated using 0.13- $\mu\text{m}$  CMOS technology foundry models for the transistors. The simulated relative second-order non-linear coefficient of the NMOS transistor is 0.917 for a  $V_{GS} - V_{TH}$  of 360 mV. Equation (6.17) is verified by a two-tone test simulation applying a 4% mismatch ( $\Delta gm_i$ ) to the NMOS input transistor pair of Gm1. The simulated IIP2 of Gm1 is +37 dBV, which corresponds with the IIP2 calculated from (6.17). Correspondingly, (6.25) and (6.28) are verified with simulations.

According to [23], the differential signal at the output of a single-balanced transconductance mixer is

$$A_{IF} = -\frac{2}{\pi} g_{m_{mixer}} R_L A_{RF}, \quad (6.29)$$

when  $\eta_{nom} = 1/2$  and  $\Delta\eta \approx 0$ . Furthermore, the common-mode signal at  $\omega_{md2}$  at the output of a single-balanced transconductance mixer is [23]

$$\begin{aligned} A_{CM} &= \eta_{nom} \alpha_2' g_{m_{mixer}} R_L A_{RF}^2 \left(1 + \frac{\Delta\eta \cdot \Delta R}{2}\right) \\ &\approx \frac{1}{2} \alpha_2' g_{m_{mixer}} R_L A_{RF}^2. \end{aligned} \quad (6.30)$$

When (6.29) and (6.30) are substituted into (6.26), it can be written

$$\frac{imd2_{CM-to-diff}}{imd2_{two-tone}} = \frac{\pi^2 \Delta g_{m_{tot}} \alpha_2'}{2 \Delta g_{m_1} \alpha_2'' g_{m_{mixer}} R_L G_{RC}^2(\omega_{IF1})}. \quad (6.31)$$

The size of the PMOS load transistors in Gm1 is typically larger compared to the size of the NMOS input transistors with the uniform drain bias currents. Therefore, on the basis of (6.12) and (6.24),  $\Delta g_{m_{tot}} \approx \Delta g_{m_1}$ . In addition, the value of the relative second-order non-linear coefficient of the CMOS transconductance mixer  $\alpha_2'$  can be assumed to be close to the value of  $\alpha_2''$ . When the gain of the mixer and the attenuation of the passive pole at  $\omega_{F1}$  are assumed to be 10 dB,

$$\frac{imd2_{CM-to-diff}}{imd2_{two-tone}} = \frac{\pi^2}{2 \cdot 10^{10/20} \cdot (10^{-10/20})^2} \approx 0.88. \quad (6.32)$$

This example shows that the  $imd2_{CM-to-diff}$  term can be significant when compared with the  $imd2_{two-tone}$  term.

Let us finally estimate the ratio between the modulated part of  $g_{m_i}$  and the original value of  $g_{m_i}$  in (6.28)

$$\frac{g_{m_{i,mod}}}{g_{m_{i,orig}}} = 2\alpha_2'' A_{CM} = (\alpha_2'')^2 g_{m_{mixer}} R_L A_{RF}^2, \quad (6.33)$$

where  $A_{CM}$  is replaced by (6.30). When it is assumed that the stop-band attenuation of the preselect filter of the receiver is of the same order of magnitude as the gain of the low-noise amplifier, an out-of-band blocker as

large as  $-10$  dBV at the antenna connector will not attenuate before the mixer input. Hence, from (6.33)

$$\frac{gm_{1,\text{mod}}}{gm_{1,\text{orig}}} = (0.917)^2 \cdot 10^{10/20} \cdot \left(\sqrt{2} \cdot 10^{-10/20}\right)^2 \approx 0.53, \quad (6.34)$$

which is not negligible.

### 6.6.6 Conclusions of the analysis

The inability of pseudo-differential circuits to reject common-mode input signals can potentially give rise to signal distortion. The specific scenario of a mixer and a gm-C baseband filter in a direct-conversion receiver was studied. Two error mechanisms originating from the combination of even-order distortion of the mixer and the lack of input common-mode rejection in the filter were found. Analysis suggests that the common-mode leakage is slightly lower than the distortion resulting from the IIP2 of the gm-C filter, while the impact of transconductance modulation depends heavily on the interference scenario.

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## 7 Experimental CMOS gm-C filter circuits

In this chapter, a total of three continuous-time gm-C low-pass filter implementations are presented, together with their measured performance. They include two evolution versions of fifth-order 240-MHz gm-C filters that were designed and implemented in this work as a part of two single-chip WiMedia UWB direct-conversion receivers in a standard 0.13- $\mu\text{m}$  and 65-nm CMOS technology, respectively. The 65-nm CMOS filter implementation was also embedded into the I-branch of a single-chip 60-GHz dual-conversion receiver. Correspondingly, a third-order 1-GHz gm-C filter was designed for the Q-branch, rather as a test structure. The 1-GHz design is the third experimental gm-C filter circuit implemented in this work. All three filter implementations are original work in this thesis. Moreover, all of them were synthesized from lossy LC prototype filters in order to investigate and demonstrate the feasibility of the filter design approach presented in Chapter 4 and, especially, to benefit from the approach. The fifth-order 240-MHz gm-C filter implementations have previously been published in [1] and [2], respectively. The 1-GHz filter implementation has not been published because it did not function properly in the measurements, unlike the simulations. The second evolution version of the two WiMedia UWB receivers and the 60-GHz radio receiver, both implemented in a 65-nm CMOS technology, have been published in [3] and [4]-[5], respectively. To the best of the author's knowledge, and based on [5], the latter is the first published 60-GHz radio receiver implementation that also contains an analog baseband circuit with an ADC on the same silicon chip with a 60-GHz receiver front-end. In the first evolution version of the two WiMedia UWB receivers, some re-design and, hence, re-processing needed to be done for the RF front-end and therefore, the first UWB receiver implementation has not been published as a complete RF receiver circuit. Instead, each individual circuit block has been published separately. This chapter is mainly based on the contents of the first four references of this chapter<sup>6</sup>.

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<sup>6</sup>Portions of this chapter are taken from [1] (© 2007 IEEE), [2] (© 2009 IEEE), [3] (© 2008 IEEE), and [4] (© 2009 IEEE).

The WiMedia UWB radio technology plays an important role in the low-voltage wideband gm-C filter implementations of this work and, in fact, it was one of the main motivators for this thesis. The WiMedia UWB radio technology was reviewed in Chapter 2. Correspondingly, Section 7.1 is devoted to giving an overview of the filter requirements in the WiMedia UWB direct-conversion receivers that were under development at the time when the 240-MHz low-pass filters were designed. Next, in Section 7.2, the first evolution version of the low-pass filters designed for a WiMedia UWB receiver is presented, together with the experimental results. It should be pointed out that in principle, all three gm-C filter circuits implemented in this work are similar to the one shown in Fig. 6.1. Hence, they consist of a real pole placed at the filter input, a gm-C filter realizing the complex pole pairs of the filter transfer function, an output buffer designed to drive a following ADC or a limiting amplifier chain, and a current-steering DAC for the DC offset compensation. The circuit techniques that were used in the design and implementation of the gm-C filter circuits were described extensively in the previous chapter. Therefore, the gm-C filter implementations are presented in this chapter by referring to Chapter 6 and the main emphasis is on the experimental results. The second WiMedia UWB receiver implementation and the 60-GHz radio receiver with the corresponding low-pass filter implementations are presented in Sections 7.3–7.4, respectively, together with the experimental results. It was already emphasized in Chapter 5 that, in this work, it is important to give an overview of the complete RF receivers for which the experimental filter circuits were designed and to show the overall measured performance of the receivers as well. The experimental results of the three low-pass filter implementations are summarized in Section 7.5, in addition to a comparison of the 240-MHz filters of this work to the work of others.

## 7.1 Filter requirements in WiMedia UWB receivers

The two 240-MHz low-pass filters that were designed and implemented in this work are intended to fulfill the performance requirements of the analog baseband block in a WiMedia UWB radio receiver between a constant-gain RF front-end and a low-resolution 5-bit ADC, for example a similar ADC as reported in [6]. The passband edge frequency of a low-pass filter intended for a WiMedia UWB receiver has to be in the range of 240 MHz in order to receive a MultiBand-OFDM signal using a direct-conversion topology. According to [7], the minimum sensitivity of a WiMedia UWB receiver is  $-80$  dBm. The voltage gain of the preceding RF front-end is 27 dB on the basis of [8] and the desired full-scale level of the 5-bit ADC can be assumed



to be  $-23$  dBV<sub>rms</sub> for an MB-OFDM signal. Thus, the baseband filter is required to have approximately 40 dB of voltage gain. In the first and second designs, the filters have an adjustable gain control from 13 dB to 48 dB and from 9 dB to 43 dB, respectively, in 1-dB gain steps in order to amplify both minimum and maximum received in-band signals to the desired full-scale level of the following ADC. The noise figure (NF) of the RF front-end can be assumed to be 5 dB [8]. Allowing a 0.5-dB degradation in the NF of the whole receiver with a 27-dB RF front-end gain, the requirement for the input-referred noise density of the filter becomes as low as 8.8-nV/ $\sqrt{\text{Hz}}$ . To alleviate the stringent stopband linearity requirement of the baseband filter in the targeted UWB application, the LNA of the preceding RF front-end is assumed to include a notch filter, as discussed in Section 2.3. According to the simulations of the prototype filter, the selectivity requirement can be met with a fifth-order low-pass filter. Since the filters are a part of a wideband receiver, a flat in-band frequency response on the part of the filter, i.e. passband ripple lower than 3 dB, is desirable.

## 7.2 A 1.2-V 240-MHz CMOS continuous-time low-pass filter for a UWB radio receiver

An integrated fifth-order 0.13- $\mu\text{m}$  CMOS gm-C low-pass filter for the WiMedia UWB system is presented in this section. This section is based on [1]. The block diagram of the filter corresponds to the one shown in Fig. 6.1. The circuit is intended for a direct-conversion receiver, which in a WiMedia UWB system results in a filter corner frequency requirement of 240 MHz. A fifth-order prototype is selected to suppress interference from concurrently operating radio transmitters in the vicinity or within the same terminal. For example, cellular or WLAN transmitters can interfere with a UWB receiver. As shown in Fig. 6.1, the filter is implemented as a cascade of a real pole placed at the filter input and a fourth-order leapfrog gm-C filter, which realizes the complex pole pairs of the transfer function. The real pole was placed at 250 MHz and implemented with the passive load components of a preceding Gilbert cell-type downconversion mixer, thus improving the stopband linearity of the low-pass filter compared to an active implementation. The filter uses a 1.2-V supply voltage and was synthesized for a transconductor DC gain of 24 dB, as described in Chapter 4. The resulting accuracy requirement with this gain is 1 dB for a 0.3-dB amplitude error at the passband edge. The pseudo-differential transconductor structure that was used in this design was presented in the previous chapter.

The filter includes an adjustable gain control from 13 dB to 48 dB in 1-dB gain steps. The filter gain partitioning is a trade-off between noise, linearity, prototype realizability, and the feasibility of the transconductor size ratios in the filter stages. The latter two were discussed in Chapter 4. In this design, the 48-dB voltage gain is distributed between the first three filter stages and the output buffer. The gain control is divided into 6-dB and 1-dB gain steps implemented in the input transconductor of the filter,  $G_{m1}$  in Fig. 6.1, and the output buffer, respectively. Both filter gain control implementations were presented in Section 6.3. The output buffer is designed to drive the 5-bit ADC that is presented in [6]. A current-steering DAC that was described in Section 6.5 performs the DC offset compensation. The corner frequencies of the passive pole and leapfrog gm-C filter are separately controlled by 5-bit switched-capacitor matrices, the realization of which was described in Section 6.4. The separate controls are required since the leapfrog filter corner frequency is proportional to the transconductance of the transconductors, while the passive pole frequency is dependent on the source resistance, which is the load of the preceding mixer.

The complete RF receiver that was designed and implemented has not been published. However, each circuit block has been published separately. The ADC has been reported in [6], the synthesizer in [9], and an improved (i.e. the second) version of the RF front-end in [8] and [10].

### 7.2.1 Experimental results of low-pass filter

The filter was fabricated in a 0.13- $\mu\text{m}$  CMOS process and the chips were directly bonded onto a PCB. A micrograph of the filter is shown in Fig. 7.1. The active silicon area of the filter is 0.34 mm<sup>2</sup>. The filter includes a test input with an on-chip NMOS buffer and a test output with a CMOS switch in order to measure the filter as a stand-alone circuit. In addition, there is a test structure of an integrator implemented on-chip in order to manually tune the correct gate-source voltage for the negative resistance circuit controlling the DC gain of the filter transconductors, as described in Chapter 6. The test input of the filter was utilized in all measurements. The frequency response and the linearity of the filter were measured using the test output of the filter, while the voltage gain and the noise were measured from the output of the 5-bit ADC [6].

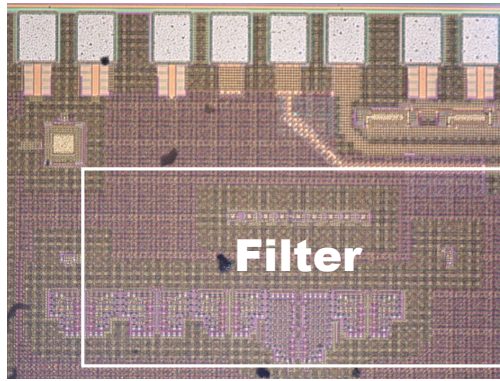


Figure 7.1. Micrograph of the filter [1] (© 2007 IEEE).

The measured and simulated frequency responses of the low-pass filter are shown in Fig. 7.2. The measured frequency response is scaled to 0 dB at 10 MHz. The measured passband edge frequency and  $-3$ -dB frequency are 240 MHz and 265 MHz, respectively. The measured passband ripple is 1.5 dB instead of the targeted 1-dB passband ripple. However, at the stopband of the filter, the designed selectivity is achieved. Considering the wide bandwidth, over 200 MHz, the measured and simulated frequency responses of the filter can be said to compare favorably with each other. It was observed in the simulations that the parasitic Miller capacitances (i.e. between the gate and drain of the NMOS input transistors) of the single-stage transconductors affected the frequency response of the wideband filter. It was observed that the frequency response of a fifth-order gm-C filter resembles the frequency response of a fourth-order filter when the number of minima and maxima at the passband are considered. This effect can be seen both in the measured and simulated frequency responses in Fig. 7.2 and later on in Fig. 7.13. The effect of parasitic Miller capacitances on the integrator equations was theoretically studied in Chapter 4. There also seem to be other second-order effects at the passband of the measured filter which were not modeled in the simulations. After the fabrication of the chip, a Monte Carlo simulation was carried out. That simulation showed that unavoidable mismatches between the transistors affect the filter frequency response at the passband. The measured integral gain errors of the 6-dB and the 1-dB gain steps are presented in Fig. 7.3. The error of an individual 6-dB gain step is approximately 0.1 dB. This accuracy is adequate to guarantee a monotonic filter gain control characteristic.

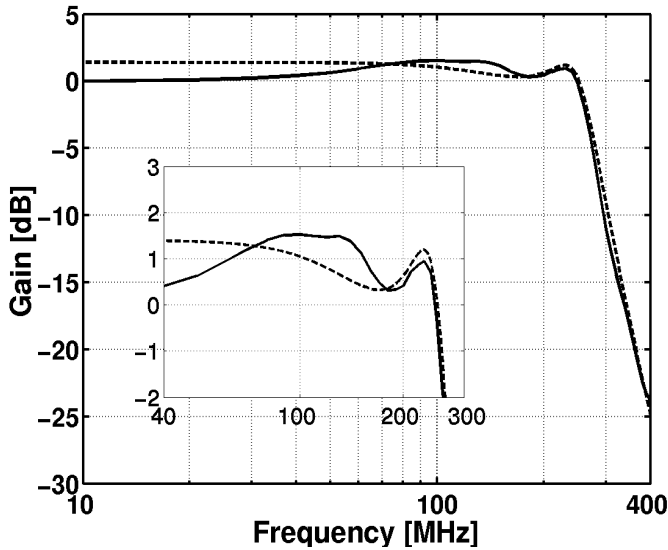


Figure 7.2. Measured (solid line) and simulated (dashed line) filter frequency response [1] (© 2007 IEEE).

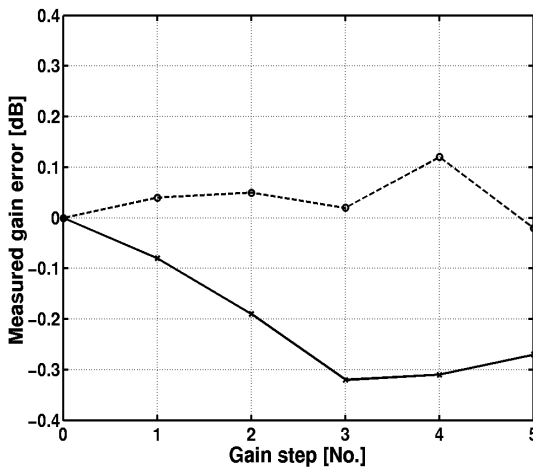


Figure 7.3. Measured gain error of 6-bit (solid line) and 1-bit (dashed line) gain steps.

The measured performance results are collected in Table 7.1. The noise of the filter measured at the ADC output is shown in Fig. 7.4. As can be seen, the in-band noise of the filter is over 15 dB higher than the noise floor of the ADC. The integrated input-referred noise is 117  $\mu\text{V}_{\text{rms}}$ , corresponding to an input-referred noise density as low as 7.7-nV/ $\sqrt{\text{Hz}}$ . This is due to the simple transconductor structure that was used. The noise was integrated from 2 MHz to 233 MHz, which corresponds to the downconverted UWB channel

occupying all the subcarriers. The challenging design goal for a low noise calculated in Section 7.1 was thus achieved. The out-of-band IIP<sub>3</sub> was measured with 400-MHz and 790-MHz test signals. As shown in Fig. 7.5, the measured out-of-band IIP<sub>3</sub> of the filter with the maximum gain is  $-8.2$  dBV. The in-band IIP<sub>3</sub> was measured with 30-MHz and 50-MHz test signals. The measured in-band IIP<sub>3</sub> with the maximum gain is  $-48.2$  dBV, as shown in Fig. 7.6. The out-of-band IIP<sub>2</sub> was measured with 400-MHz and 410-MHz test signals. As shown in Fig. 7.7, the measured out-of-band IIP<sub>2</sub> of the filter with the maximum gain is  $+18.2$  dBV. The filter was measured to consume 24 mW.

Table 7.1. Measured performance [1] (© 2007 IEEE).

Technology	0.13- $\mu$ m CMOS
Supply voltage	1.2 V
Filter order	5
Voltage gain at 10 MHz	12.9 – 47.6 dB
Passband edge frequency	240 MHz
$-3$ -dB frequency	265 MHz
Integrated input-referred noise (2 – 233 MHz)	117 $\mu$ V <sub>rms</sub>
Input-referred noise density	7.7 nV/ $\sqrt{\text{Hz}}$
IIP <sub>3</sub> (in-band, $f_1 = 30$ MHz, $f_2 = 50$ MHz)	$-48.2$ dBV
IIP <sub>3</sub> (out-of-band, $f_1 = 400$ MHz, $f_2 = 790$ MHz)	$-8.2$ dBV
IIP <sub>2</sub> (out-of-band, $f_1 = 410$ MHz, $f_2 = 400$ MHz)	$+18.2$ dBV
Power consumption	24 mW
Die area without pads	0.34 mm <sup>2</sup>

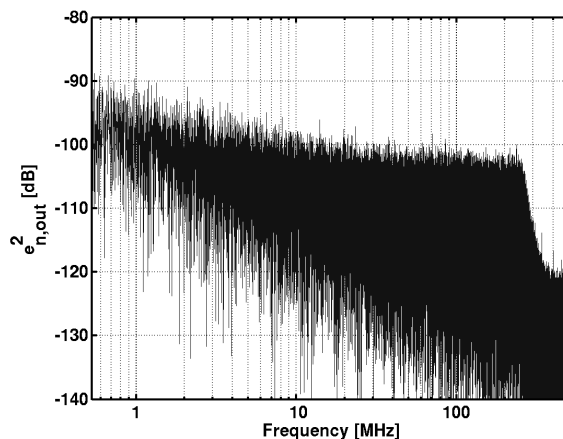


Figure 7.4. Noise of the filter measured at the output of the ADC.

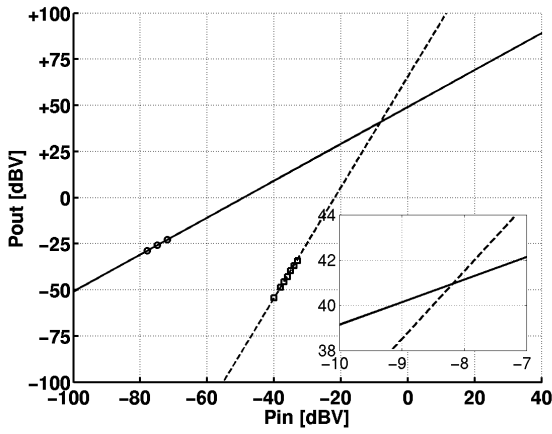


Figure 7.5. Measured out-of-band third-order linearity with the maximum gain.

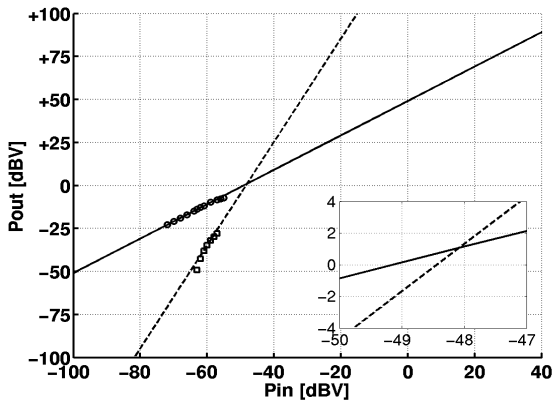


Figure 7.6. Measured in-band third-order linearity with the maximum gain.

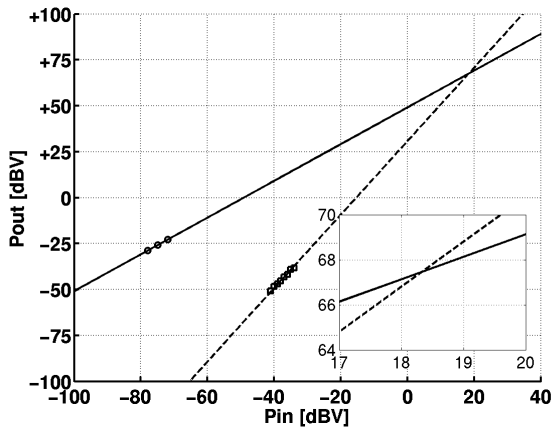


Figure 7.7. Measured out-of-band second-order linearity with the maximum gain.

### 7.3 A WiMedia UWB receiver with a synthesizer

This section describes a single-chip direct-conversion receiver for WiMedia UWB applications. The section is mainly based on [3], except for the experimental results of the low-pass filter, which are based on [2]. The receiver consists of separate BG1 and BG3 LNAs including a 2.4-GHz notch filter, quadrature downconversion mixers followed by gm-C low-pass filters with programmable gain, and a fast-hopping synthesizer. In addition, an ADC was implemented on the same chip as the receiver. However, since it did not function properly, it is omitted from the discussion. The UWB receiver under consideration in this section is intended for a mobile handset and therefore, special emphasis is placed on the reduction of interferers. The maximum gain of the receiver in BG1 mode is 60 dB with a noise figure of less than 6.2 dB. The LO signal generator achieves a settling time of less than 3-ns. The DC current consumption of the receiver is 137 mA from a 1.2-V supply for BG1 operation mode. The chip was fabricated in a standard 65-nm CMOS process.

#### 7.3.1 Receiver

The block diagram of the direct-conversion receiver that was implemented is shown in Fig. 7.8. The receiver consists of a dual-band RF front-end, two programmable-gain 240-MHz low-pass filters, and a fast-hopping synthesizer. In addition to the main signal path, the receiver has test inputs and outputs, as depicted in Fig. 7.8, in order to perform stand-alone measurements for each circuit block. The receiver covers the band groups (BG) 1 and 3, which consist of sub-bands with center frequencies of 3432, 3960, and 4488 MHz and 6600, 7128, and 7656 MHz, respectively. UWB band groups with corresponding sub-bands were presented in Fig. 2.6 in Chapter 2.

With the dual input, the matching and gain responses of both signal paths can be optimized separately and thus, higher interferers can be tolerated. The RF front-end utilizes separate signal paths up to the buffer driving the mixers. A current-steering DAC, similar to that shown in Fig. 6.13, at the input of both baseband filters controls the DC offset injected into the baseband. The synthesizer uses three parallel phase-locked loops (PLL) to generate an LO tone for each sub-band within the corresponding band group. It also includes a multiplexer (MUX) for selecting one of the LO tones for the quadrature generation circuits. The LO quadrature generation circuits utilize a dual signal path where a divide-by-two (DIV2) circuit is used for BG1 and an active two-stage poly-phase filter (APPF), where the resistors are replaced by transconductance elements, is used for BG3. This

quadrature generation scheme enables both band groups, 1 and 3, to be covered with only one VCO in each PLL. Additional buffering circuits are used to amplify and drive the LO signal to the mixers. The low-quality passive components available in the process degrade the performance of a passive poly-phase filter. Therefore, an aggressive design choice was made, to use the APPF. Unfortunately, the APPF did not perform as simulated and thus the measurement results of the BG3 mode are limited to a gain plot.

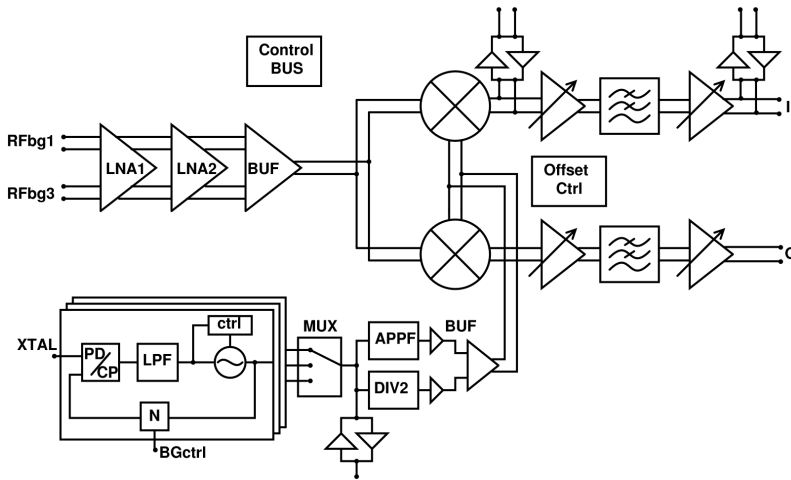


Figure 7.8. Receiver block diagram with test inputs and outputs [3] (© 2008 IEEE).

### 7.3.2 RF front-end

The wide bandwidth of the UWB radio poses challenges in the design of the RF front-end. Despite the pre-select filtering, interfering signals (GSM900, 2.4-GHz WLAN, etc.) can corrupt UWB reception because of intermodulation or desensitization. This situation is relaxed when operating in BG3 because of the less congested spectrum. In this design, the topology chosen for the BG1 LNA1 relies on two feedbacks, one from the load of the first stage and another from the load of the second stage to the input, as shown in Fig. 7.9. The double-feedback arrangement provides sufficient input matching even with additional parasitic capacitance introduced at the LNA input. Moreover, a degeneration inductor is not needed, which saves on die area and enables the dual-input configuration to have a compact layout. A cascode configuration was utilized in the amplifier stages to achieve a higher gain. The differential signal paths are cross-coupled in the LNA to obtain a negative feedback. It should be noted that both amplifier stages invert the signal phase. In the first stage, a shunt-peaked load provides gain peaking, while the feedback enables only one inductor to be



used in this topology. There is also a LC notch filter that is used to attenuate interferers around 2.4 GHz.

Super source-follower buffers after the LNAs are used to drive the mixers. The output signals of the buffers are directly connected to the sources of the double-balanced Gilbert cell mixer switches. Compared to a typical high-impedance input, this low-impedance node suffers less from the parasitic capacitance of the two signal paths, resulting in a near-flat frequency response. A current source and common-mode feedback circuitry is used to bias the switches and set the output DC voltage of the mixer for the following analog baseband filter.

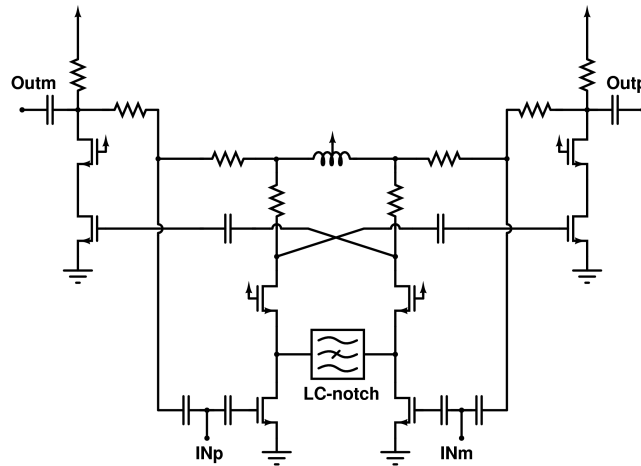


Figure 7.9. Schematic of BG1 LNA1 and LNA2 [3] (© 2008 IEEE).

### 7.3.3 Low-pass filter

The fifth-order 240-MHz continuous-time low-pass filter is similar to the one shown in Fig. 6.1 and described in 7.2. However, in this design, the leapfrog gm-C filter was synthesized for a transconductor DC gain of 26 dB. When the effects of the parasitic Miller capacitors were also taken into account, the design goal for the passband ripple was set to be 1 dB. The accuracy requirement with the 26-dB gain of the transconductors is 1 dB for a 0.25-dB amplitude error at the passband edge. The passive pole was placed at 190 MHz. The filter includes an adjustable gain control from 9 dB to 43 dB in 1-dB gain steps. As a result of the trade-off between a high gain in order to reduce the input-referred noise of the filter and adequate attenuation in the filter stopband in order to increase the out-of-band linearity of the filter, the gain of the first filter stage is 16 dB. Since the last filter stage limits the in-band linearity of the filter, it has no gain. Because of the realizability of the prototype, the gains of the second and third stage

are 10-dB and 12-dB, respectively. The output buffer was designed to have 5 dB of gain, as was the case in the first evolution version described in Section 7.2. In addition to the 65-nm CMOS technology adopted in this design with slightly different transistor characteristics, another difference compared to the first evolution version is that the 5-bit switched-capacitor matrices had to be re-designed using metal-finger capacitors. The metal-insulator-metal capacitors used in the previous design were not available in the 65-nm CMOS process.

### 7.3.4 Experimental results of receiver

The chip was fabricated using a standard 1.2-V 65-nm CMOS process and it was bonded directly onto a PCB. The active area of the receiver is 2.7 mm<sup>2</sup>, which includes the receiver circuit blocks that were described, a control bus, decoupling capacitance, and interconnection wiring. A micrograph of the chip is shown in Fig. 7.10. It is worth mentioning that the chip also incorporates a transmitter that is not of concern here.

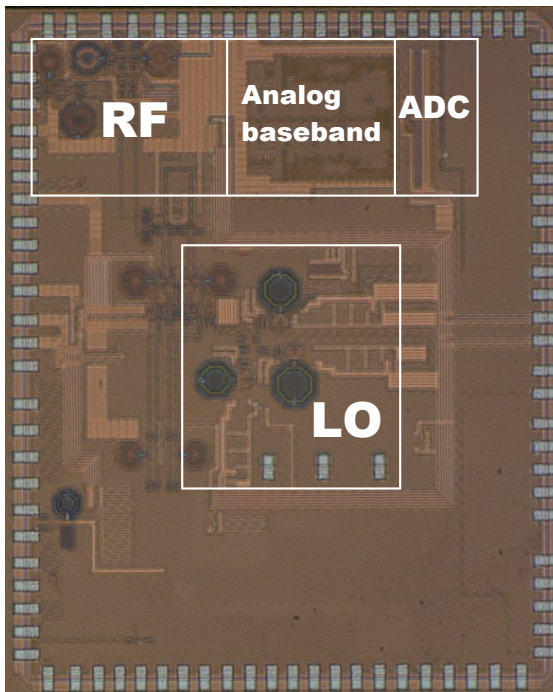


Figure 7.10 Chip micrograph [3] (© 2008 IEEE).

The measured frequency responses of the receiver in BG1 and BG3 mode are presented in Fig. 7.11. The gain was measured from the low-pass filter output and thus the effects of the RF front-end, baseband filter, and LO

generation are all visible in the figure. The gain level of the first sub-band in BG3 is already 10 dB lower than for BG1, which indicates that the LO signal amplitude is not sufficient for the mixers. This was also verified in the reception band, where the operating band of the divider and the APFF overlap. In addition, there is a 15-dB difference in the gain of the three sub-bands, which suggests that the frequency response of the LO path droops heavily. The BG1 gain of the receiver is  $60 \pm 1$  dB. The gain variation is slightly higher than had been expected on the basis of the simulation results. The most probable cause of this is the PCB board and the modeling of the RF input. Matching the BG1 input covers a frequency range from 2.6 to 4.9 GHz with the PCB board. The measured noise figures of the receiver are 6.2, 6.1, and 5.7 dB for sub-bands 1, 2, and 3, respectively. If the noise from the active baseband filter is excluded, the receiver noise figure decreases by 1 dB. This is due to the fact that although the noise of the low-pass filter is as low as targeted, the gain of the RF front-end is lower compared to the design goal. The measured input compression point (ICP) of the receiver is -32.5 dBm (referred to a 100- $\Omega$  source impedance) with a 4-GHz test tone and minimum baseband gain. The in-band IIP2 and IIP3 of the receiver are +15.5 and -19 dBm with maximum gain, respectively. The ICP with a 2.4-GHz blocker is -28 dBm, measured with maximum baseband gain. The measured IIP3 for 880- and 2420-MHz interferers with a 15-dB power level difference is -9 dBm, which is 10 dB better than without the notch filter. The total current consumption of the receiver in BG1 mode is 137 mA.

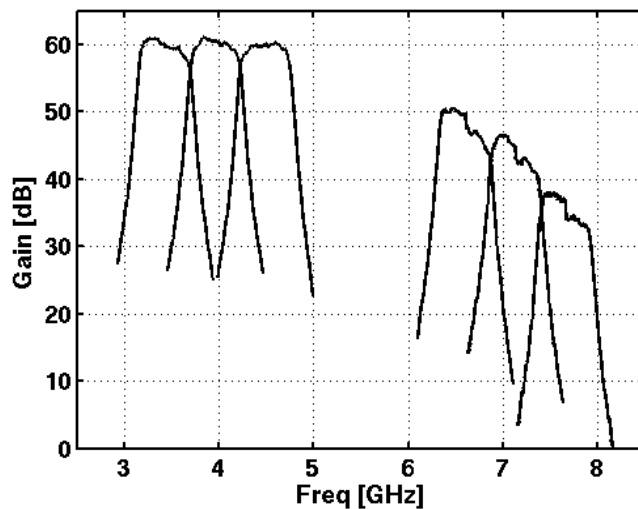


Figure 7.11. BG1 and BG3 gain response [3] (© 2008 IEEE).

The frequency synthesizer was measured to be able to provide the BG1, BG3, and BG6 tones for the LO generator circuitry. The measured settling time between the sub-sequent bands is less than 3 ns with a 3-MHz hopping rate. The measurement results are collected in Table 7.2.

Table 7.2. Measurement results of the receiver [3] (© 2008 IEEE).

		<b>Band Group 1</b>		
<b>RF band</b>		3168-3696 MHz	3696-4224 MHz	4224-4752 MHz
<b>Gain max/min</b>		58.5 / 24.5 dB	59 / 25 dB	59 / 25 dB
<b>NF</b>		6.2 dB	6.1 dB	5.7 dB
<b>S11 &lt; -10dB</b>		2.6...4.9 GHz		
<b>ICP</b>		-32.5 dBm@100Ω		
<b>In-band IIP2</b>		+15.5 dBm@100Ω		
<b>In-band IIP3</b>		-19 dBm@100Ω		
<b>Blocker IIP3*</b>		-9 dBm@100Ω		
<b>Frequency hopping</b>		< 3 ns		
<b>Phase noise</b>	<b>In-band</b>	-86 dBc/Hz		
	<b>Out-of-band</b>	-94 dBc/Hz @ 1 MHz		
<b>Spurious tones</b>		-48 dBc @ 66 MHz		
<b>Supply</b>		1.2 V		
<b>DC current</b>		35 (RF) + 60 (BB) + 42 (LO) = 137 mA		
<b>Technology</b>		65-nm CMOS		
<b>Active area</b>		2.7 mm <sup>2</sup>		

\*Measured with 2420- and 880-MHz test signals at 15-dB power difference.

### 7.3.5 Experimental results of low-pass filter

A micrograph of the filter is shown in Fig. 7.12. The active silicon area of the filter is 0.21 mm<sup>2</sup>. The filter circuit includes a test input with an on-chip NMOS buffer and a test output with an on-chip CMOS switch in order to measure the filter as a stand-alone circuit. The test input of the filter was utilized in all the measurements. The frequency response and noise of the filter were measured directly from the lossy test output. The gain and linearity were measured from the test output with an off-chip instrumentation amplifier that had a balanced high-impedance input and a single-ended output matched to 50 Ω.

The measured and simulated nominal frequency response of the low-pass filter with the maximum gain is shown in Fig. 7.13. The measured frequency response is scaled to 0 dB at 5 MHz. It is a combination of two separate curves measured at different input signal levels to expand the dynamic range of the measurement. The measured passband edge frequency and -3-dB frequency are 240 MHz and 275 MHz, respectively. The measured passband ripple is less than 2 dB and the designed selectivity is achieved at the stopband of the filter. Considering the wide bandwidth, over 200-MHz, the measured and simulated frequency responses of the filter can be said to

compare favorably with each other, as was also the case with the previous 240-MHz filter design. The effect of the parasitic Miller capacitances and the transistor mismatches on the filter frequency response at the passband have already been discussed in Section 7.2.1.

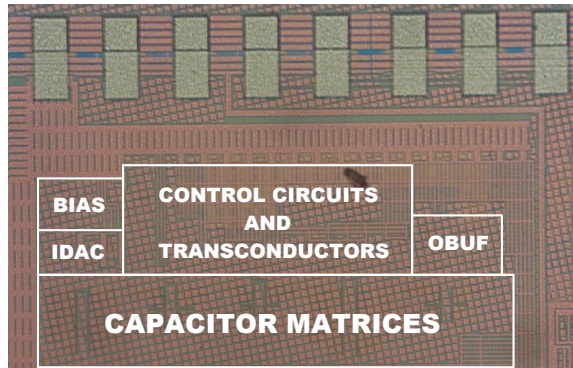


Figure 7.12. Micrograph of the filter [2] (© 2009 IEEE).

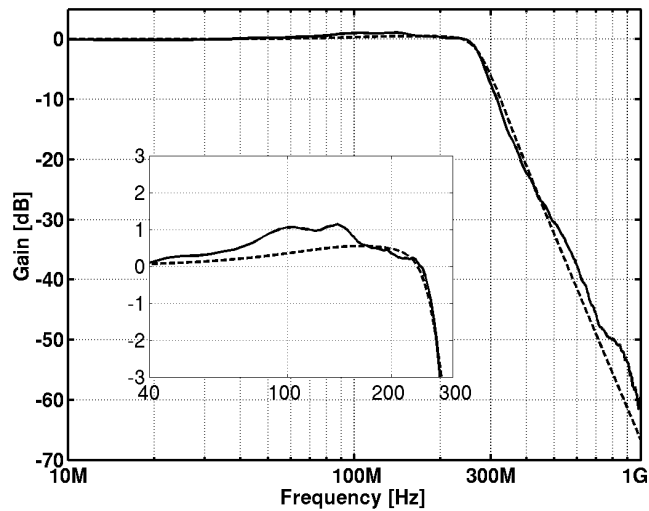


Figure 7.13. Measured (solid line) and simulated (dashed line) frequency response of the filter.

The measured maximum and minimum voltage gains of the filter are 43 dB and 9 dB, respectively, which corresponds to a programmable gain range of 34 dB. The measured integral gain errors of the 6-dB and the 1-dB gain steps of the filter are presented in Fig. 7.14. The error of an individual 6-dB gain step is less than 0.2 dB. Correspondingly, the error of an individual 1-dB gain step is 0.26 dB at the maximum. On the basis of the measurements of the previous filter design, the  $R_{ON}$ -resistance of the CMOS switch at the test output with the finite input impedance (approximately

30 k $\Omega$ ) of the external instrumentation amplifier were known to degrade the resistive 1-dB gain steps. In addition, it was known that a more reliable measurement result would have been obtained from the output of a following ADC, which did not perform properly in this receiver design. However, in the 60-GHz receiver implementation presented in Section 7.4, the 1-dB gain steps of a similar low-pass filter were measured from the output of the following ADC. Those measurement results showed that the error of the individual 1-dB gain steps is approximately 0.2 dB, as was originally measured without an ADC.

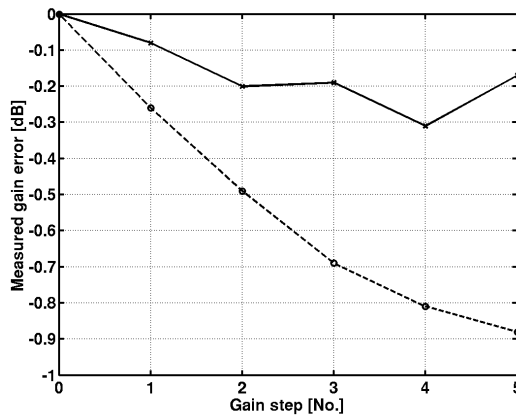


Figure 7.14. Measured integral gain errors of 6-dB (solid line) and 1-dB (dashed line) gain steps [2] (© 2009 IEEE).

The measured frequency responses of the filter with all the 6-dB gain steps and, in addition, with the minimum gain are shown in Fig. 7.15. The 6-dB gain steps were implemented in the first filter transconductor,  $G_{m1}$  in Fig. 6.1, with parallel binary-weighted transconductors, as was described in Section 6.3. In the measurements, it was observed that when the parallel transconductors are disconnected one by one from the leapfrog filter input, the reduction of the total parasitic Miller capacitance associated with the transconductor  $G_{m1}$  directly affects the location of the real pole at the leapfrog filter input. In other words, each time the gain of the filter is altered by connecting or disconnecting unit transconductors in  $G_{m1}$ , the change of the real pole frequency has to be compensated by adjusting the capacitance of capacitor matrix  $C_1$  at the filter input. This undesired effect was shown in the simulations only by adding much more parasitic Miller capacitance between the input and output of each unit transconductor of  $G_{m1}$  than there was expected to be. In fact, even more parasitic Miller capacitance had to be added than was extracted from the layout in order to obtain a similar effect in the simulations.

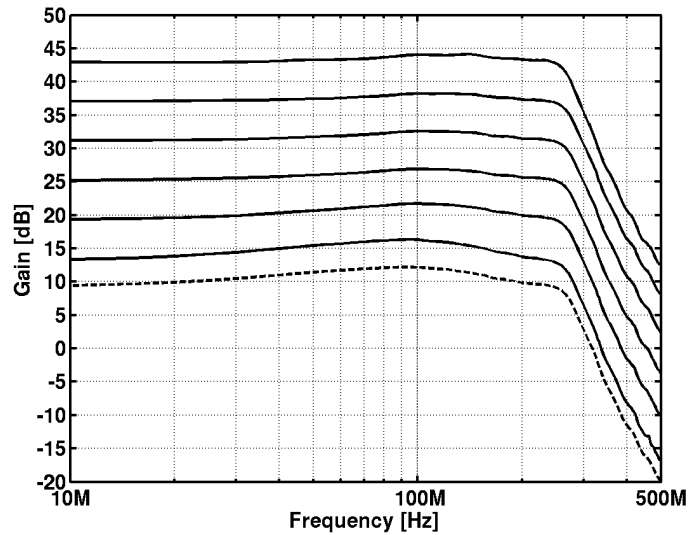


Figure 7.15. Measured frequency responses with all 6-dB gain steps (solid lines) and with the minimum gain (dashed line) [2] (© 2009 IEEE).

Table 7.3. Measured performance of the filter [2] (© 2009 IEEE).

Technology	65-nm CMOS
Supply voltage	1.2 V
Filter order	5
Voltage gain at 5 MHz	9 – 43 dB
Passband edge frequency	240 MHz
-3-dB frequency	275 MHz
Integrated input-referred noise (1 Hz...240 MHz)	121 $\mu\text{V}_{\text{rms}}$
Input-referred noise density	7.8 nV/ $\sqrt{\text{Hz}}$
IIP3 (in-band, $f_1 = 115\text{MHz}$ , $f_2 = 225\text{MHz}$ ) with the maximum and the minimum gain settings	-46 dBV -12.5 dBV
IIP3 (out-of-band, $f_1 = 400\text{ MHz}$ , $f_2 = 795\text{ MHz}$ )	-8 dBV
IIP2 (out-of-band, $f_1 = 400\text{ MHz}$ , $f_2 = 405\text{ MHz}$ )	+15 dBV
Power consumption	36 mW
Die area without pads	0.21 mm <sup>2</sup>

The measured performance results are collected in Table 7.3. The measured integrated input-referred noise from 1 Hz to 240 MHz with the maximum filter gain is 121  $\mu\text{V}_{\text{rms}}$ , which corresponds to an input-referred noise density as low as 7.8-nV/ $\sqrt{\text{Hz}}$ . Several measurements were performed and averaging was used to improve the statistical reliability of the noise voltage measurement.

The linearity measurements are presented next. In each of these, the frequencies of the input test tones were chosen in such a way that one of the corresponding intermodulation products arose at a low 5-MHz frequency.

This was due to the limited bandwidth ( $< 20$  MHz) of the external instrumentation amplifier. The out-of-band IIP<sub>3</sub> was measured with 400-MHz and 795-MHz test signals. As shown in Fig. 7.16, the measured out-of-band IIP<sub>3</sub> of the filter with the maximum gain is  $-8$  dBV. The in-band IIP<sub>3</sub> was measured with 115-MHz and 225-MHz test signals. The measured in-band IIP<sub>3</sub> with the maximum and minimum gain is  $-43$  dBV and  $-12.5$  dBV, respectively, as shown in Figure 7.17. Hence, the in-band spurious-free dynamic range (SFDR) of the filter is 44 dB. The out-of-band IIP<sub>2</sub> was measured with 400-MHz and 405-MHz test signals. As shown in Fig. 7.18, the measured out-of-band IIP<sub>2</sub> of the filter with the maximum gain is  $+15$  dBV. The filter was measured to consume 36 mW.

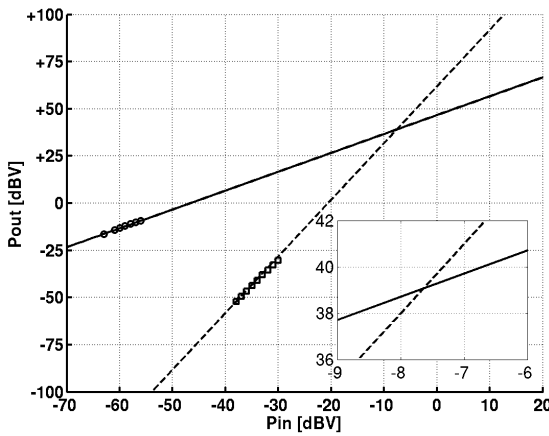


Figure 7.16. Measured out-of-band third-order linearity with the maximum gain [2] (© 2009 IEEE).

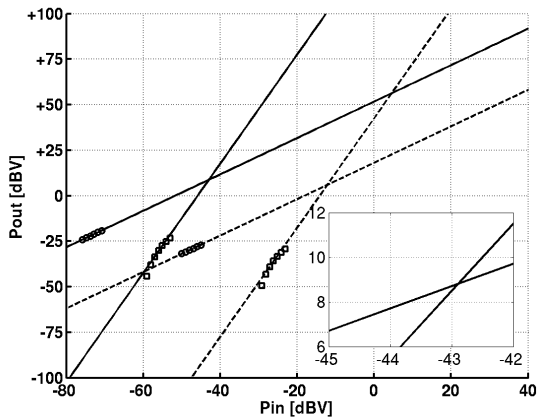


Figure 7.17. Measured in-band third-order linearity with the maximum (solid lines) and with the minimum (dashed lines) gain [2] (© 2009 IEEE).



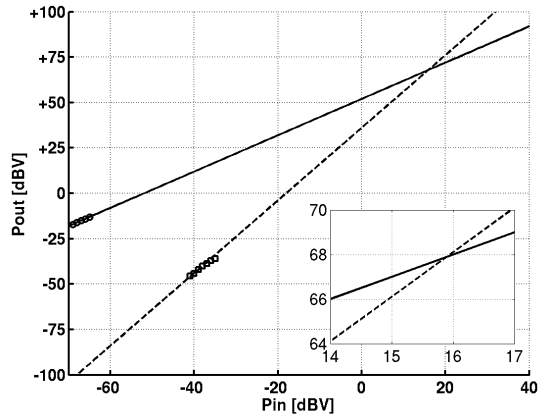


Figure 7.18. Measured out-of-band second-order linearity with the maximum gain [2] (© 2009 IEEE).

## 7.4 60-GHz CMOS receiver with an on-chip ADC

A broadband 60-GHz receiver integrated on a single silicon chip is presented in this section. The circuit consists of a millimeter-wave front-end, including a single-ended low-noise amplifier and a balanced resistive mixer, an IF stage, and an analog baseband circuit with an analog-to-digital converter. The receiver is implemented in a 65-nm baseline CMOS technology. No additional options were employed in the fabrication process and the receiver layout fulfills all the technology-specific design rules required. The millimeter-wave front-end and IF-stage circuits are designed to achieve high performance and wideband operation for 60-GHz reception. A 275-MHz analog baseband filter partially merged with a programmable gain amplifier (PGA) ensures an optimal input signal level for the ADC and supports wireless MB-OFDM UWB system data reception. The receiver achieves a measured 7.0-dB noise figure at 60 GHz and the voltage gain can be controlled from 45 dB to 79 dB. The measured  $-1$ -dB input compression point is  $-38.5$  dBm. This section is mainly based on [4], except for the ultra-wideband filter design, at the end of the section, which has not been published previously.

### 7.4.1 Receiver

The block diagram of the single-chip 60-GHz receiver is shown in Fig. 7.19. The dual-conversion architecture was chosen to minimize the number of blocks operating at millimeter-wave frequencies. The 60-GHz front-end consists of a single-ended LNA and a balanced resistive mixer, which downconverts the signal to a 4-GHz intermediate frequency (IF). A

differential two-stage cascode amplifier follows the resistive mixer before the separation of the IF signal into the I/Q baseband signals with a quadrature mixer. The balanced quadrature signals for the mixer are generated on-chip with an active poly-phase filter in which the resistors are replaced with transconductors. The analog baseband circuit contains a 275-MHz low-pass filter and a programmable gain amplifier partially merged together and is followed by a 6-bit 600-MS/s flash-ADC. In this test chip, both local oscillator (LO) signals are external and one complete baseband chain with an ADC is integrated on a single silicon chip. The other baseband channel (Q branch) incorporates a third-order low-pass filter designed to have a 1-GHz  $-3$ -dB frequency and a four-stage limiting amplifier chain similar to the one reported in [11].

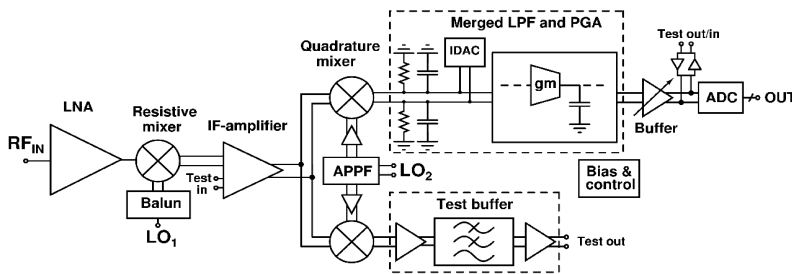


Figure 7.19. Receiver block diagram [4] (© 2009 IEEE).

#### 7.4.2 Millimeter-wave front-end

To minimize the noise contribution of the resistive mixer and the following receiver stages, the LNA uses four common-source stages. Although the weak reverse isolation of the common-source topology that was selected makes the design challenging, a low noise figure and sufficiently high gain can be achieved at millimeter-wave frequencies with this topology. For accurate simulations in the millimeter-wave front-end design, both active and passive components were characterized using test structures from the previous process run [12]. It is also worth emphasizing that the metal density requirements of the 65-nm CMOS technology that was adopted were taken into account. The design of the mixer is presented in detail in [12]. The balanced resistive mixer configuration establishes a broadband conversion from the single-ended 60-GHz input to the differential IF.

#### 7.4.3 IF stage and low-pass filter

A two-stage amplifier with a cascode configuration is utilized in the IF stage to reduce the noise contribution of the remaining receiver chain. The first amplifier stage has a shunt-peaked load to guarantee a broadband

response. An enhanced source-follower output buffer is designed to drive the following quadrature mixer, which is a double-balanced Gilbert cell mixer. A common-mode feedback circuit at the mixer output biases the mixing transistors and sets the DC input voltage for the baseband filter. The fifth-order analog baseband low-pass filter is similar to the one presented in Section 7.3 and shown in Fig. 6.1, including the current-steering DAC at the filter input and a buffer at the filter output.

#### 7.4.4 Experimental results of receiver

The receiver was fabricated in a 65-nm baseline CMOS technology and the chips were directly bonded onto a PCB, excluding the millimeter-wave inputs. A micrograph of the receiver is shown in Fig. 7.20. The total silicon area, including the bonding pads, is 2.8 mm<sup>2</sup>. The receiver measurements were performed from the output of the ADC, with the exception of the –1-dB input compression point (ICP), which was measured from the analog test output. The millimeter-wave signals were fed to the chip via RF probes. The performance of the whole receiver was characterized with a combination of a fixed LO<sub>2</sub> frequency of 4 GHz, baseband frequencies of both 10 MHz and 100 MHz, and an ADC sampling rate of 600 MS/s. The measured noise and gain performance of the receiver, with LO<sub>1</sub> between 59 to 64 GHz and with the maximum baseband gain setting, are shown in Fig. 7.21. The measurement setup limited the RF input to 60 GHz. The NF, which is dominated by the LNA, is 7.0 dB at 60 GHz and 7.9 dB at 55 GHz, showing a relatively flat NF over the measured frequency range. The maximum gain of the receiver chain is 79 dB at 60 GHz and it remains flat within 2 dB over the measured band. As shown in Fig. 7.22, there is a good agreement between the measured and simulated input matching S<sub>11</sub> of the receiver. Input matching is observed to be below –12 dB from 55 to 62 GHz. The measured ICP of the receiver is –38.5 dBm with the minimum receiver gain of 45 dB. Fig. 7.23 shows the output spectrum of the ADC at 600 MS/s with a 10-MHz baseband signal. The overall power consumption of the receiver with one baseband channel is 198 mW from a 1.2-V supply. Table 7.4 summarizes the experimental results of the whole receiver.

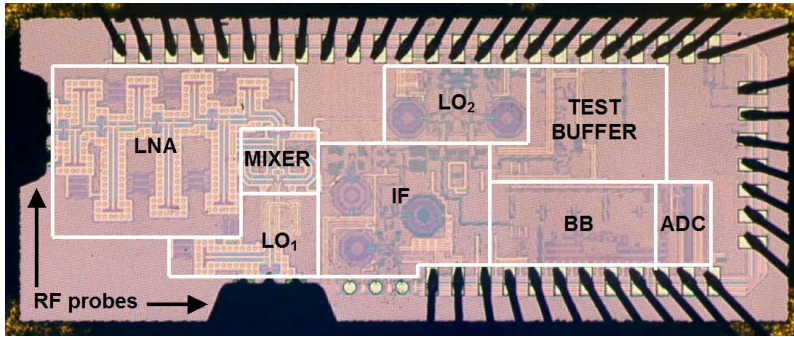


Figure 7.20 Micrograph of the receiver [4] (© 2009 IEEE).

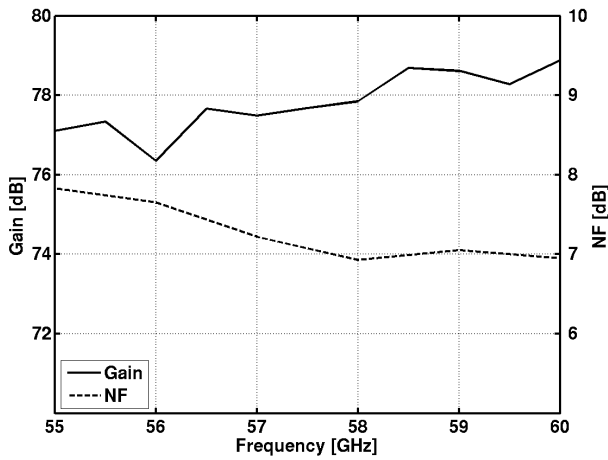


Figure 7.21 Measured voltage gain and noise figure of the receiver [4] (© 2009 IEEE).

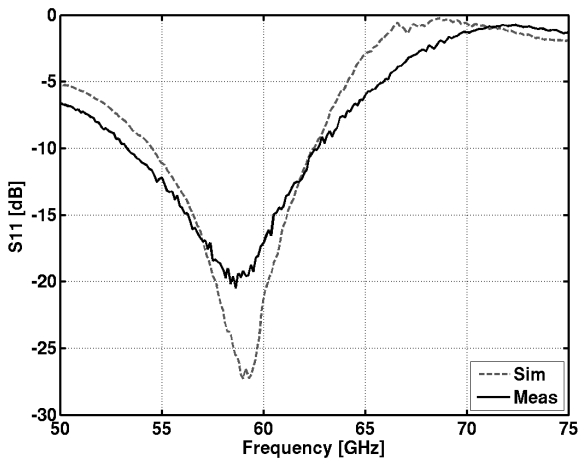


Figure 7.22 Measured and simulated  $S_{11}$  of the receiver [4] (© 2009 IEEE).

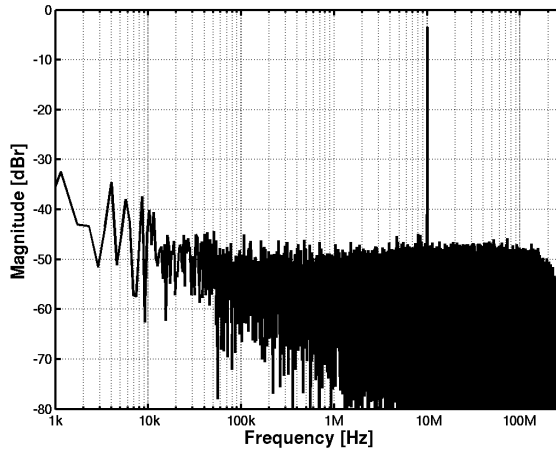


Figure 7.23 Spectrum of the whole receiver measured from the output of the 600-MS/s ADC with a 10-MHz signal at the baseband [4] (© 2009 IEEE).

Table 7.4. Measured performance of the 60-GHz CMOS receiver [4] (© 2009 IEEE).

Technology	65-nm CMOS
Supply voltage	1.2 V
Range of operation*	55 to 60 GHz
NF**	7.0 dB
Voltage gain**	79 to 45 dB
Gain control step	1 dB
ICP** with min gain	-38.5 dBm
S11***	< -12 dB
BB -3dB frequency	275 MHz
ADC sampling rate	600 MS/s
ADC ENOB	> 4.0 bits
ADC SFDR	> 30 dB
Power dissipation	198 mW
Chip area	2.8 mm <sup>2</sup>

\* Limited to 60 GHz by the measurement setup

\*\*RF/IF at 60/4GHz

\*\*\*Over the entire range of operation

#### 7.4.5 Ultra-wideband low-pass filter

This sub-section describes the circuit design of the third experimental gm-C filter circuit of this work. The design goal for the -3-dB bandwidth of the filter was set to be as large as 1 GHz, a bandwidth approximately four times wider compared to the two previous gm-C filter designs. Partially for that reason, the filter order was selected to be three instead of the five used in the previous two gm-C filter designs. Moreover, a third-order continuous-

time filter at the baseband of a dual-conversion radio receiver can be considered to be a feasible choice in 60-GHz applications owing to the much less congested spectrum compared to, for example, the one allocated for the use of UWB devices below 10 GHz. In the design phase of the receiver, the overall voltage gain of the receiver front-end preceding the analog baseband filter (i.e. the millimeter-wave front-end and IF stage together) was estimated to be around 38 dB. The design goal for the NF of the whole receiver was set to be 7–8 dB on the basis of the measured performance of a previous 60-GHz stand-alone LNA reported in [12], corresponding to an input-referred noise density of approximately  $50\text{-}\mu\text{V}/\sqrt{\text{Hz}}$ . To amplify a signal as low as  $50\text{-}\mu\text{V}$  at the receiver input to a rail-to-rail signal at the limiting amplifier output, the analog baseband circuit, consisting of a low-pass filter and a limiter, was required to have approximately 50 dB of voltage gain when the total voltage gain of the millimeter-wave and IF stage was expected to be the aforementioned 38 dB. Because it is challenging to design both a low-pass filter and limiting amplifier which have a high gain and a wide bandwidth simultaneously, the gm-C biquad was intended to have approximately 20 dB of the voltage gain and the remaining 30 dB of the gain was left for the limiter. It was decided to embed the gain of the filter into the biquad in order to avoid the challenging task of designing and implementing an auxiliary current-consuming wideband amplifier stage.

#### *7.4.5.1 Implemented third-order low-pass filter*

The schematic of the third-order low-pass filter circuit that was implemented is shown in Fig. 7.24. As was the case in the two previous gm-C filter implementations, the real pole was extracted from the third-order filter transfer function and realized at the filter input with the passive load components of the preceding downconversion mixer. A current-steering DAC, similar to the one shown in Fig. 6.13, and an output buffer, similar to that in Fig. 6.9, were employed to compensate for the DC offset and to drive the parasitic input capacitance of the following limiting amplifier chain, respectively. To reduce the parasitic capacitance associated with the switchable n-well resistors forming the load of the output buffer and, hence, to maximize the bandwidth of the buffer, the resistors  $R_{21}\text{--}R_{24}$  shown in Fig. 6.10 were removed. The elimination of the resistors corresponds to removing four gain settings from the buffer. With this design, it is feasible to drive the following limiting amplifier chain without a programmable gain. The bandwidth of the modified version of the output buffer with a 0-dB gain setting was simulated to be 3.8 GHz. The frequency response of the 1-GHz filter was predistorted to compensate for the small

amplitude error (i.e. drooping) at frequencies close to the filter passband edge as a result of the finite bandwidth of the following output buffer.

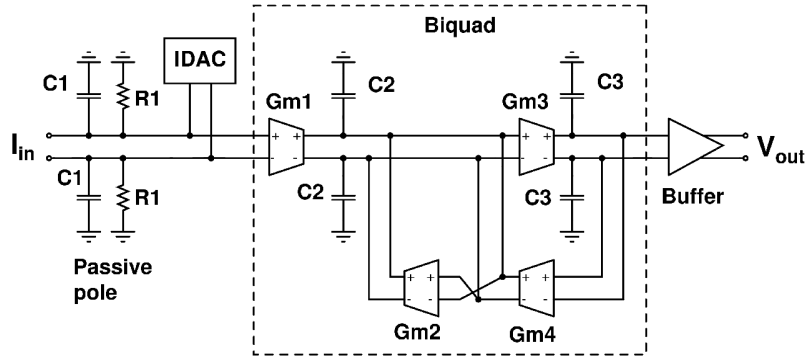


Figure 7.24. Third-order gm-C low-pass filter.

#### 7.4.5.2 Filter prototype design

In a gm-C filter as wide as 1-GHz, the filter coefficients ( $C_1$ ,  $C_2$ , and  $C_3$ ) become small compared to the total amount of the parasitic capacitance in the filter nodes. For an accurate filter frequency response, the ratios between the parasitic capacitances and the filter coefficients ( $C_2$  and  $C_3$ ) have to be in balance at each filter node. Thus, for a practical filter implementation, a prototype initially resulting in balanced ratios at each filter node is worth selecting. The total parasitic capacitance,  $C_{para,input,total}$ , at the filter input (i.e. at the IF-baseband interface) consists of the parasitic output capacitance of the mixer and current-steering DAC, the parasitic input capacitance of the first transconductor  $G_{m1}$ , and a parasitic wiring capacitance.

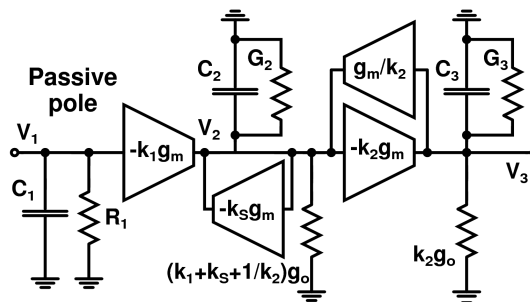


Figure 7.25. Equivalent single-ended gm-C filter with gain scaling factors  $k_i$ .

Fig. 7.25 shows an equivalent single-ended version of the third-order gm-C filter with gain scaling factors  $k_i$ . It is worth emphasizing that the circuit shown in Fig. 7.25 corresponds to the one shown in Fig. 4.4. The circuit shown in Fig. 4.4 was under consideration when filter synthesis with

lossy gm-C integrators was presented in Chapter 4. The same filter design approach was used in this design for the third time, in this case for a filter with a much wider bandwidth. As shown in Table 7.5, several different combinations of the filter prototype, the gain partitioning in the filter, and the DC gain of the transconductors were studied. As a baseline for the study, the transconductance of the unit transconductor (with  $k_i = 1$ ) was assumed to be  $860 \mu\text{S}$  on the basis of the two previous gm-C filter designs. The design goals were as follows:

- 1) total gain of the filter:  $k_1 \cdot k_2 \geq 8$ ;
- 2)  $C_1 \geq C_{para,input,total}$  (passive pole realizability condition);
- 3)  $k_1 \leq 4$  in order meet design goal 2);
- 4)  $C_2$  has to be high because there will be a large amount of parasitic capacitance at the corresponding biquad node, which is due to the fact that all four transconductors are connected to that node;
- 5) the ratios between the parasitic capacitances and the filter coefficients,  $C_2$  and  $C_3$ , have to be in balance.

Table 7.5. Filter prototype and gain partitioning selection.

Prototype	Order	Passband ripple	ks	k1	k2	Adc	C1	Passive pole frequency	C2	C3
Chebyshev	3	0.5 dB	1	1	1	26 dB	508 fF	626 MHz	313 fF	55 fF
Chebyshev	3	0.1 dB	1	1	2	26 dB	328 fF	969 MHz	209 fF	59 fF
Chebyshev	3	0.1 dB	1	8	2	26 dB	328 fF	969 MHz	328 fF	38 fF
Chebyshev	3	0.5 dB	1	4	2	26 dB	508 fF	626 MHz	370 fF	47 fF
Chebyshev	3	0.005 dB	1	4	1	26 dB	175 fF	1.8 GHz	106 fF	46 fF
Butterworth	3	-	1	4	1	26 dB	318 fF	1 GHz	190 fF	104 fF
Butterworth	3	-	1	8	1	26 dB	318 fF	1 GHz	222 fF	90 fF
Butterworth	3	-	1	8	1	36 dB	318 fF	1 GHz	161 fF	118 fF
Butterworth	3	-	0.5	8	1	26 dB	318 fF	1 GHz	140 fF	140 fF
Butterworth	3	-	1	4	2	26 dB	318 fF	1 GHz	201 fF	105 fF
<b>Butterworth</b>	<b>3</b>	<b>-</b>	<b>1</b>	<b>4</b>	<b>2</b>	<b>22 dB</b>	<b>318 fF</b>	<b>1 GHz</b>	<b>261 fF</b>	<b>88 fF</b>
Butterworth	3	-	1	3	3	22 dB	318 fF	1 GHz	314 fF	158 fF

It should be pointed out that, in Table 7.5,  $C_2$  and  $C_3$  represent the filter coefficient values which have been predistorted according to the losses caused by the low DC gain of the transconductors and the voltage gain embedded into the filter. The row written in bold in Table 7.5 shows the combination that was selected. With this selection, the ratios between the parasitic capacitances and filter coefficients,  $C_2$  and  $C_3$ , in the biquad are in balance when the second biquad stage (i.e. the transconductor  $Gm_3$  and capacitor  $C_3$ ) is scaled by a factor of two. In addition, the realizability condition of the passive pole can be met by minimizing the parasitic wiring capacitance at the filter input node with a careful layout design and by reducing the parasitic input capacitance of the first transconductor compared to the previous designs of this work. The latter is discussed in the next paragraph. It should be noted that the load resistor of the mixer,  $R_1$  in Fig. 7.24 and 7.25, is designed to have a nominal resistance value of  $500 \Omega$



and, therefore, the capacitance value of  $C_1$  is critical in this design. During the design phase, the filter coefficients were tuned according to the simulations in order to compensate for the undesired effects of the parasitic Miller capacitances of the transconductors at the passband of the filter.

#### 7.4.5.3 Filter transconductors

On the basis of the investigation shown in Table 7.5 and the decision made, all the transconductors in the filter were designed to have a nominal 22-dB DC gain. The transconductor structure that was adopted is similar to the one used in the two previous gm-C filter designs and presented in Chapter 6. However, the channel length of the transistors was reduced from  $0.25\ \mu\text{m}$  to  $0.18\ \mu\text{m}$  in this design to reduce the parasitic capacitances of the transconductors and increase the bandwidth of the common-mode feedforward and feedback circuits. In the previous gm-C filter designs, the transistors M1 and M3 and, correspondingly, the transistors M7 and M9 in the transconductors, shown in Fig. 6.2, were designed to have an equal number of fingers. In the first filter transconductor of this ultra-wideband design, Gm1, the number of fingers of the CMFF transistors M3 and M9 was reduced by a factor of  $1/4$  in order to considerably reduce the parasitic input capacitance of the transconductors. Owing to small filter coefficient values compared to the amount of parasitic capacitance at the filter nodes, capacitor matrices could not be implemented in this design. Instead, the transconductance of the transconductors was designed to be adjustable, as was described in Section 6.4.2.

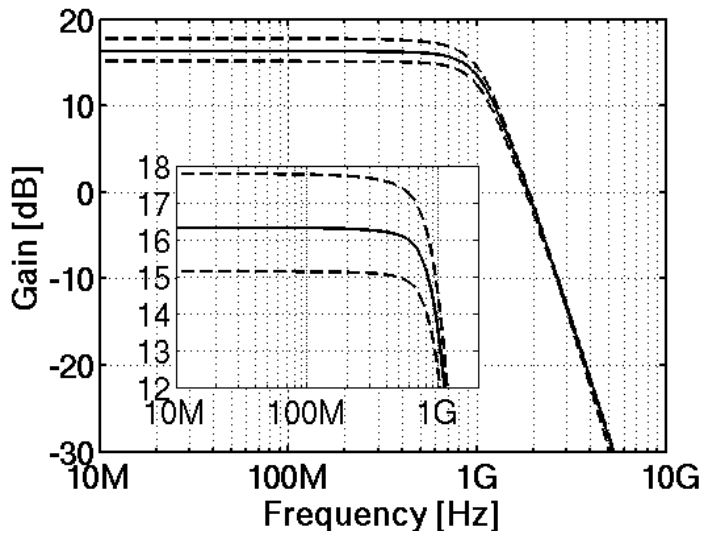


Figure 7.26. Simulated filter frequency responses in the nominal case (solid line) and in the two worst cases, i.e.  $\pm 3\sigma$  corners combined with  $-30^\circ/+100^\circ$  temperatures (dashed lines).

#### 7.4.5.4 Simulation and experimental results of the filter

Fig. 7.26 shows the simulated filter frequency responses in the nominal case and in the two worst-case corners. The filter  $-3$ -dB frequency is tuned to 1 GHz by means of the transconductance control in both worst-case corners.

To measure the filter frequency response, a test signal was injected into the filter through the test input of the preceding IF stage, shown in Fig. 7.19. The frequency response of the IF stage and the filter shown in Fig. 7.27 was then measured from a test output between the output of the buffer amplifier and the input of the following limiting amplifier chain. As can be seen in Fig. 7.27, the filter frequency response has deteriorated.

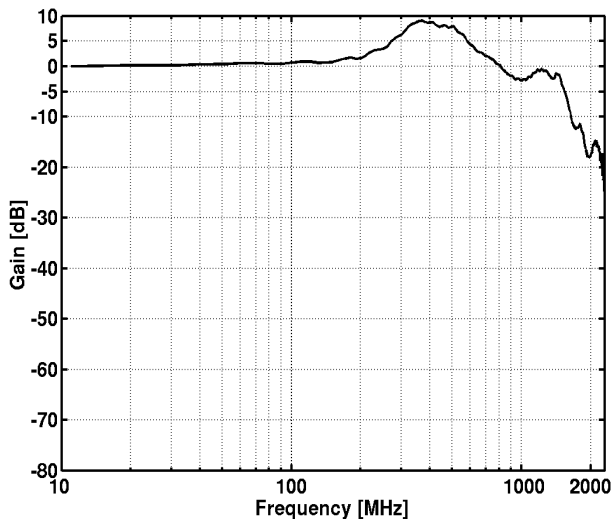


Figure 7.27. Measured frequency response of the IF stage and the 1-GHz filter.

## 7.5 Summary and comparison to other published filters

The three continuous-time gm-C filter implementations of this work were presented in this chapter, together with the experimental results. Two of them are fifth-order 240-MHz filters that were designed and implemented for two evolution versions of single-chip WiMedia UWB receivers in standard 0.13- $\mu$ m and 65-nm CMOS technologies, respectively. Both filters were partially merged with a PGA, resulting in a programmable gain range of over 30 dB with accurate 6-dB gain steps. In addition, in both filter circuits, a separate output buffer designed to drive a following ADC was measured to be capable of adjusting the voltage gain of the circuit with five 1-dB gain steps with an accuracy better than 0.3 dB. The filter synthesis

approach that was presented in Chapter 4 was utilized in both designs. As an advantage of the approach that was used, a voltage gain of almost 40 dB was implemented in the filters, although the Q-factors of the filter integrators are degraded.

The measured frequency responses of the 240-MHz filters were shown to compare favorably with simulations. In addition to a high out-of-band selectivity, the 240-MHz gm-C filters were measured to have a low ( $\leq 7.8\text{-nV}/\sqrt{\text{Hz}}$ ) input-referred noise density. The high measured  $-8\text{-dBV}$  out-of-band IIP<sub>3</sub> is achieved by implementing a passive pole at the filter input. Despite the pseudo-differential structure that was used, the measured out-of-band IIP<sub>2</sub> of  $+15\text{-}18\text{-dBV}$  is tolerable. Assuming a 30-dB voltage gain for the RF front-end, the performance of the filters demonstrated here leads to negligible deterioration of the dynamic range of the receiver despite the high level of functionality and selectivity.

The measured performance of the 240-MHz low-pass filter implementations is compared to recently published low-pass filters that have a bandwidth of approximately 200-MHz in Table 7.6. Depending on the application being targeted in each filter implementation, the parameters that are measured are different. Thus, the direct comparison of the filters is not straightforward. There are wideband continuous-time filter implementations published in the literature in which gm-C [13]-[28] or other filter techniques [29]-[37] are utilized. However, to the best of the author's knowledge, only a few published single-chip UWB receivers and transceivers [13]-[15], [29], [30] have an analog baseband circuit which simultaneously achieves a selectivity, out-of-band linearity, and programmable gain range comparable with the 240-MHz filters designed and implemented in this work. The circuits in [14], [15], and [29] have been fabricated in a BiCMOS technology with a supply of over 2 V. The other two are CMOS implementations. In [30], the gain control of the receiver is, at least partially, based on the adjustable gain of the LNA and the supply voltage that is used is 1.5 times higher compared to the filter implementations of this work. In [13], the baseband circuit, which consists of two cascaded third-order filters and three variable gain amplifiers (VGAs), is a more complex structure, with an equal selectivity when compared to the 240-MHz filters presented in this thesis. The stand-alone filters published in [16]-[25], [28], [32]-[34], and [36] use a supply voltage higher than 1.2 V and they were not fabricated in a technology as modern as the 65-nm CMOS one; together, these factors enable transistors with a better analog performance, more complex control circuits, and cascode transistors to be utilized. Furthermore, they and the filter in [35] have no gain or, at least, the gain control range and the number of gain steps are

limited, which significantly simplifies the filter design. The analog baseband chain reported in one of the most recent publications, [27], is implemented according to similar design goals compared to the 240-MHz filter implementations of this work. It is worth pointing out that in [27], the voltage gain of the circuit is implemented with additional PGAs instead of the sixth-order gm-C filter. Another publication among the most recent ones, [37], reports an implementation where a programmable gain amplifier is merged with a sixth-order 240-MHz Bessel low-pass filter. As a result, the circuit has an adjustable gain control from 0 dB to 40 dB in 5-dB gain steps but the selectivity is not comparable with the 240-MHz filter implementations of this work.

The measured performance of the 240-MHz filter implementations of this work show that wideband selective gm-C filters can be realized in modern ultra-deep-submicron CMOS technologies by using pseudo-differential transconductors with a nominal DC gain as low as 24–26 dB. At the same time, the two successful low-voltage wideband filter implementations demonstrate the usability of the filter design approach presented in Chapter 4. However, the third gm-C filter implementation shows that the influence of the undesired second-order effects on the filter frequency response, including the parasitic Miller capacitances between the input and output of the single-stage transconductors and unavoidable mismatches between the transistors, increase considerably as a function of frequency. Thus, when very wide bandwidths are being targeted, the increased influence of second-order effects, together with the smaller values of the filter coefficients, which are mainly realized with parasitic capacitances in the filter nodes, result in inaccurate unpredictable filter frequency responses.

As a next design phase, beyond the scope of this thesis, it would be interesting to investigate how much the accuracy of the frequency response of a gm-C filter is affected if the integrator time constants and the finite DC gain of the transconductors were automatically controlled by means of on-chip tuning circuitry.

In addition to the three gm-C filter implementations, two single-chip RF receiver implementations were presented in Sections 7.3 and 7.4, respectively. The former is a WiMedia UWB direct-conversion receiver and the latter a 60-GHz dual-conversion receiver. The WiMedia UWB receiver was described with an active baseband filter and a synthesizer. The receiver operates in BG1 mode with a 60-dB maximum gain and an NF better than 6.2 dB. The settling time of the on-chip synthesizer is less than 3 ns with in-band phase noise of -86 dBc/Hz. The current consumption is 137 mA from a 1.2-V supply. The receiver design presented here cannot easily be compared to other UWB implementations because of their different target

applications and the extent of their realizations. However, comparing this design to recent implementations reported in [38] and [39], it is observed that the performance metrics given by BG1 are comparable to existing ones. The broadband 60-GHz receiver with an analog baseband circuit and an ADC was designed and implemented in a 65-nm baseline CMOS technology. As a result of the accurate modeling of the millimeter-wave circuit blocks and careful system-level design, a wide operating bandwidth and an NF as low as 7 dB were achieved. The dynamic range of the receiver was considerably increased by embedding an active baseband low-pass filter with a 34-dB programmable gain range into the receiver. The experimental results demonstrate the feasibility of a broadband single-chip 60-GHz receiver with an ADC in a nanoscale CMOS technology. Despite the high level of integration, the receiver compares favorably to existing state-of-the-art millimeter-wave front-ends, as can be seen in Table 7.7.

Table 7.6. Comparison of wideband filter implementations.

Ref.	Year	CMOS technology	Topology	Proto/Order	$f_{-3dB}$ [MHz]	Gain [dB]	Noise (1) [nV/√Hz]	IIP3 (2) [dBV]	THD (2) [dB]	V <sub>DD</sub> [V]	P <sub>D</sub> [mW]	Area (3) [mm <sup>2</sup> ]
[16]	2000	0.25- $\mu$ m	gm-C	Bu / 4	60-350	$\approx$ 0	13.7 (4)	-2 (27)	< -40 (5)	3.3	70	0.15
[17]	2002	0.25- $\mu$ m	gm-C	Eq / 7	200	$\approx$ 0 (6)	na	na	-43 (7)	3.0	210	na
[18]	2003	0.35- $\mu$ m	gm-C	Li / 7	200	$\approx$ 0	na (8)	na	< -44 (9)	+/-1.5	60 (10)	0.18
[34]	2003	0.18- $\mu$ m	op-RC	El / 5	500	$\approx$ 0	18	+13.5	-40 (11)	1.8 (12)	90	na
[19]	2003	0.35- $\mu$ m	gm-C	Eq / 4	80-200	$\approx$ 0	138 (13)	+14 (27)	< -44 (14)	2.3	72	na
[20]	2006	0.35- $\mu$ m	gm-C	Li / 4	550	$\approx$ 0	6.3 (15)	0 (27)	-40 (16)	+/-1.65	140	1.1
[21]	2006	0.12- $\mu$ m	gm-C	na / 3	235	-5-0.5	na	na	-43 (17)	1.5	14.3	0.345
[23]	2006	0.35- $\mu$ m	gm-C	Ch / 5	70-500	$\approx$ 0	16.4 (18)	0 (27)	< -40 (19)	3.3	100	0.65
[1]	2007	0.13- $\mu$ m	gm-C	Ch / 5	265	13-48	7.7	-48 (20)	na	1.2	24	0.34
[35]	2008	0.13- $\mu$ m	s-f-b	na / 6	280	$\approx$ 0	na	na	na	1.2	0.12	0.018
[25]	2009	0.18- $\mu$ m	gm-C	El / 3	50-300	$\approx$ 0	5	+3.9	na	1.8	72	0.9
[36]	2009	0.18- $\mu$ m	op-RC	Ch / 5	44-300	0	49.7 (21)	+2.5 (22)	< -40 (23)	1.8	54	0.63
[2]	2009	65-nm	gm-C	Ch / 5	275	9-43	7.8	-46 (20)	na	1.2	36	0.21
[37]	2009	90-nm	P&F	Be / 6	240	0-40	4.6	-48 (20)	-30 (24)	1.2	3.48	0.062
[26]	2010	0.13- $\mu$ m	gm-C	na / 2	200	$\approx$ 0	35.4	+1.0	< -40 (25)	1.2	20.8	0.5
[27]	2010	0.13- $\mu$ m	gm-C	Ch / 6	250	-9-73	1.42	-71 (20)	na	1.2	56.4	0.8
[28]	2010	0.13- $\mu$ m	gm-C	Ch / 5	70-280	0	14 (26)	+7	na	1.5	21	0.12

Ref.	Year	Proto	V <sub>DD</sub> [V]	SFDR (28) [dB]	FoM1 (29) [pJ]	FoM2 (30) [fJ]	FoM3 (31) [fJ] / ranking	FoM4 (32) [fJ mm <sup>2</sup> ] / ranking
[16]	2000	Bu	3.3	46	50	1.3	1.3 / 9	0.19 / 4
[17]	2002	Eq	3.0	na	150	na	na	na
[18]	2003	Li	+/-1.5	na	43	na	na	na
[34]	2003	El	1.8 (19)	57	36	0.07	0.07 / 1	na
[19]	2003	Eq	2.3	46 (33)	120	3.0	3.0	na
[20]	2006	Li	+/-1.65	51	64	0.51	0.51 / 6	0.56
[21]	2006	na	1.5	na	20	na	na	na
[23]	2006	Ch	3.3	46	40	1.0	1.0 / 8	0.65
[1]	2007	Ch	1.2	20	18	181	0.72 / 7	0.25 / 6
[35]	2008	na	1.2	na	0.07	na	na	na
[25]	2009	El	1.8	57	80	0.16	0.16 / 4	0.14 / 3
[36]	2009	Ch	1.8	48 (22)	245	3.9	3.9	2.5
[2]	2009	Ch	1.2	21	26	208	1.5 / 10	0.31 / 7
[37]	2009	Be	1.2	23	2.4	12	0.12 / 3	0.01 / 1
[26]	2010	na	1.2	45	52	1.6	1.6	0.82
[27]	2010	Ch	1.2	15	38	1189	0.27 / 5	0.21 / 5
[28]	2010	Ch	1.5	53	15	0.08	0.08 / 2	0.01 / 1

op-RC = opamp-RC, P&F = PGA&Filter block (three cascaded PGAs), s-f-b = source-follower-based, Be = Bessel, Bu = Butterworth, Ch = Chebyshev, El = Elliptic, Eq = Equiripple, Li = Linear phase

- (1) Input-referred noise density in the case of the max. bandwidth
- (2) In-band linearity in the case of the max. bandwidth. It should be noted that the in-band IIP3 of a low-pass filter depends on the test tone frequencies selected.
- (3) active chip area
- (4) calculated from the reported  $257\text{-}\mu\text{V}_{\text{rms}}$  integrated output noise value
- (5) for a  $380\text{-mV}_{\text{pp}}$  input signal
- (6) boost at the passband edge
- (7) for a  $800\text{-mV}_{\text{pp}}$  differential input signal at 66 MHz
- (8) integrated output noise level is reported to be around  $-85\text{ dBm}$  but the input-referred noise density cannot be reliably calculated because of the uncertainty about the passband gain of the filter
- (9) for a  $500\text{-mV}_{\text{pp}}$  input signal
- (10) including an automatic tuning system
- (11) for a  $1.73\text{-V}_{\text{pp}}$  differential input signal
- (12) also  $3.3\text{ V}$  for the gate of the  $3.3\text{-V}$  devices used
- (13) calculated from the  $1.69\text{-mV}_{\text{rms}}$  noise level reported for the filter bandwidth of  $150\text{-MHz}$
- (14) for a  $2\text{-V}_{\text{pp}}$  differential input signal at 20 MHz
- (15) calculated from the reported  $-151\text{-dBm/Hz}$  output noise density
- (16) *THD* is approximated with *HD3*. Since in the publication  $HD3 \approx 49\text{ dB}$  is reported for a  $-7\text{ dBm}$  input signal, the input signal level for the  $HD3 \approx 40\text{ dB}$  is estimated to be around  $-2.5\text{ dBm}$  ( $470\text{ mV}_{\text{pp}}$ ).
- (17) for a  $710\text{-mV}_{\text{pp}}$  input signal and  $400\text{-mV}_{\text{pp}}$  output signal with the minimum gain ( $-5\text{ dB}$ )
- (18) calculated from the reported  $366\text{-}\mu\text{V}_{\text{rms}}$  integrated output noise value
- (19) for a  $500\text{-mV}_{\text{pp}}$  input signal
- (20) with max. gain
- (21) calculated from the reported  $860\text{-}\mu\text{V}_{\text{rms}}$  integrated output noise value
- (22) with the lowest bandwidth ( $44\text{-MHz}$ )
- (23) for a  $2.2\text{-V}_{\text{pp}}$  differential input signal
- (24) for a  $3.2\text{-mV}_{\text{pp}}$  input signal with the maximum  $40\text{-dB}$  gain at 80 MHz (input signal level is calculated from the reported output-referred power value of  $-6\text{ dBm}$ )
- (25) for a  $0.75\text{-V}_{\text{pp}}$  input signal at 150 MHz
- (26) calculated from the reported  $234\text{-}\mu\text{V}_{\text{rms}}$  input noise value
- (27) Although the in-band *IIP3* is not reported in the publication, it is evaluated for the comparison table with the assumption that the reported *THD* is equal to the *HD3*, as proposed in [40]. As a result of this assumption and on the basis of (2.5) and (2.6), it can be written

$$THD[dB] \approx HD3[dB] = 20 \log_{10} \left( \frac{1}{4} A_1^2 \left| \frac{\alpha_3}{\alpha_1} \right| \right). \quad (7.1)$$

The in-band *IIP3* can be evaluated by resolving the term  $\left| \frac{\alpha_1}{\alpha_3} \right|$  from

- (7.1) and substituting it into (2.9).
- (28) In-band SFDR calculated from the in-band noise and *IIP3* in the case of the max. bandwidth using (2.15).
- (29) Calculated from (2.19)
- (30) Calculated from (2.20)
- (31) Calculated from (2.21)
- (32) Calculated from (2.22)
- (33) with the filter bandwidth of  $150\text{-MHz}$

Table 7.7. Comparison to published 60-GHz CMOS receiver front-ends [4] (© 2009 IEEE).

	[41]	[42]	[43]	This work
Technology	90-nm CMOS	90-nm CMOS	90-nm CMOS	65-nm CMOS
Integrated Blocks	Antenna, LNA, mix, TIA, VCO, synth.	LNA, poly-phase, 2xmix, LO	LNA, mix, VGA, buffer	LNA, mix, IF amp, IF mix, IF IQ-gen, BB LPF+PGA, ADC
Max. gain	22.5 dB*	22 dB	55.5 dB*	79 dB
NF	8.4 dB**	5.7 to 8.8 dB	6.1 to 6.35 dB**	7.0 dB
P <sub>1dB,IN</sub>	---	-27.5dBm	-26dBm	-38.5dBm
S11	< -6.25 dB	---	< -10 dB	< -12 dB
Supply	1.2 V	1.2 V	1.0 V	1.2 V
P <sub>d</sub>	144 mW	36 mW	24 mW	198 mW
Area	2.64 mm <sup>2</sup> ***	0.185 mm <sup>2</sup> ***	1.55 mm <sup>2</sup>	2.8 mm <sup>2</sup>

\*Power gain instead of voltage gain

\*\* DSB NF

\*\*\*Active area without pads

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## 8 Conclusions

This thesis was focused on the design and implementation of analog baseband continuous-time low-pass filters for integrated wideband radio receivers. Throughout the thesis, radio receiver integrated circuits (ICs) were examined from the analog baseband filter standpoint. In the work, a total of five experimental analog baseband low-pass filter circuits were designed and implemented as a part of five single-chip radio receivers. Although the filters were designed for a certain radio system, the results of the research presented in this thesis can be utilized in other wideband applications as well.

To successfully detect a potentially weak desired signal lying among potentially large out-of-band interfering signals in a radio channel, the incoming signal is typically first amplified and filtered in a radio receiver before the signal demodulation and digitization. In this work, the low-pass filters were designed to have voltage gain to accomplish both of the aforementioned supportive signal-processing operations with a single circuit at the analog baseband. When aiming at wide bandwidths, continuous-time baseband filter realizations become the most practical choice, rather than their digitally intensive counterparts.

Different techniques to realize integrator-based continuous-time low-pass filters were introduced. The relationship between the integrator non-idealities and integrator Q-factor, as well as the effect of the integrator Q-factor on the filter frequency response, were studied on the basis of a literature review. The non-idealities of active devices forming an integrated filter easily cause the shape of the filter frequency response to deteriorate. The wide bandwidth that is required in wideband applications exacerbates the undesirable effect further. Therefore, the primary goal for the study presented in this thesis was to investigate whether integrated wideband continuous-time low-pass filters with an accurate frequency response shape can be implemented in standard ultra-deep-submicron CMOS technologies. The baseline for the study was to accept (i.e. live with) the non-idealities of the low-voltage, active devices forming the filter but to take their effect into account beforehand in the filter synthesis. As a result, in this thesis, it was

shown that the losses of a gm-C low-pass filter with embedded voltage gain can be taken into account in the filter synthesis. Moreover, it was shown that wideband gm-C leapfrog filters constructed from non-ideal finite-DC-gain integrators can be realized with a desired frequency response by predistorting the filter coefficients of the LC ladder prototype filter according to predefined losses. The feasibility of the filter design approach that was presented was demonstrated by means of three experimental gm-C filter implementations. The experimental results also show that as a limitation of the approach, the non-idealities must be quantities that can be measured and controlled in one way or another. This is not the case with undesired second-order effects, including parasitic capacitances and mismatches between the transistors, of which influence on the filter performance is considerably increased at very high frequencies.

Two evolution versions of fourth-order opamp-RC low-pass filters that were implemented in a 0.25- $\mu\text{m}$  SiGe BiCMOS technology for two single-chip multicarrier UTRA FDD WCDMA base-station receivers were presented, along with the experimental results of both the low-pass filters and the corresponding receivers. Because of the conventional filter design approach that was used, the BiCMOS opamps were designed to have a high 60-dB DC gain and wide 2-GHz GBW. The experimental results show that the first opamp-RC filter has a fixed  $-3$ -dB bandwidth of 9.8 MHz and fixed voltage gain of 11 dB. The  $-3$ -dB bandwidth of the second filter version can be programmed to four different bandwidths: 2.6 MHz, 5.2 MHz, 7.7 MHz, and 10.2 MHz. The voltage gain of the second filter version can be programmed from 12 dB to 24 dB in 6-dB gain steps. The filters achieve a low input-referred noise density, 11.2 nV/ $\sqrt{\text{Hz}}$  and 8.8 nV/ $\sqrt{\text{Hz}}$ , respectively, and a high in-band spurious-free dynamic range, 76 dB and 67 dB, respectively, at the expense of a high current consumption of over 80 mA from a 2.5-V supply. The first evolution version of the multicarrier receiver that was presented can receive four adjacent WCDMA channels simultaneously. The second multicarrier receiver version can be programmed to receive from one to four adjacent WCDMA channels. The experimental results of the receiver ICs show that it is feasible to implement a multicarrier WCDMA receiver on a single silicon chip.

The influence of the implementation of the mixer-baseband interface on the linearity of both the mixer and low-pass filter in integrated receivers was studied theoretically. It was concluded that the overall performance and the wireless application that is targeted determine whether it is preferable to use a voltage-mode or a current-mode mixer-baseband interface in a radio receiver. Moreover, the effect of the inability of pseudo-differential gm-C filter circuits to reject common-mode input signals in a

direct-conversion receiver was examined. On the basis of the analysis carried out, two error mechanisms originating from the combination of the even-order distortion of the mixer and the lack of input common-mode rejection in the filter were found.

Two evolution versions of fifth-order 240-MHz gm-C low-pass filters implemented for two single-chip WiMedia UWB direct-conversion receivers in standard 0.13- $\mu\text{m}$  and 65-nm CMOS technologies, respectively, were presented, along with the experimental results of both the low-pass filters and the second receiver version. In addition, the 65-nm CMOS filter implementation was also embedded into the I-branch of a single-chip 60-GHz dual-conversion receiver, the experimental results of which were presented as well. The state-of-the-art experimental results of the 240-MHz filters show that selective wideband gm-C filters can be realized in modern ultra-deep-submicron CMOS technologies by using pseudo-differential transconductors with a nominal DC gain as low as 24–26 dB. As a result of the filter design approach that was used, a voltage gain of almost 40 dB was implemented in the filters. The filters achieve an input-referred noise density as low as 7.8-nV/ $\sqrt{\text{Hz}}$  and they consume 24 mW and 36 mW, respectively, from a 1.2-V supply. The performance metrics of the second evolution version of the WiMedia UWB receiver in the BG1 operating mode was observed to be comparable to the existing ones. The experimental results of the 60-GHz receiver IC demonstrate that it is feasible to implement a broadband 60-GHz millimeter-wave front-end together with an analog baseband circuit and an ADC on a single silicon chip.

A third-order 1-GHz gm-C low-pass filter that was implemented rather as a test structure for the Q-branch of the 60-GHz receiver was presented. The measured frequency response of the third-order gm-C filter shows that the influence of the undesired second-order effects on the filter frequency response increases considerably as a function of frequency. Thus, the filter frequency response becomes inaccurate and unpredictable when extremely wide bandwidths are being targeted.

Wideband radio receiver ICs are needed in modern wireless applications, such as in wireless communication systems, to support ever-higher data throughputs. At the same time, single-chip power-efficient CMOS radio implementations are of special interest for consumer electronic products. The research work presented in this thesis was mainly addressed on both of these issues.

## Appendix A: Gain and denominator coefficients of (4.12)

In this appendix, corresponding to (4.12) of Section 4.2.1, the gain ( $G_{lossy}$ ) and denominator coefficients ( $x_0 - x_4$ ) of the transfer function of a lossy fourth-order LC ladder prototype filter shown in Fig. A.1 are presented. The coefficients are

$$\begin{aligned}
 G_{lossy} &= \frac{1}{L_2 C_3 L_4 C_5} \\
 x_0 &= \frac{(R_S + R_2) G_3 R_4 (G_L + G_5)}{L_2 C_3 L_4 C_5} + \frac{(R_S + R_2) G_3}{L_2 C_3 L_4 C_5} \\
 &\quad + \frac{(R_S + R_2)(G_L + G_5)}{L_2 C_3 L_4 C_5} + \frac{R_4 (G_L + G_5)}{L_2 C_3 L_4 C_5} + \frac{1}{L_2 C_3 L_4 C_5} \\
 x_1 &= \frac{G_3 R_4 (G_L + G_5)}{C_3 L_4 C_5} + \frac{G_3}{C_3 L_4 C_5} \\
 &\quad + \frac{(G_L + G_5)}{C_3 L_4 C_5} + \frac{(R_S + R_2) R_4 (G_L + G_5)}{L_2 L_4 C_5} + \frac{(R_S + R_2)}{L_2 L_4 C_5} \\
 &\quad + \frac{(R_S + R_2) G_3 (G_L + G_5)}{L_2 C_3 C_5} + \frac{(R_S + R_2) G_3 R_4}{L_2 C_3 L_4} \\
 &\quad + \frac{(R_S + R_2)}{L_2 C_3 L_4} + \frac{(G_L + G_5)}{L_2 C_3 C_5} + \frac{R_4}{L_2 C_3 L_4} \\
 x_2 &= \frac{(R_S + R_2) R_4}{L_2 L_4} + \frac{(R_S + R_2) G_3}{L_2 C_3} + \frac{R_4 (G_L + G_5)}{L_4 C_5} \\
 &\quad + \frac{1}{L_4 C_5} + \frac{G_3 (G_L + G_5)}{C_3 C_5} + \frac{G_3 R_4}{C_3 L_4} + \frac{1}{C_3 L_4} \\
 &\quad + \frac{(R_S + R_2)(G_L + G_5)}{L_2 C_5} + \frac{1}{L_2 C_3} \\
 x_3 &= \frac{(R_S + R_2)}{L_2} + \frac{G_3}{C_3} + \frac{R_4}{L_4} + \frac{(G_L + G_5)}{C_5} \\
 x_4 &= 1,
 \end{aligned} \tag{A.1}$$

where  $R_2$ ,  $G_3$ ,  $R_4$ , and  $G_5$  are the losses of the non-ideal gm-C integrators

mapped to the passive LC prototype filter as shown in (4.19).

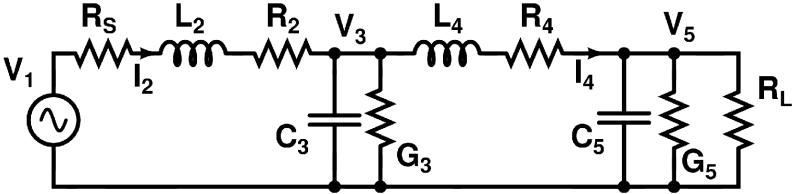


Figure A.1. Lossy fourth-order LC ladder prototype filter.





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