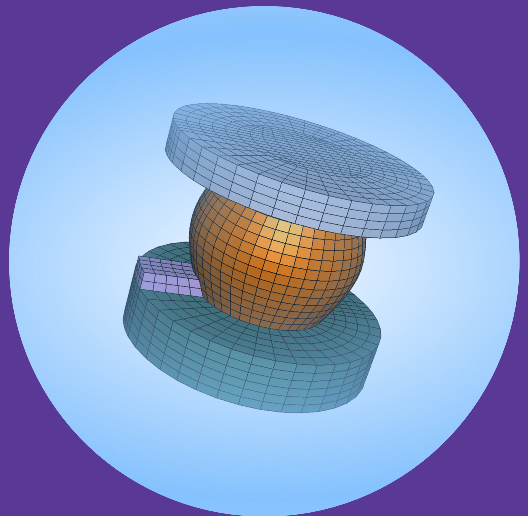
Department of Electronics

Numerical Simulations for Reliability Assessment of Lead-Free Solder Interconnections in BGA Packages

Jue Li



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Numerical Simulations for Reliability Assessment of Lead-Free Solder Interconnections in BGA Packages

Jue Li

Doctoral dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the School of Electrical Engineering for public examination and debate in Auditorium S4 at the Aalto University School of Electrical Engineering (Espoo, Finland) on the 21st of June 2011 at 12:00 o'clock.

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Abstract

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Abstract

This work presents the results of computer-aided numerical simulations for the reliability assessment of lead-free solder interconnections in BGA packages. The finite element and Monte Carlo methods were employed for the macroscale structural and the mesoscale microstructural simulations, respectively. The major reliability tests for electronic component boards, i.e. thermal cycling, power cycling and drop impact tests, were simulated via the finite element method. The results provide a feasible tool for a better understanding of the observed failure modes in the reliability tests. The lifetime predictions based on the simulation results are helpful for the lifetime estimations of the BGA packages. The temperature effects on the drop impact reliability of the BGA packages were successfully elucidated by the finite element numerical experiments. In addition, a new algorithm was developed in order to predict dynamic recrystallization in solder interconnections during thermal cycling. The approach was realized by combining the Potts model based Monte Carlo method and the finite element method. The correlation between real time and Monte Carlo simulation time was established with the help of the in situ test results. Recrystallization with the presence of intermetallic particles in the solder matrix was simulated by introducing the energy amplification factors in the particle-affected deformation regions. The present algorithm predicted both the incubation period of the recrystallization as well as the growth tendency of the recrystallized regions in a way consistent with the experimental findings.

Keywords BGA, Drop impact, Finite element method, Monte Carlo, Recrystallization, Thermal cycling

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Preface

This work has been conducted in the Electronics Integration and Reliability unit under the Department of Electronics at Aalto University. The work was financially supported by two projects, ‘TEMA’ and ‘CRT’, which were funded by the Finnish Funding Agency for Technology and Innovation (TEKES), Nokia, Nokia Siemens Networks, Efore Plc, NXP Semiconductors, Salon Teknopaja Oy and the National Semiconductor Corporation.

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Finally, I would like to express my thanks to my parents for their unequivocal love and support throughout my life.

Espoo, September, 2010

Jue Li

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List of Publications

This thesis consists of an overview of the following publications which are referred to in the text by their Roman numerals.

I J. Li, J. Karppinen, T. Laurila, J. K. Kivilahti, "Reliability of Lead-Free solder interconnections in Thermal and Power cycling tests," *IEEE Transactions on Components and Packaging Technologies*, vol. 32, pp. 302-308, 2009.

II J. Li, T. T. Mattila, J. K. Kivilahti, "Computational Assessment of the Effects of Temperature on Wafer-Level Component Boards in Drop Tests," *IEEE Transactions on Components and Packaging Technologies*, vol. 32, pp. 38-41. 2009.

III J. Li, T. T. Mattila, H. Xu, M. Paulasto-Kröckel, "FEM simulations for reliability assessment of component boards drop tested at various temperatures," *Simulation Modelling Practice and Theory*, vol. 18, pp. 1355-1364, 2010.

IV J. Li, T. T. Mattila, J. K. Kivilahti, "Multiscale Simulation of Microstructural Changes in Solder Interconnections during Thermal Cycling," *Journal of Electronic Materials*, vol. 39, pp. 77-84, 2010.

V J. Li, H. Xu, T. T. Mattila, J. K. Kivilahti, T. Laurila, M. Paulasto-Kröckel, "Simulation of Dynamic Recrystallization in Solder Interconnections during Thermal Cycling," *Computational Materials Science*, vol. 50, pp. 690-697, 2010.

VI J. Li, H. Xu, J. Hokka, T. T. Mattila, H. Chen, M. Paulasto-Kröckel, "Finite element analyses and lifetime predictions for SnAgCu solder interconnections in thermal shock tests," *Soldering & Surface Mount Technology*, vol. 23, July 2011 (in press).

Author's contribution

The author was responsible for writing the publications I-VI. In these publications, he conducted all the finite element modeling, stress-strain analyses and lifetime predictions, and established the Monte Carlo Potts model based algorithm for microstructural simulations. The reliability tests and experimental observations in these publications were carried out by the co-authors.

List of Abbreviations and Symbols

BGA	ball grid array
CAD	computer-aided design
CSP	chip scale package
CTE	coefficient of thermal expansion
FE	finite element
FEA	finite element analysis
FEM	finite element method
IMC	intermetallic
IMP	intermetallic particle
MC	Monte Carlo
min	minute or minutes
OPC	operational power cycling
PC	power cycling
PWB	printed wiring board
RT	room temperature
TC	thermal cycling or thermal cycle
WL-CSP	wafer level chip scale package

a	crack length
c_1	life prediction model constant
c_2	life prediction model constant
c_3	life prediction model constant
c_4	life prediction model constant
C	model constant
C^{pl}	temperature-dependent material constant
$H(S_i)$	stored energy of the site i
i	constant
j	constant

J	a unit of grain boundary energy in the MC model
k	Boltzmann constant
K_1	correlation constant
K_2	correlation constant
K_3	correlation constant
K_4	correlation constant
n	temperature-dependent material constant or model constant
N_0	number of cycles to crack initiation
N_f	characteristic life
S_i	site i
t	time
T	absolute temperature
W_{acr}	accumulated inelastic strain energy density per cycle
α	model constant
δ_{ij}	Kronecker delta
ε_{acr}	accumulated creep strain per cycle
γ_{pl}	rate independent plastic shear strain
γ_s	steady-state strain
σ	stress
τ	shear stress

1. Introduction

Nowadays, electronic products have become a necessity in our everyday life due to their extensive use in various applications. Among all the reliability concerns associated with the electronic products, solder interconnections that provide both mechanical and electronic connections are one of the key reliability concerns [1-5]. In this work, the solder interconnections of ball grid array (BGA) packages are studied since BGA packages have high interconnection density and small outlines, and are extremely popular in the electronics industry at the moment.

Almost all electronic products are subjected to temperature changes due to the internal heat dissipation of components or ambient temperature fluctuations. The coefficient of thermal expansion (CTE) mismatch between adjoining dissimilar materials results in the thermomechanical fatigue of solder interconnections, leading to the cracking of the interconnections and failures of the electronic products. Furthermore, electronic products, especially portable devices, are prone to accidental drop impacts during field use [6]. As the connection between surface mount components and printed wiring board (PWB), solder interconnections often experience extremely high strain rates and stresses, which probably lead to the failure of the interconnections as well as the devices [7-11].

Nowadays SnAgCu solder is the most used solder material in the electronics industry [12-15]. The microstructure of Sn-rich lead-free solder is significantly different from the traditional SnPb solder. The microstructure typically contains cells, dendrites, colonies of Sn and intermetallic (IMC) particles such as Cu_6Sn_5 and Ag_3Sn [16-20]. The complex microstructure affects the behavior and physical properties of the material, and eventually influences the reliability of the solder interconnections. It has been found that the as-solidified microstructure of SnAgCu solder can transform locally into a more or less equiaxed grain structure through recrystallization [16, 17]. Hence, there is a strong need for quantitative models which can explicitly predict microstructural changes in

solder interconnections during thermal cycling (TC) in order to establish a physically meaningful lifetime estimate.

Moreover, to improve the reliability of electronic products and at the same time to shorten the time for designing and testing, efficient test methods as well as accurate numerical simulations have become ever more important. In the industry, the finite element method (FEM) is a powerful numerical technique used in the design and development of products. FEM allows the visualization of structure deformation and indicates the distribution of stresses, displacements, temperatures and other physical fields [21, 22]. With the help of FEM, engineers can construct, refine and optimize their designs before the designs are manufactured. The FEM software, such as ABAQUS, ANSYS, MARC, and NASTRAN, provides a wide range of simulation options for both modeling and analysis of a system.

In the current work, finite element analyses were carried out to assess the reliability of lead-free solder interconnections in BGA packages subjected to various reliability tests including thermal cycling, power cycling (PC), and drop tests. Lifetime predictions of the BGA packages based on the simulation results were conducted. The simulation results offered explanations to the experimentally observed failure modes of the reliability tests. Moreover, a new algorithm combining the Potts model based Monte Carlo (MC) method and the finite element method was developed for microstructural simulation. Compared to the in situ experimental observations, a correlation between real time and MC simulation time was established. In addition, the intermetallic particles (Cu_6Sn_5 and Ag_3Sn) were explicitly modeled and the effects of the particles on recrystallization in solder matrix were included in the simulation. It is the first time that dynamic recrystallization and grain growth in solder interconnections have been simulated, and the effects of intermetallic particles on recrystallization in solder matrix were studied.

The thesis is organized as follows. A brief introduction of the major reliability tests and the associated failure modes are given in Section 2. Current understanding of the

microstructural changes in SnAgCu solder interconnections is addressed in Section 3. The numerical methods including FEM, MC method, and the hybrid algorithm are reported in Section 4. Section 5 presents stress-strain analyses. Section 6 deals with the lifetime predictions of solder interconnections. Finally, Section 7 gives the summary of the thesis including the main results and conclusions of the listed publications.

2. Reliability Tests and Failure Modes

The state-of-the-art of the component board reliability tests is briefly addressed here. Although thermomechanical and mechanical shock tests are traditional reliability tests of component boards, they still deserve a close look due to the concern that the numerous existing experiences associated with lead-containing solders may not be applicable to lead-free solders. Tests with combined loadings are the most realistic ones that represent the complex multiple loading conditions experienced by the electronic devices during their service life. Furthermore, the reliability concerns and observed failure modes of each loading condition are also presented in this section.

2.1 Thermomechanical Loading

Most thermomechanical reliability tests can be categorized into two broad groups, (i) thermal cycling and (ii) power cycling tests.

Thermal cycling tests subject the components and solder interconnects to alternating temperatures. The tests are conducted to determine the ability of the parts to resist a specified number of temperature cycles from a specified high temperature to a specified low temperature with a certain ramp rate and dwell time [23]. A traditional TC test cabinet usually includes a single chamber that is heated or cooled by introducing hot or cold air into the chamber with a temperature ramp rate normally less than 15 ℃/min. A number of investigations have been carried out in order to study the influence of the temperature profile on the solder interconnection reliability (e.g. [24-29]).

Another branch of TC testing is called thermal shock (TS) testing named after the high temperature ramp rate (15 ℃/min or higher). In general, TS tests are more efficient than the traditional TC tests. A TS test cabinet usually has a dual chamber (e.g. WEISS TS130). This type of tester is made of two stationary chambers. One is maintained at a fixed high temperature and the other one is maintained at a fixed low temperature. The

thermal loading is exerted by a moving platform that shuttles between the two stationary chambers. It is noteworthy that a temperature profile can be input into a thermal cycling tester for controlling the temperature during a cycle, however, only the temperatures and time spent at each chamber are controllable parameters in a thermal shock tester. This difference is significant for optimizing the testing parameters in order to accelerate the reliability tests. During thermal cycling and thermal shock tests, the package, solder interconnections, and PWB are nearly at the same temperature all the time while only negligible thermal gradients exist within the mounted package. The uniform distribution of temperature makes these tests rather different from power cycling tests.

Power cycling tests offer a more realistic representation of the actual operational conditions of electronic devices by increasing the temperature of the component when the power is on and allowing the temperature to decrease when the power is off [30-35]. Due to the nature of the PC test, there are large thermal gradients existing in the package, and sometimes the temperature difference between the hot and cold spots of the package can reach 60 ℃ (see Publication I). Compared to thermal cycling tests, power cycling tests are less accelerated but more realistic.

The main source of most thermally induced reliability failures in electronic packages is the CTE mismatch between adjacent dissimilar materials. There are two types of CTE mismatch: (i) a “global” CTE mismatch between the component and PWB, and (ii) a “local” CTE mismatch between the adjacent materials (e.g. solder, solder mask, and copper pad). During either the thermal cycling or power cycling, solder interconnections are subjected to the thermally induced low cycle fatigue, in a way similar to cyclic bending. Fatigue is one of the primary reasons for the failure of solder interconnections under thermomechanical loadings. Fatigue is the progressive structural damage that occurs when a material is subjected to cyclic loading with stresses below its ultimate tensile stress. Fatigue crack initiation, as well as propagation, strongly depends on microstructure, temperature, stress ratio, and loading frequency, making the failure analysis of the solder interconnections a significant challenge. According to the experimental observations, the fractures initiating at the surfaces of solder

interconnections usually are located on the component side or PWB side of the critical solder interconnections that experience the highest levels of stresses and strains. The critical solder interconnections are often the die edge interconnections (beneath the silicon die corner) or the outermost interconnections (beneath the package corner). For instance, two typical cracked critical solder interconnections are shown in Figs. 1 and 2. The micrographs are from the thermomechanical reliability study of a BGA package (see Publication I). The crack in Fig. 1 is wide, relatively straight, and propagates along the interface just below the intermetallic region. The cross-polarized light image shows that the fracture mode is a mixed intergranular (the fracture follows the grain boundaries) and transgranular (the fracture travels through the grains) fracture. This type of fracture is the primary failure mode in both TC and PC tests. The secondary critical solder interconnections are the outermost interconnections (see Fig. 2). The crack is composed of multiple fronts and propagates through the interconnection along the grain boundary in an intergranular manner. This type of fracture is mainly observed in TC tests.

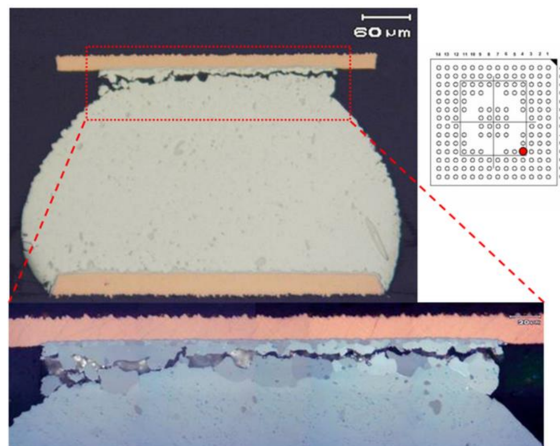

Fig.1. Crack path and the location of the primary critical solder interconnection (TC 5500 cycles). (reprinted with permission from IEEE)

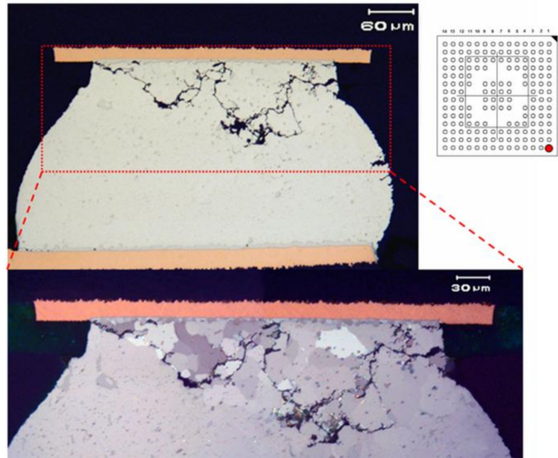

Fig.2. Crack path and the location of the secondary critical solder interconnection (TC 5500 cycles). (reprinted with permission from IEEE)

2.2 Mechanical Shock Loading

Drop impact reliability is crucial to all electronic products, especially portable devices since these products are more prone to being dropped during their service life. The drop tests usually follow the JEDEC standard [7]: 1500 G deceleration and 0.5 ms half-sine pulse shape. The test is designed to evaluate and compare the drop performance of surface mount electronic components for handheld electronic product applications in an accelerated way while duplicating the failure modes normally observed after a product level test. A typical drop tester is shown in Fig. 3.

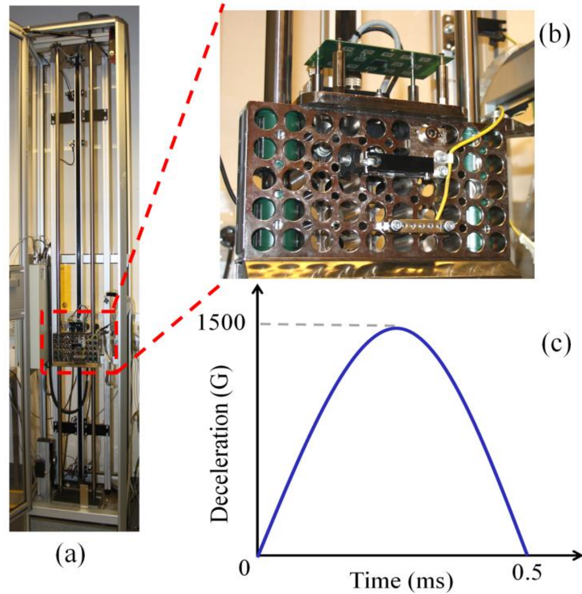

Fig. 3. Drop test setup and input shock pulse: (a) board level drop tester; (b) enlarge view of the tester (PWB, supporting rods, and base plate); (c) Input shock pulse (1500 G deceleration, 0.5 ms duration, half-sine pulse). (reprinted with permission from Elsevier)

During the drop events, the electrical failures may originate from various failure modes such as cracking of the PWB, copper trace cracking, cracking of solder interconnections, as well as component cracking. Among the different types of failure modes, the crackings of solder interconnections and copper trace are the most frequently observed ones [8-11]. The critical solder interconnections are typically the outermost ones. The cracking of solder interconnections usually takes place in the intermetallic layers at the interface between the solder and copper pad, and thereby, this failure mode is also called intermetallic layer cracking. Three micrographs are given in Fig. 4 to show the observed cracking of the intermetallic layer and copper trace in drop tests.

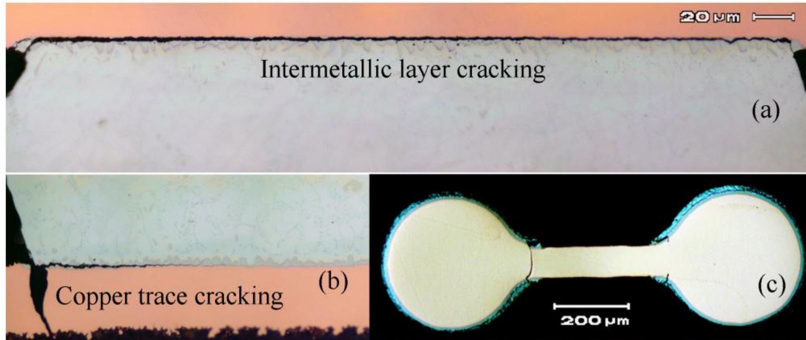

Fig. 4. Two typical failure modes of drop tests (a) intermetallic layer cracking (b) copper trace cracking (c) copper trace cracking (top view). (reprinted with permission from Elsevier)

2.3 Combined Loading

It is likely that the temperatures inside the products are well above their ambient when they experience mechanical shocks, meaning that thermomechanical loading as well as mechanical shock loading is simultaneously applied to the devices. Combined loading tests are thus necessary in order to better assess the reliability of component boards. In the combined loading test, the component boards are heated up locally by the integrated heating elements, and then drop tested at designed elevated temperatures. Details of the combined loading tests are presented in Publications II and III.

Since most of the material properties in the assembly are temperature dependent, the influences of temperature change on the drop impact reliability are highly complicated. Neglecting other trivial factors, the influences of increasing temperature can be analyzed by three major factors: (i) the change of PWB stiffness, (ii) the change of yield strength and elastic modulus of solder, and (iii) the effect of thermomechanical residual

stress. The temperature dependent material properties of the PWB and SnAgCu solder are listed in Table 1. With increasing temperature, the PWB becomes softer, resulting in a larger value of deflection during the drop impact and eventually leading to more significant plastic deformations in the solder interconnections. However, the yield strength and elastic modulus of solder decrease with increasing temperature, leading to the lower stresses and more plastic deformations. Furthermore, the component size and PWB structure have been found to have a significant influence on the reliability of the component boards under combined loading conditions (see Publications II and III).

Table 1
Temperature dependent material properties

Materials	Temperature (℃)	Strain rate (%/s)	Young's modulus(MPa)	Yield strength (MPa)
PWB	0	—	18.0 E+3	—
	140		12.7 E+3	
SnAgCu	0	100	52.4 E+3	34
	140		40.6 E+3	20

Several different packages have been studied and the observed failure modes associated with the combined loadings are more complex than those of the single loading tests. Besides the intermetallic layer cracking and copper trace cracking as shown in Fig. 4, a new failure mode, combined intermetallic layer and bulk solder cracking, has been observed. An example is shown in Fig. 5, where the failure mode of the wafer level chip scale packages (WL-CSP) gradually changes from the intermetallic layer cracking to the bulk solder cracking with increasing test temperature. In addition, the failure mode of one type of BGA package was found to be the component side intermetallic layer cracking at the room temperature and the PWB side copper trace cracking at the high temperature (70 ℃ or higher). The failure mode of another type of BGA package was found to be always the intermetallic layer cracking.

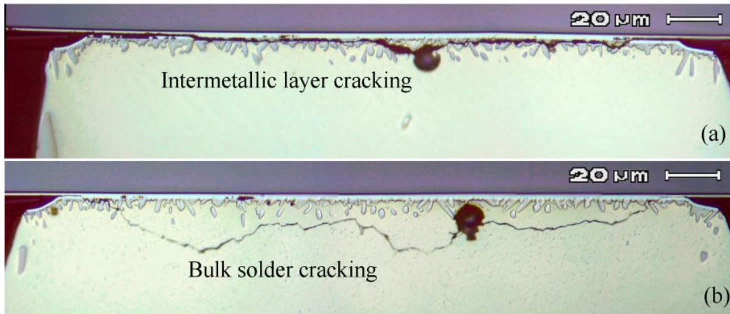

Fig. 5. Failure modes of WL-CSP gradually change from the intermetallic layer cracking to the bulk solder cracking: (a) failure mode at RT; (b) failure mode at 100 ℃. (reprinted with permission from Elsevier)

3. Microstructural Changes in SnAgCu Solder Interconnections

Two micrographs of the same solder interconnection but from different stages of the thermal cycling test are presented in Fig. 6 in order to show the microstructural changes of solder interconnections. The as-solidified microstructure of SnAgCu solder interconnections are usually composed of several large Sn-based colonies (typically less than five) separated by high angle boundaries [16, 17]. During cyclic thermomechanical loading, a fraction of the energy associated with the plastic deformation of solder interconnections is stored in the metal, mainly in the form of point defects and dislocations. The stored energy is subsequently released during restoration, which can be divided into three main processes: recovery, primary recrystallization and grain growth. Recovery and recrystallization are two competing processes, which are driven by the increased internal energy of the deformed material. Recovery decreases the driving force for recrystallization and thus hinders the initiation of recrystallization. In high stacking fault energy metals such as Sn, the release of stored energy takes place so effectively by recovery that recrystallization will not practically take place [20, 36, 37]. Studies have shown that after a single deformation static recrystallization rarely occurs in Sn-rich solders [37]. However, under dynamic loading conditions such as in thermal cycling tests, recrystallization often occurs in the high stress concentration regions of solder interconnections. In the recrystallized region a continuous network of high angle grain boundaries provides favorable sites for cracks to nucleate and to propagate intergranularly, which can lead to failures in the solder interconnections [20].

Besides the microstructural changes in Sn matrix, the interfacial IMC layer growth and morphology changes have been found to have a significant influence on the solder interconnection reliability (e.g. [38]). Cu_6Sn_5 is the first detectable phase to form at the Cu/Sn interface during soldering and Cu_3Sn is usually observable after the annealing or thermal cycling. Based on the annealing studies, it has been concluded that from room temperature up to 50-60 ℃ only the Cu_6Sn_5 layer growth is detectable and it is

controlled by the release of Cu atoms from the Cu lattice. Above 60 ℃ the Cu_3Sn layer starts to grow at the expense of the Cu_6Sn_5 layer, and meanwhile, both Cu and Sn are mobile (see [39] for more information). Compared to the annealing, the IMC layer growth rate is accelerated during thermal cycling as a result of the thermomechanical stress generated by the CTE mismatch. Furthermore, under high current density the electromigration plays a significant role in the growth of the IMC layer. Due to the "electron wind", the atoms are transported in the directions of the electron-flow, resulting in the microvoid formation near the cathode and the "hillocks" formation near the anode. As discussed in Section 2, cracks usually propagate along the IMC/solder interface under thermomechanical loading or within the IMC layer under mechanical shock loading. Hence, the IMC layer growth is a significant reliability concern in electronics devices.

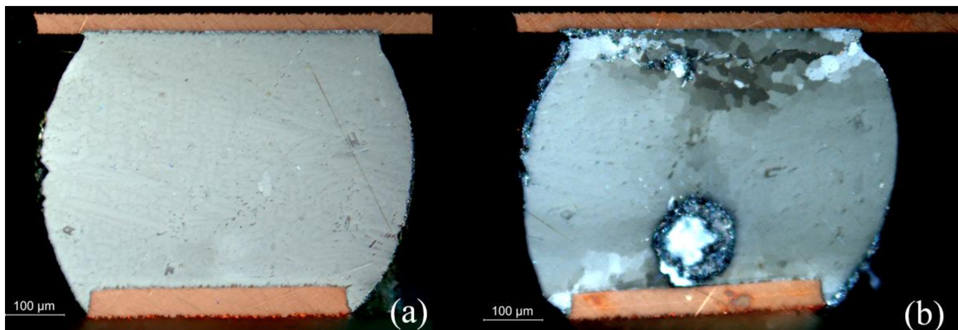

Fig. 6. (a) as-solidified microstructure of a SnAgCu solder interconnection observed with cross-polarized light, (b) the same interconnection after 1000 thermal cycles.

A thorough understanding of the microstructural changes in solder interconnections is of great importance to the reliability studies of electronic products. The motivation for the microstructural simulation work presented in this thesis is to offer better understanding and to provide a quantitative description of the restoration processes, i.e. recrystallization and recovery, in solder interconnections.

4. Numerical Methods for Simulations

The finite element method has been employed for the macroscale structural simulation and the Monte Carlo method for the mesoscale microstructural simulation. The brief introductions to the FE method and the MC method, their main features, and the specific techniques used in the current work are addressed in this section. In addition, the newly developed hybrid algorithm for microstructural simulations of solder interconnections during thermal cycling is also presented.

4.1 Finite Element Method

The finite element method originated from the discretization of continuous problems. In the 1940s it was successfully used to solve complex elastic continuous problems in civil engineering [40, 41]. From the middle 1950s to the late 1960s, a lot of progress was made by mathematicians and engineers. The key FEM concepts, such as the stiffness matrix and element assembly, were developed in the late 1950s. The finite element software NASTRAN was developed for NASA in the late 1960s. In 1974, the finite element method was provided with a rigorous mathematical foundation by Strang and Fix [42]. Nowadays, the method is applied to a wide variety of engineering fields, such as structural mechanics, fluid dynamics, and electromagnetics.

The finite element method is a numerical approach for finding approximate solutions to partial differential equations. The continuum is divided into a finite number of elements and the elements are assumed to be interconnected at a discrete number of nodal points situated on their boundaries and occasionally in their interior. In structural analysis, the displacements of these nodal points will be the basic unknown parameters of a problem.

4.1.1 Finite Element Analysis Process

A typical finite element analysis (FEA) process includes the following seven steps.

(1) *Model creation*: The model is drawn in a pre-processor or other CAD software.
(2) *Mesh generation*: The finer mesh usually leads to better results but requires longer analysis time, and thereby, there is a trade-off between accuracy and solution speed.
(3) *Assigning material properties*: The material properties are defined and the suitable material models are chosen.
(4) *Applying loads*: For instance, displacement in a stress analysis or heat generation in a thermal analysis.
(5) *Applying boundary conditions*: A boundary condition may be applied to all directions (x, y, z) or to certain directions only. Zero displacements are usually used in stress analysis, and specified temperatures in thermal analysis.
(6) *Solution*: The analysis types (e.g. static, transient, implicit, and explicit) are defined. The time increment procedure and error control are specified.
(7) *Post-processor*: the results are read and interpreted. They are usually visualized in the form of a contour plot or presented in a table.

The following points are crucial to a successful finite element analysis. In addition, they are also useful checkpoints for improving the quality of an FEA.

(1) To establish a simplified and approximately accurate geometry representation.
(2) To choose appropriate element types, mesh, material properties, and material models.
(3) To apply accurate loads and boundary conditions.
(4) To use appropriate analysis type and error control.

4.1.2 Finite Element Techniques

In the current work, two specific finite element techniques, the “submodeling” and “global-local” techniques, are employed in different simulations. Both techniques are addressed in detail in the following text.

The submodeling technique is used in order to obtain accurate results of a local part of a model with a refined mesh. It is based on interpolation of the solution from an initial, relatively coarse global model. For instance, in a structural analysis the calculated displacements of the global model are stored and used as the boundary conditions in the submodel. The details included in the submodel have no effect on the global behavior. The submodeling technique is most useful when the detailed solution in a local region is required and the detailed modeling of that local region has a negligible effect on the overall solution. Besides, according to the element type of the global model and submodel the submodeling can be solid-to-solid, shell-to-shell, or shell-to-solid.

The global-local technique is useful when the accurate results of a local part are necessary. A fine mesh is applied to the local part while a relatively coarse mesh is applied to the global model. The constraint equations are used to tie together the dissimilar meshes. The variables are transferred along the boundary between the global and local models. Different from the submodeling technique, the details of the local model have influence on the global behavior when the global-local technique is used.

4.1.3 Material Models

In mechanics, material models are the quantitative descriptions of material behaviors (e.g. elastic, plastic, or creep). A material model usually composes of a set of constitutive equations relating stresses and strains, e.g. Hooke's law for the constitutive relation of linear materials. Choosing suitable material models during FEA is crucial to the accuracy of stress-strain analyses.

In general, deformations of materials are categorized into elastic, rate-independent plastic, and creep (also called rate-dependent plastic or viscoplastic) deformations. Rate-independent plastic deformations are irreversible and take place almost instantaneously as the applied stress is beyond the yield stress. Creep deformations usually occur over a long period of time when the materials are exposed to a relatively high temperature and a mild loading. In order to avoid misunderstanding, in the following text the term

"plastic" is used to denote "rate-independent plastic" and "creep" for the "rate-dependent plastic".

The Anand model is the most popular viscoplastic model to describe solder deformation as SnAgCu solder shows viscoplastic deformation characteristics when subjected to temperature cycle loadings. The model is often used for modeling metal behaviors under elevated temperature when the behaviors become very sensitive to strain rate, temperature, and the history of the strain rate and temperature [43]. The model is composed of a flow equation and three evolution equations that describes strain hardening or softening during the primary stage of creep and the secondary creep stage (see [43] for more information). Different from other models, the Anand model needs no explicit yield condition and involves one state variable, i.e. the scalar non-zero variable called deformation resistance, in order to describe strain hardening or softening. In addition, the Anand model is available in the FEA software ANSYS and users can easily employ the model for FE modeling without extra coding work. This fact is another reason for the popularity of the model.

Besides the Anand model, a lot of researchers have treated solder alloys as "elastic + plastic + creep". The plastic deformation is normally described by a power law relationship (e.g. [44]).

$$\tau = C^{pl} \, {\gamma_{pl}}^{n} \tag{1}$$

where τ and γ_{pl} are the shear stress and the rate independent shear strain, respectively. C^{pl} and n are both temperature-dependent material constants. The steady-state creep of SnAgCu can be well described by a hyperbolic sine stress function (see Eq. 2). One of the popular creep models was developed by Schubert et al. [45, 46].

$$\frac{d\gamma_s}{dt} = C \left[\sinh(\alpha\sigma)\right]^n \exp\left(\frac{-Q_a}{kT}\right) \tag{2}$$

where γ_s is the steady-state strain, k is the Boltzmann's constant, T is the absolute temperature, σ is the applied stress, Q_a is the apparent activation energy, and C, α, and n are constants.

It is noteworthy that many life prediction models for solder interconnections are associated with certain material models. For instance, the Darveaux's prediction model [47] employs the Anand constitutive model during FE modeling and the Schubert's approach uses the materials models, "elastic + plastic + creep", as previously discussed. Using unsuitable material models may lead to significant errors in the lifetime predictions.

4.2 Monte Carlo Method

The Monte Carlo method is named after the Monte Carlo Casino in Monaco. The systematic development of the method dates back to 1944 [48, 49]. After the first electronic computer appeared, the Monte Carlo methods began to be studied in depth. In the 1950s they were used in the work related to the development of the hydrogen bomb. Later, the method became popular in computational physics, computational material science, physical chemistry, and related applied fields.

The Monte Carlo methods are a class of stochastic techniques that rely on repeated random sampling to investigate problems. Since the methods rely on repeated computation of random numbers (trial and error), they are especially suitable to be carried out on computers. Monte Carlo methods are useful in studying systems with a large number of coupled degrees of freedom and for modeling phenomena with significant uncertainty in inputs.

The expression "Monte Carlo method" is very general, meaning that the term describes a large and widely-used class of approaches. These approaches tend to follow a specific pattern as follows.

(1) Define a domain of possible inputs.
(2) Generate inputs randomly with a certain specified probability distribution.
(3) Conduct a deterministic computation using the inputs.
(4) Aggregate the results of all the individual computations into the final result.

In the current work, a Potts model based Monte Carlo method is used to simulate the microstructural changes of solder. In the Potts model, the material is divided into a number of discrete points and sites, which form a regular lattice (see Fig. 7). The model does not simulate the behavior of single atoms, and thereby, each MC lattice site represents a large cluster of atoms with the typical size being in the order of micrometers. Within each site the microstructure is assumed to be homogeneous. Each site is given a number corresponding to a grain orientation and two adjacent sites with different grain orientation numbers are regarded as being separated by a grain boundary. A group of sites having the same orientation number and surrounded by grain boundaries are considered as a grain.

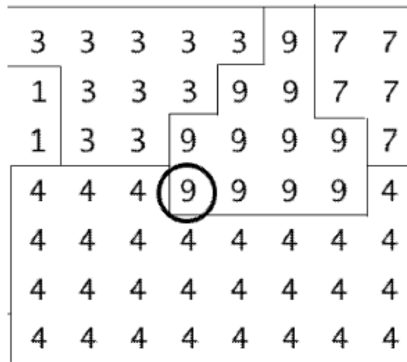

Fig. 7. Schematic show of the MC lattice

The grain boundary energy and the volume stored energy are taken into consideration in the energy minimization calculations to simulate the recrystallization and grain growth processes. Each site contributes an amount of stored energy, $H(S_i)$, to the system, and

each pair of unlike neighboring sites contributes a unit of grain boundary energy, J, to the system. When using the square lattice as shown in Fig. 7, the first and second nearest neighbors are included in the energy calculation, and thereby, each site has eight nearest neighbors. For example, the site with the number "9" inside the circle has eight nearest neighbors, and four of which are unlike neighboring sites. The nucleation of recrystallization is modeled by introducing nuclei (small embryos with zero stored energy) into the lattice.

In the reorientation process, if the randomly selected site is unrecrystallized, it will be recrystallized under the condition that the total energy of the system is reduced. If the selected site is recrystallized, the reorientation process is a simulation of the nucleus growth process. The total energy of the system, E, is calculated by summing the volume stored energy and the grain boundary energy contributions throughout all the sites.

$$E = J \sum_{<ij>} (1 - \delta_{S_i S_j}) + \sum_i H(S_i) \tag{3}$$

where the sum of i is over all N_{MC} sites in the system, the sum of j is over all the nearest-neighbor sites of the site i, and δ_{ij} is the Kronecker delta.

4.3 Hybrid Algorithm

The Monte Carlo simulation approach provides a convenient way to simulate the changes in the microstructure of materials, however, the treatment of heterogeneous nucleation and inhomogeneously deformed material still remains a challenge for the simulation. Hence, hybrid methods are needed to perform the task. As steps in this direction, Rollett and Raabe [50] developed a hybrid model for mesoscopic simulation of recrystallization by combining the MC and Cellular Automaton methods. Song and Rettenmayr [51] presented a hybrid MC model for studying recovery and recrystallization of titanium at various annealing temperatures after inhomogeneous deformation. Furthermore, hybrid models, combining FEM and recrystallization models, have been developed in earlier work. For instance, Yu and Esche [52]

combined the MC method with the finite element method in order to simulate the microstructure of structural materials under forging and rolling; Zambaldi et al. [53] modeled the indentation deformation and recrystallization of a single crystal nickel-based superalloy; and Raabe and Becker [54] combined a plasticity finite element model with a probabilistic cellular automaton for simulating primary static recrystallization of aluminum. Nevertheless, most of the previous studies are limited to static recrystallization or relatively simply loading conditions such as annealing.

In this study, a new hybrid algorithm, combining the Potts model based Monte Carlo and finite element methods, has been developed in order to predict the dynamic recrystallization of Sn in Sn-rich lead-free solder interconnections during thermal cycling. The approach is based on the principle that the stored energy of solder is gradually increased during each thermal cycle. When a critical value of the energy is reached, recrystallization is initiated. The stored energy is released through the nucleation and growth of new grains, which gradually consume the strain-hardened matrix of high dislocation density.

In order to schematically describe the simulation process, a flow chart is shown in Fig. 8. There are three major steps in the process and all the key inputs for the simulation are listed in the boxes, which are on the left side of each step. In Step I, the finite element method is employed to calculate the inelastic strain energy density of the solder interconnections under thermal cycling loads. As discussed above, it is assumed that the net increase of the stored energy takes place after every thermal cycle. In Step II (scaling processes), the stored energy, as the driving force for recrystallization, is mapped onto the lattice of the MC model, and moreover, a correlation is established to convert real time to MC simulation time with the help of the in situ test results. In Step III, the grain boundary energy and the volume stored energy are taken into consideration in the energy minimization calculations to simulate the recrystallization and grain growth processes. Furthermore, intermetallic particles are treated as inert particles and their influence on the distribution of stored energy is included. Details of the three steps are presented in Publications IV and V.

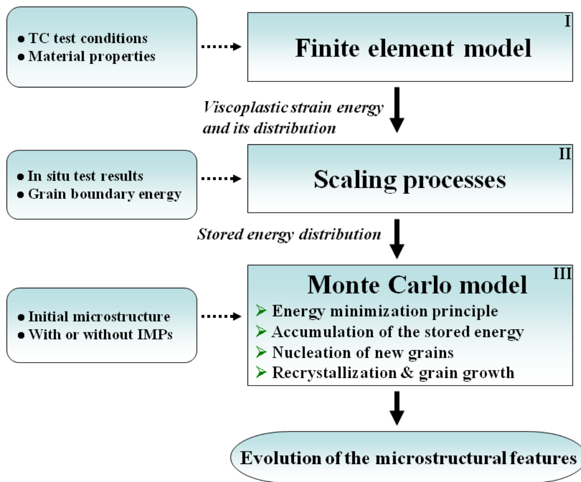

Fig. 8. Flow chart for the simulation of microstructural changes in solder interconnections. (reprinted with permission from Elsevier)

5. Stress-Strain Analyses

Stress-strain analyses based on the FE simulations can help researchers understand behavior, limits, and interactions of complex processes, explain observed failure mechanisms, and improve designs. The following subsections present the major contributions of the stress-strain analyses to the reliability assessment of solder interconnections in BGA component boards.

5.1 Mechanical Responses of Component Boards

The analysis of the PWB deformation during either thermomechanical or drop impact tests provides an insight into the stress-strain state of solder interconnections. During the thermal cycling or power cycling tests, solder interconnections are subjected to thermally induced fatigue. The cyclic loading makes solder interconnections under a complicated triaxial stress state as a result of the CTE mismatches. The bending of the component board in both TC and PC cases are schematically shown in Fig. 9. Due to symmetry, only half of the component board is presented in the figure. In the TC test, the temperature distribution is relatively uniform. The PWB expands more than the BGA component when the temperature is increased and shrinks more than the BGA component when the temperature is decreased. As a result, during thermal cycling the component board bends upwards at high temperature and downwards at low temperature. On the contrary, during power cycling the component board bends downwards when the power is on and upwards when the power is off. In the PC test, the heat generation is inside of the component and the high temperature distribution is localized in the center of the PWB where the component is located. The component expands more than the PWB when the power is on, leading to the downward bending of the component board. The upward bending of the component board during PC can be explained in the same manner.

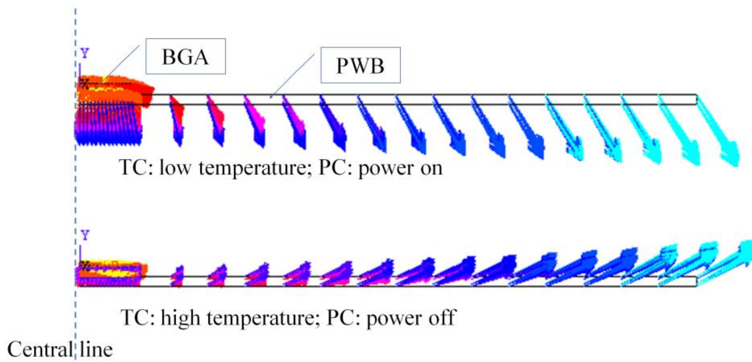

Fig. 9. Side view of the displacement vectors of the component board. (reprinted with permission from Emerald)

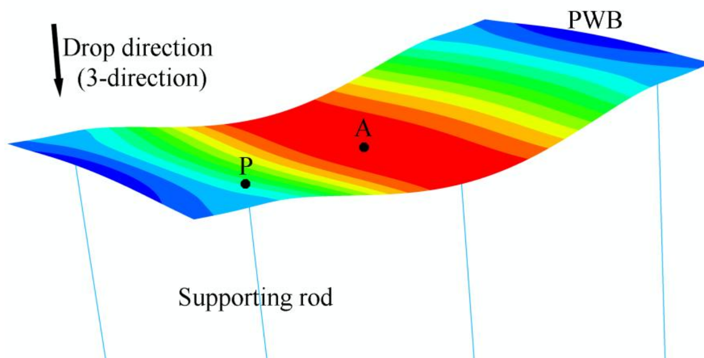

Fig. 10. 3-direction displacement contour of a PWB during a drop test, where points A and P are the center of the PWB and the supporting point, respectively. (reprinted with permission from Elsevier)

On the other hand, during the mechanical shock tests the component boards tend to bend downwards due to the impact and the inertial force. Fig. 10 gives a typical displacement contour of a PWB during a drop test. The PWB deflection is defined by the relative 3-direction displacement between the center of the PWB, point “A”, and the supporting point, point “P”. If the applied loading condition follows the JEDEC standard, the deflection value is usually about 5 mm. Larger values of the PWB deflection result in larger strains and stresses inside the assembly, and finally lead to the

earlier failure of the component boards. Furthermore, the strain rate during a mechanical shock test is notably high (about 100 %/s), and therefore, modeling the materials as “elastic + plastic” is sufficiently accurate.

5.2 Crack Initiation and Propagation

Since one failed solder interconnection will result in the failure of the component as well as the electronic device, to understand the crack initiation and propagation of the critical solder interconnections becomes one of the primary objectives of the FEA. During the result post-process, the solder interconnections with the highest stresses or strains are regarded as the critical ones. The analyses indicate that under thermomechanical loadings the critical solder interconnections are normally in the vicinity of the die edges and under drop impact tests the critical solder interconnections are the outermost ones, which are in good agreement with the experimental findings presented in Section 2.

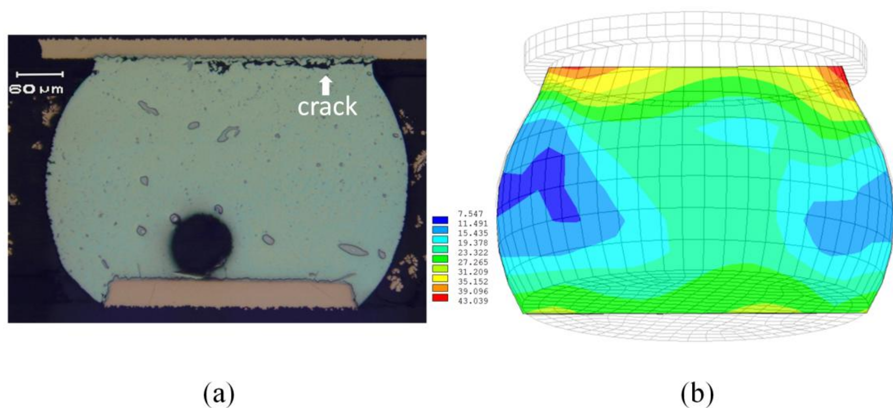

Fig. 11. (a) Micrograph of the critical solder interconnection from TS14; (b) von Mises stress contour of the same cross-section at the low-temperature stage (units: MPa). (reprinted with permission from Emerald)

The stress-strain analyses add insights into the crack initiation and propagation of the critical solder interconnection. For example, a cross-section micrograph of a cracked critical solder interconnection from the thermal shock test with 14 min cycle time (TS14) is shown in Fig.11. Besides the micrograph, a von Mises stress contour mapped on the same cross-section of the interconnection is also given. Comparing Fig. 11(a) with Fig. 11(b), it is found that the crack initiates from the corner of the solder interconnection where the high stress concentration is located. Throughout the whole interconnection, the region with the relatively high stresses is adjacent to the component side interface, providing a clue to the observed crack propagation path.

In some cases, the locations of the critical solder interconnections may change due to the different designs of the package and loading conditions. As an example the main processing unit of the cell phone studied in the reference [55] is shown in Fig. 12. The application engine component is a stacked-die BGA package-on-package design and was subjected to operational power cycling (OPC).

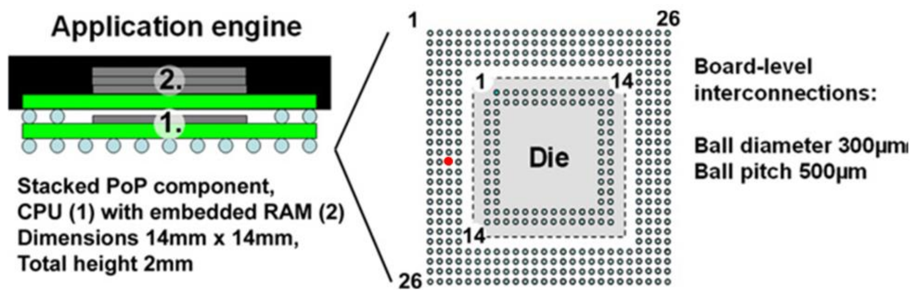

Fig.12. Predicted location of the critical solder interconnection of a stacked package-on-package component under operational power cycling.

According to the simulation results, the critical solder interconnection of the OPC test has been found to be located in the middle of the third rows (see the red dot in Fig. 12). Again, the micrograph and the calculated stress contour figure of the critical solder interconnection are given in Fig. 13. No obvious cracks are found in the micrograph, which is understandable since no failures were detected during the two-year OPC. All

the solder interconnections in the BGA have been carefully checked and no other interconnections show such significant microstructural changes as the solder interconnection shown in Fig. 13(a) [55]. The recrystallized microstructure at the interfacial regions of the interconnection suggests that plastic deformation induced microstructural evolution has taken place and eventually cracks will occur in these regions.

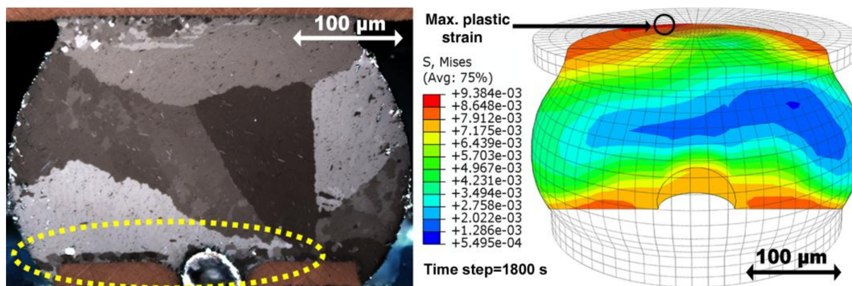

Fig. 13. Left: Polarized light cross-sectional image of the critical interconnection in OPC. Right: Calculated stress contour map of the critical interconnection.

5.3 Optimization of Temperature Profiles

Choosing optimized temperature profiles for the thermal cycling or thermal shock tests of component boards by means of stress-strain analyses has received a lot of attention over the last ten years. For instance, Zhai et al. [24] studied the lifetimes of the SnPb BGA assemblies under different ramp rates and dwell time, and Clech [27] studied the effects of thermal cycling ramp rate and dwell time on different CSP assemblies. The objective of the optimization is to find the shortest test time as well as to duplicate the same failure modes observed in the product level tests. Generally speaking, an optimized temperature profile for all types of components or PWBs does not exist due to different package designs and materials. However, the conclusions obtained from an FEA of a certain component board are applicable to other similar component boards. Before starting a time-consuming thermomechanical test of a new type of component

board, it is highly recommended to carry out an FEA in order to optimize the temperature profiles.

Stress-strain hysteresis loops are often employed to compare different temperature profiles. For example, three hysteresis loops for three thermal shock profiles (TS14, TS34, and TS44) are shown in Fig. 14. The three temperature profiles have different cycle times (14, 34, and 44 min). In the figure, the turning points of the TS14 loop are labelled as A, B, C, and D so that the loop is divided into four segments (each segment is associated with a certain temperature stage). Surrounding the hysteresis loops, four red dashed lines with arrows are used to schematically depict the process of the temperature change during one cycle. With the help of the hysteresis loops and the red dashed lines, the evolution of the stress during each temperature stage can be easily distinguished. For instance, the stress is relaxed from A (7.9 MPa) to B (3.7 MPa) during the high temperature dwell. Furthermore, the accumulated strain energy density within one cycle has been calculated (the area in the centre of a hysteresis loop is the accumulated strain energy density). The total accumulated strain energy density of the TS14 loop is 8.04 MPa and the contributions from the dwell and the ramp portions are 2 % and 98 %, respectively. The shapes of the three hysteresis loops in Fig. 14 are similar since all the cases share the same extreme temperatures and ramp rate. Increasing the dwell time increases the area of the hysteresis loops. Nevertheless, TS14 has the largest ratio (0.57 MPa/min) between the accumulated strain energy density and the cycle time, making TS14 a candidate for the most accelerated test. Regardless of the effect of dwell time on the microstructural changes, e.g. recrystallization of Sn, it can be concluded that a shorter cycle time in terms of less dwell time leads to a more efficient thermal shock test.

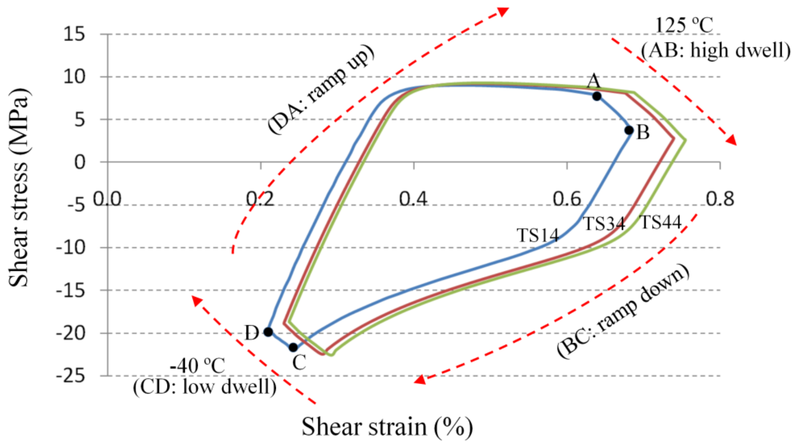

Fig. 14. Hysteresis loops for the critical solder interconnections of TS14, TS34, and TS44. (reprinted with permission from Emerald)

5.4 Influences of Multiple Factors

In complex processes, there are multiple factors affecting the final failure modes. The interactions of these factors prevent researchers from individually studying these factors by experiments. In such cases, numerical experiments based on FEA are most helpful to elucidate the influences of multiple factors and offer explanations to the observed failure modes.

As an example, the numerical experiments have been designed to study the failure modes of the combined loading tests discussed in Section 2.3. Table 2 gives the details of the three comparison cases and the factors under study. In the table, the 1st step is a thermomechanical analysis, which simulates the response of the component boards due to the temperature change, from room temperature to the elevated temperature. The 2nd step is to quantify the effect of the pure mechanical shock load while the assigned temperature distribution of the component board remains unchanged. The reference case uses the room temperature values for the material parameters. Case I uses the 100 ℃

values and includes all the three factors studied. Unlike Case I, Case II is constructed by excluding the first step, i.e. the effect of thermomechanical residual stress from the calculations while utilizing the 100 ℃ as the reference temperature for the material properties. Case III is similar to Case II but uses material properties at room temperature for the solder. The motivation behind Case III is to focus on the effect of PWB stiffness while excluding the other factors. With the help of the comparison cases, a series of stress-strain analyses have been carried out and the observed failure modes have been well explained (see Publications II and III).

Table 2
Three comparison cases designed for studying the effects of temperature change

<table>
<tr><th colspan="2"></th><th>Reference</th><th>Case I</th><th>Case II</th><th>Case III</th></tr>
<tr><td colspan="2">The 1st step</td><td>—</td><td>Included</td><td>—</td><td>—</td></tr>
<tr><td rowspan="2">The 2nd step: values for the material parameters</td><td>23 ℃</td><td>PWB, solder</td><td>—</td><td>—</td><td>solder</td></tr>
<tr><td>100 ℃</td><td>—</td><td>PWB, solder</td><td>PWB, solder</td><td>PWB</td></tr>
<tr><td colspan="2">Factors taken into account</td><td>—</td><td>a, b, c</td><td>a, b</td><td>a</td></tr>
</table>

a) the change of PWB stiffness; *b*) the change of yield strength and elastic modulus of solder; *c*) the effect of thermomechanical residual stress.

6. Lifetime predictions

Lifetime prediction models for solder interconnections under thermomechanical tests are usually classified into two major categories: strain based and energy based. Most models follow the Coffin-Manson type relation.

Strain based model: $$N_f = c_1(\varepsilon_{acr})^{-c_2} \quad (4)$$

Energy based model: $$N_f = c_3(W_{acr})^{-c_4} \quad (5)$$

where N_f is the characteristic life(time at which 63.2 % of the units will fail), ε_{acr} is the accumulated creep strain per cycle, W_{acr} is the accumulated inelastic strain energy density per cycle. c_1, c_2, c_3, and c_4 are model constants.

Another popular lifetime prediction model is the Darveaux's model [47], which is based on the crack growth correlation and the Anand constitutive model.

Crack initiation: $$N_0 = K_1 {W_{acr}}^{K_2} \quad (6)$$

Crack growth: $$\frac{da}{dN} = K_3 {W_{acr}}^{K_4} \quad (7)$$

Characteristic life: $$N_f = N_0 + \frac{a}{da/dN} \quad (8)$$

where N_0 is the number of cycles to crack initiation and $\frac{da}{dN}$ is the crack growth rate. K_1, K_2, K_3, and $K_4$are the correlation constants. a is the interconnection diameter at the interface (ultimate crack length).

According to the nature of the lifetime predictions, all the predictions are either relative or absolute. When one set of the measured lifetime for a specific package assembly is available, the relative predictions can be conducted in order to study the effects of various minor changes on the design, such as die size, mold compound thickness, and

PWB thickness. The accuracy of relative predictions is usually within the range of ±25 % or better. The accuracy of absolute lifetime predictions is somewhat less since absolute lifetime predictions cover a wide range of package designs, materials, and test conditions. In case the accuracy of the absolute lifetime prediction is not satisfactory, the following assumptions should be carefully checked: FE model, lifetime prediction model, material model, and material properties.

7. Summary of the Thesis

In this work, computer-aided numerical simulations were carried out in order to assess the reliability of solder interconnections in BGA packages. The finite element method was employed for the macroscale simulation while the Potts model based Monte Carlo method was adopted for the mesoscale microstructural simulation.

The major reliability tests for electronic component boards, i.e. thermal cycling, power cycling and drop impact tests, were simulated by employing the FEM. The work utilized stress-strain analyses to offer better understanding of the observed failure modes in the reliability tests. The lifetime predictions depending on the simulation results were greatly helpful for the lifetime estimations of the BGA packages.

A new algorithm was developed in order to predict dynamic recrystallization in solder interconnections during thermal cycling. The approach was realized by combining the Potts model based Monte Carlo method and the finite element method. The correlation between real time and MC simulation time was established with the help of the in situ test results. Recrystallization with the presence of the intermetallic particles in the solder matrix was simulated for the first time by introducing the energy amplification factors in the particle-affected deformation regions. The work provided insights into the recrystallization phenomenon in solder interconnections.

The thesis consists of six publications, of which the main results and conclusions are summarized as follows.

Publication I, entitled "**Reliability of Lead-Free solder interconnections in Thermal and Power cycling tests**", presented the thermomechanical reliability study of lead-free solder interconnections in thin fine pitch BGA packages. Finite element analyses were carried out to study the three reliability tests, i.e. thermal shock, local thermal cycling and power cycling tests. The calculated stresses, strains, and PWB expansions have

been compared among the three tests. The diagonal solder interconnections beneath the die edge were the most critical ones of all the tests studied. Darveaux's approach was used to predict the lifetime of the solder interconnections. The results showed that the thermal shock test would lead to the shortest fatigue life. With a similar temperature range, the power cycling test would have an absolute fatigue life 2.3 times longer than that of the thermal shock test, which makes the thermal cycling test a relatively conservative criterion for assessing package reliability.

Publication II, entitled "**Computational Assessment of the Effects of Temperature on Wafer-Level Component Boards in Drop Tests**", described the drop reliability of WL-CSP component boards used in portable devices. It has been found that the number of drops-to-failure increased significantly with increasing test temperature. At room temperature the cracks propagated solely along the intermetallic layers but the increase of test temperature progressively changed their propagation paths from the intermetallic layers into the bulk solder. The finite element method was employed to evaluate the complex temperature effects, which include the decrease of the strength and elastic modulus of solders, the decrease of the stiffness of printed wiring boards, and the introduction of the thermomechanical residual stress. The calculations showed that due to the increases in test temperature the peeling stress was reduced markedly, while the equivalent plastic strain was only slightly increased at the interfacial regions of the solder interconnections. The reduction of the stresses increased the proportion of the bulk solder cracking relative to the cracking of the intermetallic layers, and therefore the number of drops-to-failure increased as a function of increasing test temperature.

Publication III, entitled "**FEM simulations for reliability assessment of component boards drop tested at various temperatures**" presented the reliability study of four different component boards subjected to drop tests at different temperatures. The FEM based numerical experiments were designed to elucidate the temperature effects on the reliability. It has been found that the change of the component type from WL-CSP to other CSP-BGAs would result in a considerable increase in stresses and strains due to

the enlarged size of the components. The simulation results provided convincing explanations for the three failure modes distinguished by the fracture analyses.

Publication IV, entitled "**Multiscale Simulation of Microstructural Changes in Solder Interconnections during Thermal Cycling**" reported a new multiscale algorithm developed to predict the onset and progress of recrystallization in solder interconnections under thermal cycling tests. The algorithm consisted of a macroscale finite element method and a mesoscale Monte Carlo method. The theory was based on the accumulation of stored energy in solder interconnections during each thermal cycle and the competition between the recovery and recrystallization in consuming this energy. It was for the first time that dynamic recrystallization in solder interconnections was simulated. Verified by the experimental results, the presented algorithm predicted well the incubation period and the growth rate of the recrystallization.

Publication V, entitled "**Simulation of Dynamic Recrystallization in Solder Interconnections during Thermal Cycling**", presented a new algorithm, combining the Potts model based Monte Carlo and finite element methods, for predicting dynamic recrystallization of solder interconnections during in situ thermal cycling tests. A correlation between real time and MC simulation time was established for the time scaling process of the algorithm. Recrystallization with the presence of intermetallic particles was simulated by introducing the energy amplification factors in the particle-affected deformation regions. It was demonstrated that the algorithm predicted the dynamic recrystallization of solder interconnections, in a way consist with the experimental findings.

Publication VI, entitled "**Finite element analyses and lifetime predictions for SnAgCu solder interconnections in thermal shock tests**" reported the reliability study of SnAgCu solder interconnections under different thermal shock loading conditions. The stress-strain analysis was carried out to study the differences between different loading conditions. New crack growth data and correlation constants for the lifetime prediction model were reported. The simulation and experimental results indicate that

among all the loading conditions studied the thermal shock test with 14 min cycle time leads to the earliest failure of the BGA components.

In future work, the combined loading tests (e.g. thermal cycling & vibration, power cycling & shock impact) should be the focus of the reliability study of solder interconnections. It is a challenge to use simulation tools to assess the damage contribution from each single loading condition and the complex interactions between various loadings. Furthermore, the microstructural simulation approach can be utilized to develop an advanced crack simulation algorithm and finally lead to a novel lifetime prediction model with microstructural evolution considered.

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This work presents the results of computer-aided numerical simulations for the reliability assessment of lead-free solder interconnections in BGA packages. The major reliability tests for electronic component boards, i.e. thermal cycling, power cycling and drop impact tests, were simulated via the finite element method. The results provide a feasible tool for a better understanding of the observed failure modes in the reliability tests. In addition, a new algorithm was developed in order to predict dynamic recrystallization in solder interconnections during thermal cycling. The present algorithm predicted both the incubation period of the recrystallization as well as the growth tendency of the recrystallized regions in a way consistent with the experimental findings.

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