Department of Micro and Nanosciences

Iron gettering in silicon using doped layers and bulk defects

Heli Talvitie

Aalto University

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Iron gettering in silicon using doped layers and bulk defects

Heli Talvitie

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Abstract

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Abstract

The removal of iron impurities to desired regions in silicon wafers has been studied using phosphorus and boron doped layers and bulk defects as gettering sites. Techniques to remove metal impurities, so-called gettering techniques, are needed for improving the performance of both the microelectronic and photovoltaic silicon devices, although the desired location of impurities may be different in various applications. In this work, both separate and simultaneous influences of the doped layers and bulk defects on the gettering behaviour of iron, e.g. the gettering efficiency and gettering mechanisms, were investigated.

The phosphorus diffusion gettering studies at low temperatures enabled the determination of a more accurate segregation coefficient for iron between a phosphorus diffused layer and bulk silicon. Comparison between the phosphorus diffusion gettering experiments and similar experiments with boron showed that boron diffusion gettering can in some cases be nearly as effective as the phosphorus diffusion gettering.

The gettering studies with implanted boron layers revealed that the gettering occurs also by precipitation, not only by segregation. Competitive gettering between an implanted boron layer and bulk defects was investigated using specially designed gettering anneals. It was found that depending on the desired location of iron in silicon wafers in different applications, iron can be collected either to the doped layers or the bulk defects. The gettering anneals were also applied to a microelectronic device process and their effect on the electronic device parameters was evaluated.

These results contribute to the understanding of iron behaviour in silicon. Thus, they can help when designing the gettering anneals both for microelectronic and photovoltaic fabrication processes.

Keywords Silicon, iron, gettering, boron, phosphorus, bulk defects

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Tiivistelmä

Raudan getterointia eli raudan poistamista piikiekoissa halutuille alueille tutkittiin käyttäen fosforilla ja boorilla seostettuja kerroksia ja piikiekon kidevirheitä. Poistamalla metalliepäpuhtaudet piikiekoista voidaan parantaa sekä mikroelektroniikan että piiaurinkokennojen toimintaa. Eri sovelluksissa tosin epäpuhtaudet on poistettava eri alueille. Tässä työssä tutkittiin raudan käyttäytymistä, esimerkiksi getteroinnin tehokkuutta ja getterointimekanismeja, getteroitaessa rautaa seostettuihin kerroksiin ja piikiekon kidevirheisiin.

Raudan getterointia tutkittiin diffusoimalla fosforia ja booria matalissa lämpötiloissa. Tuloksista voitiin määrittää tarkempi arvio raudan segregaatiokertoimelle fosforilla seostetussa piissä. Vertailtaessa raudan getteroitumista fosforia ja booria diffusoimalla havaittiin, että boorin diffusointi voi joissakin tapauksissa olla lähes yhtä tehokas menetelmä getteroida rautaa kuin fosforin diffusointikin.

Raudan havaittiin getteroituvan boori-ioneilla istutettuun kerrokseen segregoitumisen lisäksi myös erkautumalla. Niin kutsuttua kilpailevaa getterointia istutetun boorikerroksen ja piikiekon kidevirheiden välillä tutkittiin käyttäen erityisiä lämpökäsittelyjä. Havaittiin, että riippuen raudan halutusta sijainnista piikiekossa rauta voidaan kerätä joko seostettuun kerrokseen tai kidevirheisiin. Samoja lämpökäsittelyjä käytettiin mikroelektroniikan komponenttien valmistusprosessissa ja niiden vaikutusta arvioitiin mittaamalla komponenttien sähköisiä parametreja.

Työssä saadut tulokset auttavat muodostamaan kokonaiskäsitystä raudan käyttäytymisestä piissä. Tuloksia voidaan käyttää suunniteltaessa getterointikäsittelyjä sekä mikroelektroniikan että piiaurinkokennojen valmistusprosesseihin.

Avainsanat Pii, rauta, getterointi, boori, fosfori, kidevirheet

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Preface

The research work for this doctoral dissertation was carried out in the Electron Physics Group in the Department of Micro and Nanosciences at the Aalto University School of Electrical Engineering (formerly Helsinki University of Technology). I wish to express my gratitude to my supervising professor, Professor Pekka Kuivalainen, for the opportunity to work in the group. The work was conducted under the supervision of Dr. Hele Savin. I am much obliged to her for her committed support and advice during the work.

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I wish to thank all my co-authors for their contribution and the pleasant collaboration. I am especially grateful to Dr. Antti Haarahiltunen for sharing his wide knowledge of iron gettering in silicon. Likewise, I would like to express my special thanks to Dr. Marko Yli-Koski for his indispensable advice on the experimental work, particularly the various measurement techniques. I wish to thank Dr. Atte Haapalinna and Dr. Jyrki Molarius for pre-examining this dissertation and Dr. Arve Holt for agreeing to be the opponent at the public examination of the dissertation. I would also like to thank Ms Charlotta Tuovinen for revising the language of this dissertation. Finally, I wish to express my gratitude to my co-workers in the Electron Physics Group and to all and everyone who have helped in various ways during this work.

Espoo, 6 October 2011

Heli Talvitie

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List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I H. Talvitie, V. Vähänissi, A. Haarahiltunen, M. Yli-Koski and H. Savin, Phosphorus and boron diffusion gettering of iron in monocrystalline silicon, Journal of Applied Physics, vol. 109, p. 093505, 2011.

II A. Haarahiltunen, H. Talvitie, H. Savin, M. Yli-Koski, M. I. Asghar and J. Sinkkonen, Modeling boron diffusion gettering of iron in silicon solar cells, Applied Physics Letters, vol. 92, p. 021902, 2008.

III A. Haarahiltunen, H. Talvitie, H. Savin, O. Anttila, M. Yli-Koski, M. I. Asghar and J. Sinkkonen, Gettering of iron in silicon by boron implantation, Journal of Materials Science: Materials in Electronics, vol. 19, pp. S41-S45, 2008.

IV H. Talvitie, M. Yli-Koski, A. Haarahiltunen, V. Vähänissi, M. I. Asghar and H. Savin, Experimental study of iron redistribution between bulk defects and boron doped layer in silicon wafers, physica status solidi (a), vol. 208, pp. 2430-2436, 2011.

V H. Talvitie, A. Haarahiltunen, H. Savin, M. Yli-Koski, M. I. Asghar and J. Sinkkonen, Effect of internal gettering of iron on electrical characteristics of devices, Materials Science and Engineering B, vol. 159-160, pp. 269-273, 2009.

VI H. Talvitie, A. Haarahiltunen, M. Yli-Koski, H. Savin and J. Sinkkonen, Effect of transition metals on oxygen precipitation in silicon, Journal of Physics: Conference Series, vol. 100, p. 072045, 2008.

Author's contribution

Publication I:	The author was actively involved in the planning of the experiments. The author fabricated and measured one of the two phosphorus diffusion sample series and one of the two boron diffusion sample series and participated in the fabrication and measurements of the other phosphorus diffusion sample series. The author also wrote the manuscript.
Publication II:	The author was actively involved in the design of the work and critically revised the manuscript.
Publication III:	The author was actively involved in the design of the work and critically revised the manuscript.
Publication IV:	The author was actively involved in the planning of the experiments, participated in the experimental work and wrote the manuscript.
Publication V:	The author was actively involved in the planning of the gettering experiments and the microelectronic device fabrication process, fabricated all the samples, analyzed the measurement results and wrote the manuscript.
Publication VI:	The author was responsible for the planning of the experiments, fabricated all the samples, carried out the measurements and wrote the manuscript.

List of Abbreviations and Symbols

BDG	Boron diffusion gettering
BMD	Bulk micro defects
BSF	Back surface field
CZ	Czochralski-grown silicon
DLTS	Deep level transient spectroscopy
Fe_{bulk}	Iron concentration in the bulk after gettering anneal
Fe_{init}	Initial iron concentration
FeB	Iron-boron pair
Fe_sP	Substitutional iron-phosphorus pair
FTIR	Fourier transform infrared spectroscopy
H_2O	Water
H_2O_2	Hydrogen peroxide
HCl	Hydrochloric acid
HF	Hydrofluoric acid
IC	Integrated circuit
IG	Internal gettering
k_{seg}	Iron segregation coefficient
MEMS	Micro-electro-mechanical systems
MOS	Metal-oxide-semiconductor structure
NH_4OH	Ammonium hydroxide
NMOS	Metal-oxide-semiconductor field-effect transistor with n-type channel
PDG	Phosphorus diffusion gettering
PMOS	Metal-oxide-semiconductor field-effect transistor with p-type channel
RT	Room temperature
SC1	Standard cleaning solution 1
SC2	Standard cleaning solution 2
SPV	Surface photovoltage
T_w	Wafer thickness
TEM	Transmission electron microscope
x_d	Depth of the diffused phosphorus layer

1 Introduction

Silicon technology has always suffered from the detrimental effect of iron and other transition metals on silicon device performance. Multicrystalline silicon contains high concentrations of iron but the presence of iron is difficult to avoid also in single crystalline silicon, as iron is a prevalent material in the silicon device processing environment. In order to reduce the harmful effect of iron, various means to remove iron, i.e. gettering techniques, have been developed. The purpose of gettering is to relocate iron in the silicon wafer to regions where it cannot deteriorate the silicon device performance. For example, iron gettering to highly doped layers or defects in the bulk of a silicon wafer have been studied both in silicon photovoltaics and microelectronics.

In silicon photovoltaics, the conventional gettering technique is phosphorus diffusion gettering. As the silicon solar cell comprises the whole wafer thickness, it is important to clear the solar cell bulk of impurities. Phosphorus diffusion gettering utilizes metal segregation to the highly doped regions in silicon. In the fabrication process of p-type silicon solar cell, which is the dominant solar cell type, the emitter formation by phosphorus diffusion simultaneously getters iron from the p-type bulk to the diffusing phosphorus layer. Phosphorus diffusion gettering is known to be effective, but the segregation coefficient of iron and the physical mechanism behind the increased iron solubility in the phosphorus diffused layer have remained unclear. Gettering by boron diffusion is usually considered to be less effective than the phosphorus diffusion gettering. Nevertheless, boron diffusion which is used to form emitter in n-type silicon solar cells, has attracted attention as the interest towards n-type silicon as a solar cell base material has increased due to e.g. its better tolerance to many metal impurities.[1]

In microelectronics, internal gettering i.e. iron precipitation to oxide precipitates and related defects in the bulk of a silicon wafer has been widely utilized. Microelectronic devices are fabricated to a very thin surface layer of the silicon wafer, which should be free of iron impurities. Iron present in the device layer can e.g. increase the pn-junction leakage current, deteriorating the device performance. The wafer bulk acts merely as a mechanical support and therefore the iron gettered to the bulk does not influence the device performance. However, iron can also accumulate to the device layer due to the segregation of iron to highly doped regions. Hence, there is a competition of iron between gettering to the highly doped regions and bulk defects.

The gettering processes are indeed often complicated, especially if several gettering mechanisms are involved. Thus, many widely exploited gettering techniques are inadequately known despite the vast amount of studies. In addition, introduction of new materials and the developments in device design may set requirements and limitations for iron gettering. The use of less pure, so-called solar grade or upgraded metallurgical grade silicon for low-cost solar cell fabrication demands effective gettering techniques.[2,3] Similarly, studies of gettering by boron and phosphorus doped layers are needed for the use of n-type silicon as a solar cell base material.[4,5,6] The results of iron gettering by dopant implantation are of interest also in photovoltaics as well as in microelectronics if solar cell emitter formation by implantation is introduced.[7,8,9,10] Furthermore, internal gettering has been proposed also for

improvement of multicrystalline silicon solar cells by precipitation of dissolved iron to the bulk defects, such as dislocations and grain boundaries.[11,12]

This work contributes to the understanding of iron gettering in silicon to highly doped regions and bulk defects. All the experiments in this work are carried out in single crystalline silicon, but many of the results are applicable also to multicrystalline silicon. Therefore, the gettering in multicrystalline silicon is also discussed in this work.

In Publication I, the experiments provide the missing steady state data of phosphorus diffusion gettering at low temperatures, from which a more accurate estimation for the iron segregation coefficient to a phosphorus doped layer can be determined. The phosphorus diffusion gettering results are compared to the corresponding boron diffusion gettering.

Iron gettering by high boron doping is studied also in Publications II to V. A model for boron diffusion gettering of iron is presented in Publication II. Iron gettering by an implanted boron layer is studied in Publication III. In Publication IV, iron gettering in the presence of both an implanted boron layer and bulk defects is investigated using various gettering anneals. These competitive gettering studies are continued by applying the same gettering anneals to a microelectronic device process. The results are presented in Publication V.

Finally, in Publication VI, bulk defect formation in metal contaminated CZ silicon wafers is studied. Oxide precipitates are known to getter iron but iron may also influence the oxygen precipitation. The purpose of the study is to find out if the metal impurities can increase the oxygen precipitation and thereby affect the internal gettering efficiency.

2 Background

2.1 Iron in silicon

The harmfulness of iron in silicon is due to the fact that it introduces deep energy levels into the forbidden band gap of silicon.[13] Through the deep levels, charge carriers can recombine reducing the minority charge carrier lifetime, or the charge carriers can be generated in depleted regions. Dissolved iron resides in silicon in interstitial lattice sites and is known to act as a strong recombination center. In p-type silicon iron forms pairs with the acceptor atoms at room temperature. In boron doped silicon, the iron-boron (FeB) pair acts as a strong recombination center as well. As the recombination activities of interstitial iron and iron-boron pair are different, the dissociation of the FeB pairs can be utilized in iron concentration measurements with recombination lifetime measurement techniques.[14,15]

In regard to gettering, diffusivity and solubility of iron in silicon are the important parameters. Iron has high diffusivity at high temperatures, which facilitates fast contamination even from a point source.[13,16,17,18] Iron diffuses interstitially, but the dependence of the iron diffusion coefficient on the charge state is not fully uncovered.

Due to a steep temperature dependence of the solubility, iron becomes supersaturated during cooling at temperatures where the diffusion is still fast.[13,17] As iron precipitates via a heterogeneous nucleation mechanism, i.e., there is a high barrier to iron-silicide nucleation and growth in a defect free silicon lattice, iron atoms can diffuse over long distances to precipitate at lattice defects during cooling.[16] For example, the iron precipitation at the silicon-silicon dioxide interface in metal-oxide-semiconductor (MOS) devices can cause an electrical breakdown.[16]

The solubility of iron increases in heavily doped silicon.[19,20] In boron doped silicon the increase is due to the Fermi level effect and the pairing of interstitial iron, which is positively charged in p-type silicon, with negatively charged substitutional boron. The total iron solubility in boron doped silicon can be expressed as the sum of neutral and positively charged interstitial iron and iron-boron pairs.[21]

In the case of phosphorus doped silicon, the increase of iron solubility is not as straightforward to explain. The interstitial iron in n-type silicon is in neutral charge state, which is why a pairing reaction with positively charged phosphorus is improbable. The physical mechanism causing the increase in iron solubility has not been discovered, despite the extensive studies.[18,22] Hence, the determination of the segregation coefficient of iron to the phosphorus doped silicon, which characterizes the gettering efficiency, has been challenging. The iron segregation coefficient is studied in Publication I.

2.2 Intentional iron contamination

In order to perform the gettering studies in a controlled way and to reliably determine the gettering efficiency, the initial iron concentration in the samples must be known accurately. All the iron gettering experiments presented in this work use intentionally iron contaminated wafers. Therefore, the iron contamination procedure which is used to produce a repeatable iron contamination level, first presented in Ref. 23, is described here.

In the contamination procedure used in this work, the iron is introduced onto the silicon wafer surfaces from a liquid source. Iron is subsequently diffused into the wafers with a high temperature anneal. The iron concentration diffused into the silicon wafer could be limited by the amount of surface contamination introduced from the liquid onto the wafer surface or by the diffusion temperature. Limiting the iron contamination level with the diffusion temperature has provided more repeatable results, which is why it has been used also in this work.

Before the contamination, the native oxide is removed from the wafer surfaces by dipping in a 50-1 parts by volume H_2O-HF solution. The wafers are then immersed for 10 min in a SC1 solution consisting of 5-1-1 parts by volume of H_2O-H_2O_2-NH_4OH and additionally 30 ppb of iron impurities. Iron is known to deposit form the alkaline SC1 solution onto the silicon surface.[24,25] Thus, a thin iron oxide layer is grown on the wafers in the contamination bath.

Iron is diffused into the silicon wafers at 850 °C which corresponds to an iron solubility of about 1×10^{13} cm^{-3}. The iron diffusivity at the in-diffusion temperature and the wafer thickness determine the time required to reach a homogeneous iron concentration at the iron solubility level, provided that the iron in-diffusion is not limited by the surface iron concentration. The in-diffusion time is chosen to be 55 min, which corresponds to an iron diffusion length of about 570 µm at 850 °C and is therefore sufficient to provide homogeneous iron distribution through the used silicon wafers. Also the lateral homogeneity of the contamination is good, as shown by an example in Figure 1. Before the in-diffusion anneal, the wafers are loaded into the furnace at 800 °C with a pulling rate of 25 cm/min, the temperature is stabilized for 10 min and then ramped up to 850 °C at a rate of 8 °C/min. After the iron in-diffusion, the wafers are unloaded to room temperature at a pulling rate of 25 cm/min. During all the steps, the composition of the gas atmosphere is 90 % nitrogen and 10 % oxygen.

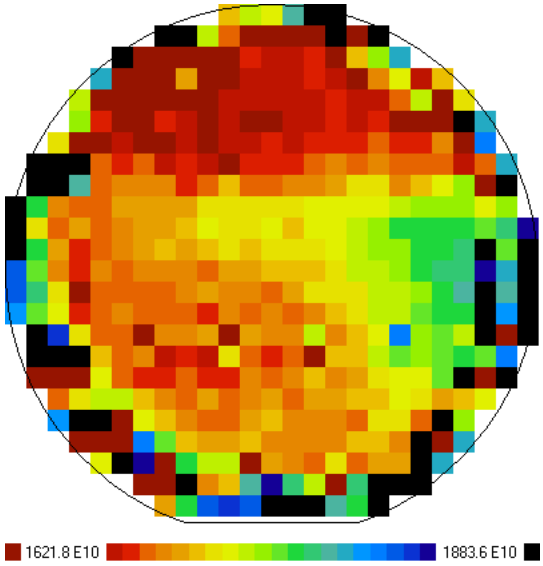

Figure 1. Iron concentration in an intentionally contaminated wafer determined with surface photovoltage (SPV) technique. The concentration unit is [cm^{-3}].

The surface contamination remaining after the iron in-diffusion is removed in 4.5 min in a 24-1-1 parts by volume H_2O-HF-H_2O_2 solution. Subsequently, the wafers are cleaned with standard cleaning procedure, i.e. 10 min in a SC1 solution consisting of 5-1-1 parts by volume of H_2O-H_2O_2-NH_4OH and then 10 min in a SC2 solution consisting of 5-1-1 parts by volume of H_2O-H_2O_2-HCl, followed by dip in a 50-1 H_2O-HF solution and thermal oxidation.

The cleaning of the wafer surfaces is critical in order to avoid additional contamination during high-temperature anneal. A failure in the surface cleaning may even lead to misinterpretation of the gettering results.

The cooling rate of the sample from high temperature is an important factor determining the state of the iron contamination after the contamination process. Quenching or moderately fast cooling results in iron remaining in interstitial sites. Slow cooling or a following anneal at a low temperature results in iron forming precipitates.[16] When the dissolved iron becomes supersaturated during cooling of the sample, iron tends to diffuse out of the sample and precipitate on the surfaces and in the bulk. However, a good quality oxide on the surface of the wafer can prevent the iron out-diffusion.[26]

3 Gettering using doped layers

3.1 Phosphorus diffusion gettering

Phosphorus diffusion gettering (PDG) is a widely used technique for the removal of iron contamination from silicon wafers by gettering to a diffusing phosphorus layer. PDG is used especially in silicon photovoltaics. Silicon solar cells are traditionally fabricated in p-type silicon wafers, in which the n-type emitter is made by phosphorus diffusion. Thus, the gettering step is inherently included in the solar cell fabrication process.

Gettering of iron to highly doped silicon regions is based on the segregation effect. The iron segregation to highly doped silicon arises from the increase of iron solubility with dopant concentration. The distinguishing feature of segregation gettering is that it can decrease the iron concentration below its solubility. Segregation gettering is an equilibrium process taking place at high temperatures, but the cooling rate also affects the segregation gettering efficiency as the segregation coefficient depends on temperature.[15]

Despite the intense investigation and utilization of PDG, the segregation coefficient of iron k_{seg}, defined as the ratio of iron solubility in the phosphorus doped layer to the solubility in the bulk silicon, has not been uncovered. For the determination of the segregation coefficient, PDG data also at low temperatures is needed. It has been found that at constant phosphorus content, the iron gettering efficiency of PDG in single crystalline silicon increases with the decrease of the phosphorus diffusion temperature.[27] The gettering efficiency of PDG in single crystalline silicon has also been observed to improve when the phosphorus diffusion is extended with a low-temperature step or a slow cooling.[28,29,30] Similar low-temperature PDG results have been obtained in multicrystalline silicon.[31,32,33] However, the amount of steady state PDG data from low temperatures has been rather limited. Therefore, PDG experiments carried out at low temperatures with a known iron contamination level and known phosphorus concentration profiles are necessary to determine a reliable segregation coefficient for iron between the phosphorus diffused layer and bulk silicon. Such studies are presented in Publication I.

Two phosphorus diffused wafer series with different phosphorus contents were prepared in intentionally iron contaminated wafers with iron concentration of 1.7×10^{13} cm^{-3} by varying the diffusion time at the phosphorus in-diffusion temperature of 870 °C. Phosphorus in-diffusion was followed by a low-temperature anneal in the temperature range of 650-800 °C. PDG results of the two wafer series with different phosphorus contents are presented in Figure 2. Iron concentration in the bulk after the PDG anneals with different low-temperature tails decreases with the tail temperature, as expected. The bulk iron concentration stays below the solid solubility of iron. Hence, the gettering is caused by a segregation type equilibrium effect, not by relaxation. The lower bulk iron concentrations in the series with lower sheet resistance could be due to the longer phosphorus in-diffusion time resulting in higher phosphorus content or the smaller wafer thickness, both of which decrease the steady state bulk iron

concentration. Because the wafer thicknesses, 525 µm in the series with high sheet resistance versus 400 µm in the series with low sheet resistance, cannot explain the iron concentration difference, it must be largely due to the difference in phosphorus content. The temperature dependence of the two wafer series is similar. The activation energies are 2.6 eV and 2.5 eV for the high and low sheet resistance series, respectively. They are close to the value obtained earlier for temperatures above 800 °C.[27]

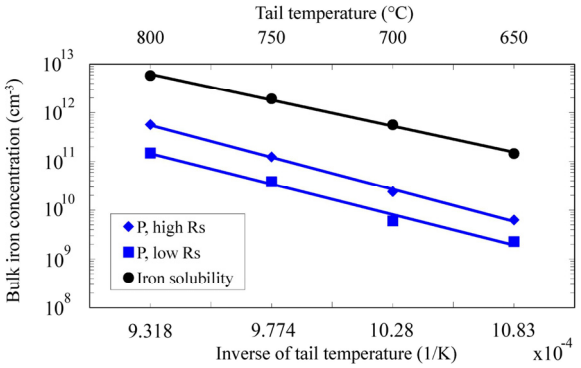

Figure 2. Bulk iron concentration after PDG with 30 min (P, high R_s) or 60 min (P, low R_s) phosphorus in-diffusion and a low-temperature anneal as a function of the temperature of the low-temperature anneal. Reprinted with permission from H. Talvitie, V. Vähänissi, A. Haarahiltunen, M. Yli-Koski and H. Savin, Journal of Applied Physics, vol. 109, p. 093505, 2011. Copyright 2011, American Institute of Physics.

The PDG results obtained in Publication I are used to determine the segregation coefficient of iron using a method presented in a previous study.[34] Like the phosphorus concentration, the segregation coefficient depends on the distance from the wafer surface. Assumptions of constant supersaturation, i.e. the relation between dissolved iron concentration and solid solubility of iron, and the conservation of mass, have led to the following equation[34]

$$\int_0^{x_d} k_{seg}(x)dx = x_d + \left(\frac{Fe_{init}}{Fe_{bulk}} - 1\right)T_w \qquad (1)$$

where Fe_{init} is the initial iron concentration, Fe_{bulk} is the iron concentration in the bulk after gettering anneal, T_w is the wafer thickness and x_d is the depth of the diffused phosphorus layer. With Eq. (1), the segregation coefficient can be fitted to the experimental data.

3.2 Boron diffusion gettering

Like in the case of high phosphorus doping, iron gettering to highly boron doped silicon regions is based on segregation. In boron doped silicon, the iron solubility is increased

due to the Fermi level effect and pairing of iron with boron. The iron segregation to highly boron doped regions can be seen e.g. in microelectronic applications when iron is collected from the moderately boron doped epitaxial layer to the highly boron doped substrate. Iron is accumulated also into diffused boron layers, such as the back surface field (BSF) layers in p-type silicon solar cells. In n-type silicon solar cells, boron diffusion is used for the emitter formation. Due to the advantages of n-type silicon compared to p-type silicon, such as better electrical transport properties, higher tolerance to iron and absence of light induced degradation, the n-type silicon has recently been considered as a possible candidate for solar cell base material. This has attracted the attention also to boron diffusion and its gettering capability.

Boron gettering has been studied in bifacial silicon solar cells with a boron diffused back surface field structure.[35,36,37] Boron diffusion followed by a low-temperature anneal was observed to increase the minority carrier lifetime.[35] However, in those studies iron was explained to be gettered into a thin surface layer instead of the boron doped p+ layer.[36,37] In order to optimize the boron diffusion from the gettering point of view, a model for boron diffusion gettering is seen as desirable. In Publication II such a model is presented, which includes both the iron segregation to the highly boron doped layer and iron precipitation to the wafer surface. Iron precipitation to the wafer surface is simulated using a model for heterogeneous precipitation of iron in silicon.[38,39] The boron diffusion gettering model takes into account the dependence of iron solubility on boron concentration and the dependence of iron diffusivity on trapping of positively charged iron by boron.

Simulations of the experimental boron diffusion gettering results from Ref. 37 with the proposed model are presented in Figure 3. The simulation parameters of the iron precipitation sites near the wafer surface are kept constant and therefore the differences in Figure 3 are caused by iron segregation to the boron doped layer. According to the simulations, the critical contamination level for nucleation and growth of iron precipitates to the wafer surface increases in the case of heavy boron doping because the solubility increases. As the boron doped p+ layer is very thin compared to the wafer thickness, the iron segregation to the p+ layer decreases the supersaturation in the wafer only very little. However, the nucleation and growth rates of iron precipitates are increased as the segregation increases the iron concentration in the thin p+ layer. The effect is much stronger than the supersaturation decrease. The simulations are also able to explain the time dependence of the experimental gettering results. Thus, the model is capable to explain the low-temperature boron gettering results, which cannot be explained by segregation alone.

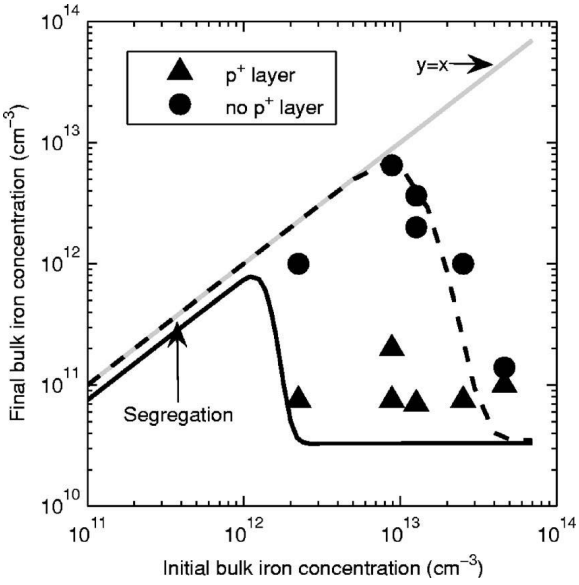

Figure 3. The final bulk iron concentration as a function of initial iron concentration after 2.25 h anneal at 600 °C. Triangles and circles are the experimental results from Ref. 37 with and without a boron doped p+ layer, respectively. Solid line and dashed line are the corresponding simulation results. The curve y=x is used as a reference to illustrate the effect of gettering. Reprinted with permission from A. Haarahiltunen, H. Talvitie, H. Savin, M. Yli-Koski, M. I. Asghar and J. Sinkkonen, Applied Physics Letters, vol. 92, p. 021902, 2008. Copyright 2008, American Institute of Physics.

The model also predicts that the optimal gettering temperature depends on the iron contamination level. At lower iron concentrations, the gettering can be improved by decreasing the gettering temperature as the segregation coefficient increases. However, at low temperatures the iron diffusion is slower and longer gettering times are needed in order to induce strong enough segregation and iron accumulation into the boron doped layer for iron to precipitate.

3.3 Comparison between phosphorus and boron diffusion gettering

The evaluation of n-type silicon as a solar cell base material involves the comparison of BDG efficiency to that of PDG. The low-temperature PDG experiments in Publication I are compared to earlier BDG experiments, where the same low-temperature anneals were applied to similarly iron contaminated wafers after boron in-diffusion at 930 °C resulting in a similar sheet resistance as the shorter phosphorus in-diffusion.[40] Previously BDG has been reported to be less effective than PDG.[21] However, the comparison presented in Figure 4 shows that PDG is only slightly more effective than BDG in the same material. In thinner wafers the BDG efficiency is even higher than the PDG efficiency.

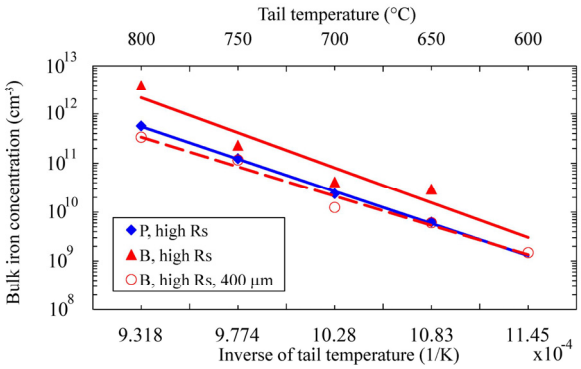

Figure 4. Bulk iron concentration after PDG (P, high R_s) and corresponding BDG in 525 µm thick wafers (B, high R_s) as a function of the temperature of the low-temperature anneal. BDG results of 400 µm thick wafers (B, high R_s, 400 µm) are also shown. Reprinted with permission from H. Talvitie, V. Vähänissi, A. Haarahiltunen, M. Yli-Koski and H. Savin, Journal of Applied Physics, vol. 109, p. 093505, 2011. Copyright 2011, American Institute of Physics.

The surprisingly high BDG efficiency has been explained by the chemisorption of iron by B-Si precipitates.[40] Some other studies have supported the observation that it is possible to achieve effective gettering by boron diffusion if the boron concentration is high. In a recent study, BDG has been shown to be ineffective at high temperatures, but the gettering efficiency was improved remarkably when the boron source vapour concentration was increased.[30] The improved gettering efficiency was explained by iron segregation to a boron rich layer. Simulations have also shown that iron precipitation in the boron layer during BDG or co-gettering by BDG and PDG can be advantageous over mere PDG in cases of high initial iron concentration, low phosphorus doping or short gettering time.[41]

From the low-temperature PDG and BDG results in Publication I and other recent results it can be concluded that effective PDG is fairly easy to achieve with a low-temperature anneal whereas effective BDG requires more accurately controlled gettering conditions. Either boron precipitation or iron precipitation during low-temperature anneal is required for effective gettering. Nevertheless, high boron concentration and a long anneal time are needed for iron gettering by B-Si precipitates, which may be disadvantageous in real solar cell fabrication processes. On the other hand, it has been proposed that BDG could be an effective gettering technique in n-type multicrystalline silicon as the high temperature of boron diffusion could release impurities, which BDG is then able to getter.[30]

3.4 Boron implantation gettering

Ion implantation instead of diffusion is commonly used in microelectronics to create heavily doped regions, as the implantation allows more accurate doping profiles. More recently, doping by implantation has aroused interest also in solar cell processes,[7,8,9,10]

due to e.g. the possibility for more accurate lateral dopant positioning in selective emitter applications. Similarly to a diffused layer, an implanted layer getters iron by segregation. The difference is that the implanted layer can getter iron also by precipitation at implantation induced defects or at precipitates formed by the implanted species.[15] Ion implantation can also be used to form gettering sites close to the microelectronic device regions,[42] which is of importance as the distance between the device region and gettering region becomes more critical in lower thermal budget processing.

Iron gettering to an implanted boron layer near the surface of a single crystalline silicon wafer is investigated in Publication III. The roles of the segregation and precipitation mechanisms in the gettering are studied. A similar model as the one used in Publication II is used in Publication III to explain the experimental results, this time including iron precipitation to the implantation induced defects and the segregation.

The wafers were intentionally iron contaminated to a level of about 2×10^{13} cm^{-3}. Two different boron implantations were carried out through a pad oxide. Also wafers without boron implantation were prepared. After the pad oxide removal, implantation activation at 1100 °C and oxidation at 1000 °C, the temperature was ramped down to the gettering temperature between 600 and 730 °C. The interstitial bulk iron concentrations after the gettering anneals were measured by surface photovoltage (SPV) technique.

The experimental gettering results of samples with boron implantation of 4×10^{15} cm^{-2} dose at 150 keV energy are shown by symbols in Figure 5. It is found that a much higher segregation coefficient than in a previous study in epitaxial wafers[26] would be needed to explain the experimental results. Reasonably good agreement between the experimental and the simulation results is achieved when the simulations include iron precipitation to the defects observed by transmission electron microscope (TEM) in the implanted boron layer. Even better agreement is achieved when also the effect of iron precipitate growth is taken into account in the simulation.

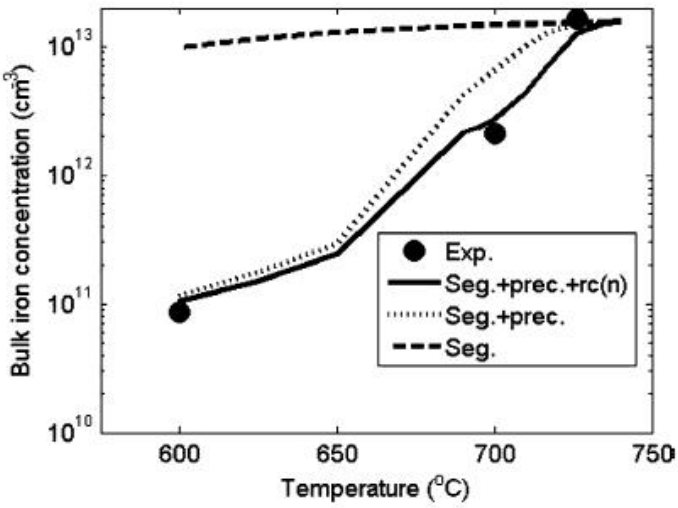

Figure 5. Experimental (spheres) and simulated (lines) results of iron gettering by boron implantation with a boron dose of 4×10^{15} cm^{-2} at 150 keV energy. A dashed line shows the simulation results that include only segregation. Solid and dotted lines include also iron precipitation to implantation damage and the solid line additionally includes the effect of iron precipitate growth. With kind permission from Springer Science+Business Media: Journal of Materials Science: Materials in Electronics, Gettering of iron in silicon by boron implantation, vol. 19, 2008, pp. S41-S45, A. Haarahiltunen, H. Talvitie, H. Savin, O. Anttila, M. Yli-Koski, M. I. Asghar and J. Sinkkonen, Figure 2.

The conclusion that iron precipitates to ion implantation induced defects is also supported by the observation that the gettering has steep temperature dependence, which is typical for precipitation. Also the final iron concentration is in agreement with the solubility value, which suggests that the gettering takes place by precipitation. In addition, similar results are also obtained with heavier boron implantation whereas in the wafers without boron implantation the iron contamination level is not changed after the gettering anneal.

4 Gettering using bulk defects

4.1 Internal gettering

Internal gettering (IG) usually refers to gettering by oxide precipitates and related crystal defects intentionally formed in the bulk of Czochralski-grown wafers (CZ silicon).[43] Internal gettering to these bulk micro defects (BMD) has been studied extensively as a means to improve the device performance in microelectronics (IC) industry, where CZ silicon is a commonly used substrate. Iron impurities can be diffused from the device layer near the wafer surface to the bulk, where they precipitate at the bulk defects. Thereby, the purification of the device layer will lead to better device performance and higher device yield.

Supersaturation of iron is needed before the internal gettering can take place. Typically, during cooling from high temperatures, the supersaturated impurities are diffused to the heterogeneous precipitation sites and precipitated there. In contrast to segregation gettering, internal gettering can decrease the iron concentration only to the solid solubility of iron.

In order for the internal gettering to occur, iron must be nucleated first at the bulk defects.[38,39,44] The iron precipitate nucleation, and thus also the gettering efficiency, can be enhanced by so-called low-high anneal.[45] The first step at a low temperature nucleates iron at the bulk defects. The second step at a higher temperature increases the iron accumulation into the bulk. Instead of the low-temperature anneal, a mere temperature ramp, e.g., to room temperature can nucleate iron sufficiently. The nucleation depends on the supersaturation level of iron, which is controlled by the iron contamination level and the processing temperatures.[39]

Internal gettering has recently been applied also to multicrystalline silicon in order to improve solar cell performance.[11,12] In solar cells the active device area extends through the wafer and therefore high bulk lifetime is desirable. The spatial and size distribution of metal defects in multicrystalline silicon has been found to have a direct impact on the minority carrier diffusion length, most metals, especially iron, being less deleterious in precipitated than in dissolved form.[46] Therefore, internal gettering of the dissolved iron in multicrystalline silicon to grain boundaries, dislocations and other crystal defects has the potential to improve the multicrystalline silicon material. However, the minority carrier lifetime is still limited by the metals remaining in the bulk after the gettering. In contrast, in the more traditional gettering techniques, such as phosphorus diffusion gettering, the higher bulk lifetimes have been strived for by removing the metal impurities from the bulk to e.g. the diffusing phosphorus layer.

4.2 Competitive gettering

Internal gettering to the bulk defects is complicated by the fact that most silicon devices contain highly doped regions, where the iron impurities tend to segregate. In such a

case, there is a competition of the metal impurities between the highly doped regions and the crystal defects. Theoretical studies on competitive gettering in integrated circuit device process have shown that iron can accumulate into the heavily doped device region but the accumulation could be reduced by adjusting the internal gettering parameters.[21] Internal gettering studies have usually been carried out studying e.g. the minority charge carrier lifetime in the gettering process. Fewer studies exist about the effect of gettering on the electrical device characteristics.[47,48,49,50,51]

4.2.1 Gettering between boron layer and bulk defects

In Publication III, the implanted boron layer was found to getter iron both by segregation and precipitation. It is followed by a study of the gettering behavior of iron in the presence of an implanted boron layer (p+ layer) and bulk defects, presented in Publication IV. The ability of various gettering anneals to minimize the iron accumulation into the p+ layer by precipitating iron to the bulk defects is investigated. The gettering anneals are based on the low-high anneal which increased the internal gettering efficiency in homogeneously doped wafers.[45] The low-temperature step is used to nucleate iron in the bulk, the high-temperature step to further grow the iron precipitates.

The gettering anneals were applied to boron doped CZ wafers with different denuded zone (DZ) widths and bulk defect densities. These various bulk defect profiles were obtained by different oxygen precipitation anneals. Samples with high bulk defect density were denoted with A or B, samples with low bulk defect density with C and samples without bulk defects with D. Then, the wafers were intentionally contaminated with iron to an iron level of 1.7×10^{13} cm^{-3}. A boron dose of 1×10^{15} cm^{-2} was implanted with 40 keV energy through the pad oxide on the front side of the wafers. The implantation parameters were chosen to be lower than in the implantation in Publication III to avoid the implantation induced defects and boron precipitation. Finally, the gettering anneals were applied to wafer sets consisting of wafers with different bulk defect profiles. The different gettering anneals and their notations are shown in Table 1. The total iron contents were determined in a 2.4 μm thick silicon layer from the front surface including the implanted boron layer (p+ layer). Iron concentrations in the bulk of some wafers were also measured.

Table 1. Gettering anneals and their notations.

Anneal notation	Gettering anneal
450	RT + 1 h at 450 °C
700-450	RT + 1 h at 700 °C + RT + 1 h at 450 °C
450-700	RT + 1 h at 450 °C + 1 h at 700 °C
270-700	RT + 1 h at 270 °C + RT + 1 h at 700 °C

The results in Figure 6(a) demonstrate that during the 450 anneal iron segregates sufficiently to the p+ layer for iron detection. However, the diffusion length of iron during the 450 anneal is too low for all the iron to be collected from the bulk. In the gettering anneal 700-450 (Figure 6(b)), the step at 700 °C increases the iron accumulation into the p+ layer compared to the gettering anneal 450. Nevertheless, in the samples with bulk defects (A-C) the accumulation is smaller compared to the sample without bulk defects (D). Also after the 450-700 gettering anneal (Figure 6(c)) iron is strongly accumulated into the p+ layer, which indicates that the step at 450 °C does not nucleate iron in the bulk. The results of the gettering anneal 270-700 (Figure 6(d)) prove that in samples with high bulk defect density (A samples), it is possible to reduce the iron accumulation into the p+ layer by gettering to bulk defects.

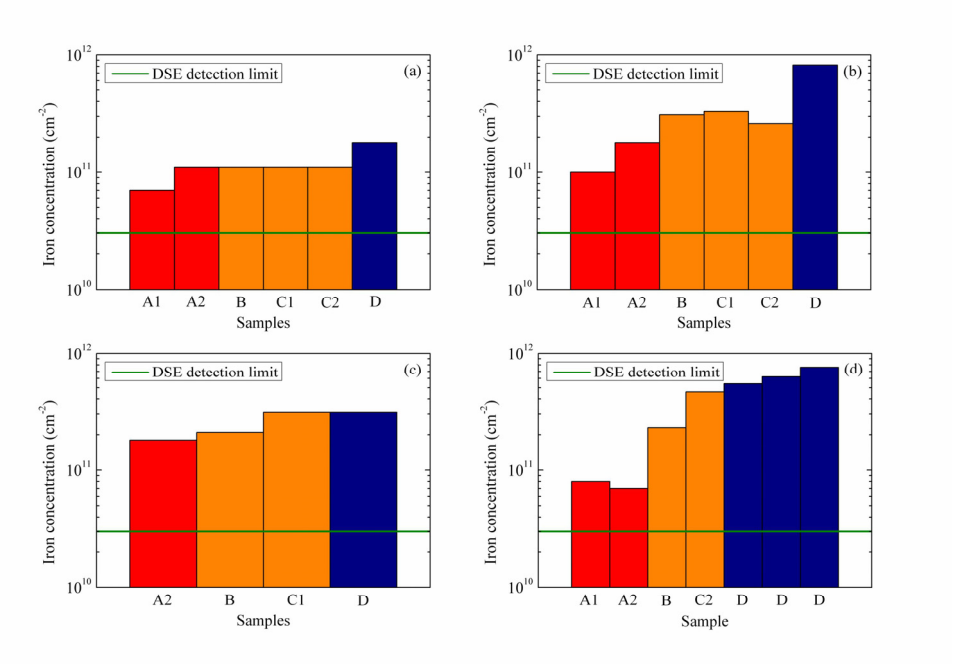

Figure 6. The total iron concentrations in the 2.4 µm etched layer including the p+ layer after the gettering anneals (a) 450, (b) 700-450, (c) 450-700 and (d) 270-700. Copyright 2011 Wiley. Used with permission from H. Talvitie, M. Yli-Koski, A. Haarahiltunen, V. Vähänissi, M. I. Asghar and H. Savin, Experimental study of iron redistribution between bulk defects and boron doped layer in silicon wafers, physica status solidi (a), vol. 208, pp. 2430-2436, 2011, Wiley-VCH Verlag GmbH & Co. KGaA.

The dissolved bulk iron concentrations were measured in some selected samples. The results are shown in Figure 7 along with the total iron concentrations in the p+ layer. The bulk iron concentrations are in agreement with the iron concentrations in the p+ layer: In the samples where the iron precipitation to the bulk defects decreased the total iron concentration in the p+ layer, it decreased also the dissolved iron concentration in the bulk.

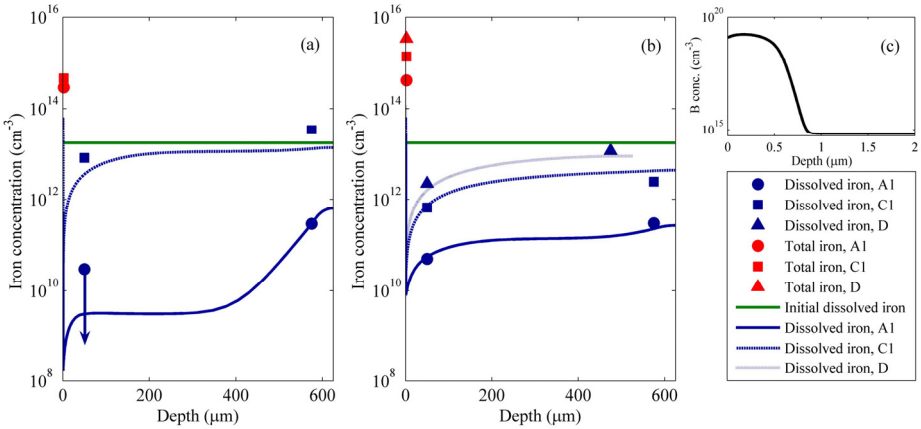

Figure 7. The dissolved iron concentrations in the bulk after the gettering anneals (a) 450 and (b) 700-450. Figure (c) shows the simulated boron concentration profile. Copyright 2011 Wiley. Used with permission from H. Talvitie, M. Yli-Koski, A. Haarahiltunen, V. Vähänissi, M. I. Asghar and H. Savin, Experimental study of iron redistribution between bulk defects and boron doped layer in silicon wafers, physica status solidi (a), vol. 208, pp. 2430-2436, 2011, Wiley-VCH Verlag GmbH & Co. KGaA.

The total iron concentrations in the p+ layers of A1 (high bulk defect density) and C1 (low bulk defect density) samples after the 450 anneal are about the same. However, in the C1 sample the dissolved iron concentration in the bulk is nearly the same as the initial value whereas in the A1 sample it is drastically decreased. Thereby, in the A1 sample the iron precipitation in the bulk was much faster than in the C1 sample.

A similar difference between dissolved bulk iron concentrations in A1 and C1 samples prevails also after the 700-450 anneal. The anneal at 700 °C decreased the dissolved bulk iron concentration to about 1×10^{12} cm^{-3}, but the anneal at 450 °C decreased it further only in the A1 sample. In the D sample (no bulk defects), the dissolved iron concentration is close to the initial value. The bulk iron concentrations suggest that iron has precipitated in the bulk defects even though the iron concentrations measured in the p+ layer did not immediately reveal it.

The total iron concentrations in the p+ layer are unexpectedly high after each gettering anneal. It indicates that iron has not accumulated into the p+ layer only by segregation but it has also precipitated in the p+ layer. This is surprising because the precipitation sites were not expected to exist in the p+ layer, neither in the form of implantation induced defects or B-Si precipitates. The iron precipitation in the p+ layer is supported by simulations in Publication IV, where the simulations that include the iron precipitation in the p+ layer are in agreement with the experimental results after 700-450 gettering anneal. In the 450-700 gettering anneal, the iron segregation to the p+ layer during the anneal at 450 °C induces higher nucleation rate in the p+ layer than in the bulk. The following anneal at 700 °C grows the iron precipitates in the p+ layer, which explains the strong iron accumulation into the p+ layer. The gettering anneal 270-700 reduces the iron accumulation into the p+ layer in the samples with high bulk

defect density (A samples). At the lower nucleation temperature at 270 °C the diffusion coefficient is decreased, which decreases the nucleation in the p+ layer even though the segregation is increased.

Based on these results presented in Publication IV it can be concluded that with appropriately selected gettering anneals and bulk defect profiles iron contamination can be directed either to the p+ layer or to the bulk. The selection of the nucleation and growth temperatures depends on the initial iron contamination level. If a low iron concentration in the doped layer is desired, which is the case in microelectronic applications, the nucleation temperature should be low enough and the bulk defect density high enough so that the nucleation of iron precipitates would be faster in the bulk than in the p+ layer. The growth temperature, on the other hand, should be high enough in order to avoid the iron segregation to the p+ layer but low enough in order to prevent iron precipitate dissolution in the bulk.

Iron gettering using high energy boron implantation has been studied earlier in float zone silicon.[52,53,54] The samples were annealed at 1000 °C after the boron implantation. In samples which were cooled fast after the annealing, iron was gettered to the boron implanted layer only from the nearby area, which was explained by segregation. In samples which received an extended anneal step at a lower temperature, almost all iron was collected to the boron implanted layer, which could only be explained by iron precipitation. Based on those studies and the results in Publication IV it can be stated that during a short anneal at low temperatures or a fast cooling, sufficient time has not elapsed for iron precipitates to nucleate. Therefore, iron accumulates into the p+ layer by diffusion and segregation. During an extended anneal, such as most of the anneals in Publication IV, iron precipitates are formed and diffusion and precipitate growth rate limit the iron accumulation into the p+ layer.

The samples in Publication IV resemble somewhat the multicrystalline silicon solar cell structure with a highly doped layer near the wafer surface and a high concentration of crystal defects in the wafer bulk. In multicrystalline silicon, a low-temperature anneal in the temperature range of 300-500 °C has been shown to induce an internal gettering to the crystal defects in regions of higher lifetimes.[12] The low-temperature anneal at around 500 °C following the phosphorus emitter diffusion has been shown to improve especially the crucible contaminated edges of multicrystalline solar cells.[55] On the other hand, the low-temperature anneal has been found to be effective when the phosphorus doped emitter is present but ineffective when the emitter is removed before the low-temperature anneal.[55] This suggests that the gettering caused by the low-temperature anneal is external gettering to a doped layer rather than internal gettering.[55] This is in agreement with the results in Publication IV, where the gettering to the doped layer dominated in most cases over the internal gettering.

4.2.2 Gettering in a microelectronic device process

The gettering anneals studied in Publication IV are applied in a microelectronic device process in Publication V. In Publication IV, certain gettering anneals were found to be able to reduce the strong accumulation of iron into the highly doped p+ layer and

instead, to precipitate iron in the bulk. In Publication V, it is studied how some of these gettering anneals affect the electrical characteristics of the devices.

The devices, simple NMOS and PMOS transistors and diode structures, were fabricated in p-type CZ silicon. The devices were fabricated both including a gettering anneal in the fabrication process and excluding the gettering anneal. Both the device process variations, i.e. with and without the gettering anneal, were applied to both intentionally iron contaminated and non-contaminated wafers. The iron concentration in the intentionally iron contaminated wafers was $1 - 2 \times 10^{13}$ cm^{-3}.

The device process is depicted in Figure 8. Thermal anneal steps for oxygen out-diffusion and oxide precipitate growth were inserted in the process. The first process step, implantation mask oxide growth for 50 min at 1050 °C for n-well implantation, was followed by a high-temperature anneal for 310 min at 1100 °C for oxygen out-diffusion, which created the denuded zone. An oxide precipitate nucleation anneal was inserted in the process when the gettering anneal was included later in the process. The purpose of this was to maximize the effect of the gettering anneal with respect to the process without gettering. The low-temperature oxide precipitate nucleation anneal for 360 min at 550 °C was included in the process before the implantation pad oxide growth step for 30 min at 1000 °C. The n-well was formed with phosphorus implantation 1×10^{13} cm^{-2} at 150 keV energy. The next annealing treatment included oxidation for 180 min at 1000 °C and a high-temperature anneal for 1080 min at 1100 °C, which served as phosphorus drive-in step and grew the oxide precipitates.

NMOS threshold voltage was adjusted with boron implantation of 2×10^{12} cm^{-2} dose with 30 keV energy. MOS transistor active area was formed with field oxide growth for 70 min at 1000 °C and patterning followed by implantation pad oxide growth for 30 min at 1000 °C. NMOS source and drain and PMOS substrate contact were formed by phosphorus implantation with 1×10^{15} cm^{-2} dose and 70 keV energy. PMOS source and drain and NMOS substrate contact were formed by boron implantation with 1×10^{15} cm^{-2} dose and 30 keV energy. Ion implantations were followed by doping activation anneal for 30 min at 950 °C and gate oxide growth for 55 min at 950 °C.

Iron gettered to the oxide precipitates can be dissolved with high temperature anneals.[56] Therefore, the oxidation and annealing steps of the device fabrication process have probably dissolved and gettered the iron in the wafers multiple times. Here the gettering anneal was inserted in the process after the last high-temperature anneal in which the iron solubility was higher than the iron contamination level, which in this device process was the gate oxide growth. After the gettering anneal, the process included contact opening formation, MOS gate and contact formation by aluminum sputtering and patterning and finally aluminum sintering for 15 min at 450 °C.

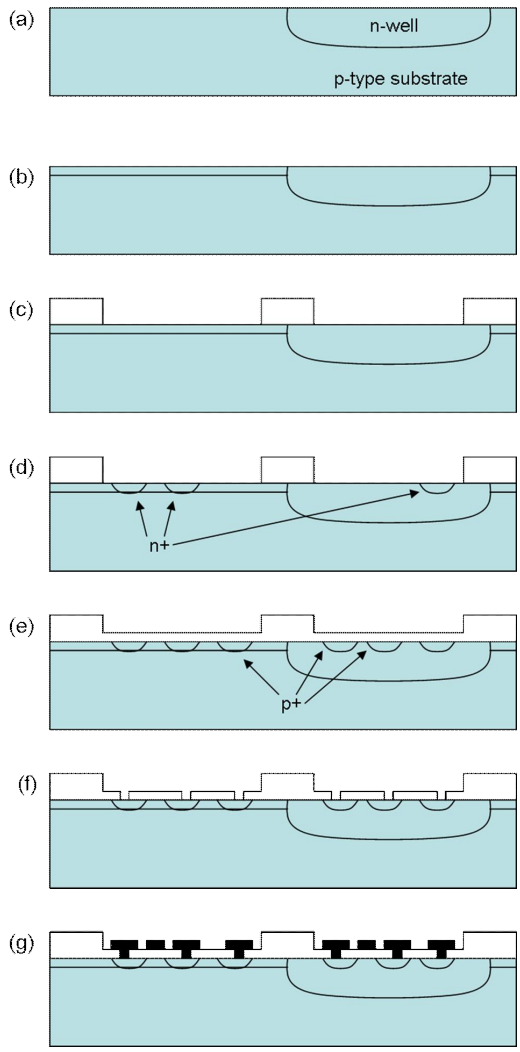

Figure 8. The device fabrication process. (a) n-well formation, (b) NMOS threshold voltage adjustment, (c) MOS transistor active area formation, (d) NMOS source and drain and PMOS substrate contact implantation, (e) PMOS source and drain and NMOS substrate contact implantation, (f) Contact opening formation, (g) Gate and contact formation. The figure is not to scale.

The effects of intentional iron contamination and gettering anneals on the devices were evaluated by measuring p^+n- and n^+p-junction leakage currents. Also some MOS transistor parameters were measured. In addition to the electrical device characteristics, iron concentrations in the device layer were studied with deep level transient spectroscopy (DLTS). Chips on different locations of wafers with and without gettering anneal 270-700, i.e. RT + 1 h at 270 °C + RT + 1 h at 700 °C, were measured.

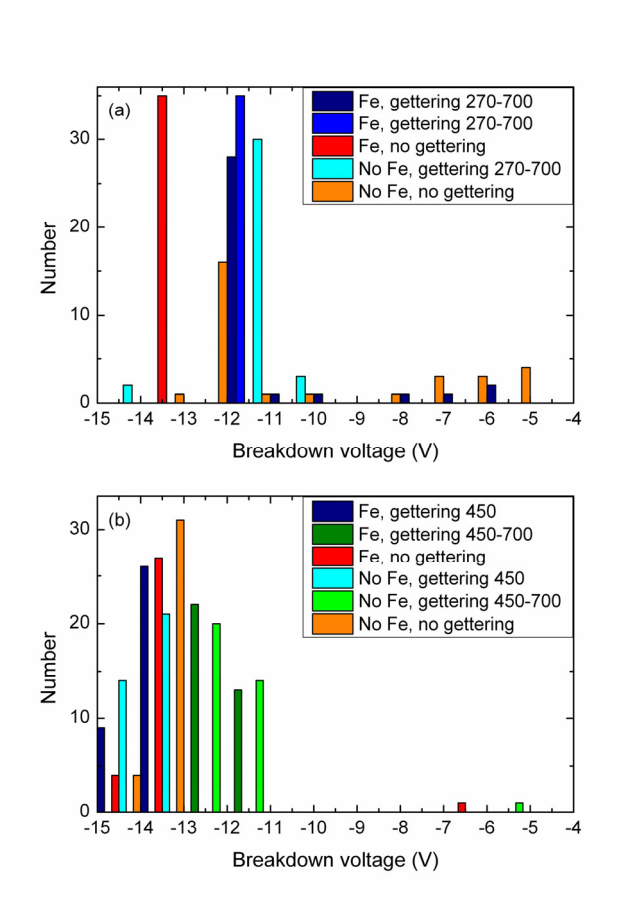

Figure 9. Distribution of breakdown voltages in PMOS transistors of 10 µm long and 50 µm wide channel after gettering anneal (a) RT + 1 h at 270 °C + RT + 1 h at 700 °C and (b) RT + 1 h at 450 °C or RT + 1 h at 450 °C + 1 h at 700 °C. Results for wafers without gettering anneal are also shown. Reprinted from Materials Science and Engineering B, vol. 159-160, H. Talvitie, A. Haarahiltunen, H. Savin, M. Yli-Koski, M. I. Asghar and J. Sinkkonen, Effect of internal gettering of iron on electrical characteristics of devices, pp. 269-273, Copyright 2009, with permission from Elsevier.

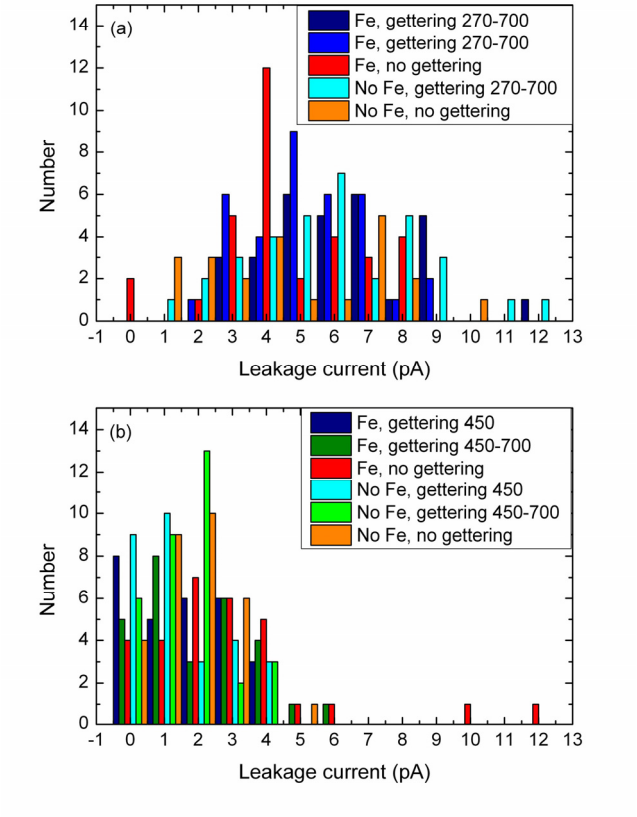

Figure 10. Distribution of p^+n-junction leakage currents in capacitors of 300 µm × 400 µm size after gettering anneal (a) RT + 1 h at 270 °C + RT + 1 h at 700 °C and (b) RT + 1 h at 450 °C or RT + 1 h at 450 °C + 1 h at 700 °C. Results for wafers without gettering anneal are also shown. Reprinted from Materials Science and Engineering B, vol. 159-160, H. Talvitie, A. Haarahiltunen, H. Savin, M. Yli-Koski, M. I. Asghar and J. Sinkkonen, Effect of internal gettering of iron on electrical characteristics of devices, pp. 269-273, Copyright 2009, with permission from Elsevier.

The device characteristics do not show a clear difference between the wafers with and without gettering, demonstrated by the distribution of PMOS breakdown voltages in Figure 9 and p^+n-junction leakage currents in Figure 10. However, the DLTS results in Figure 11 reveal a pronounced reduction in dissolved iron concentration in the device layer after the 270-700 gettering anneal compared to the samples without gettering.

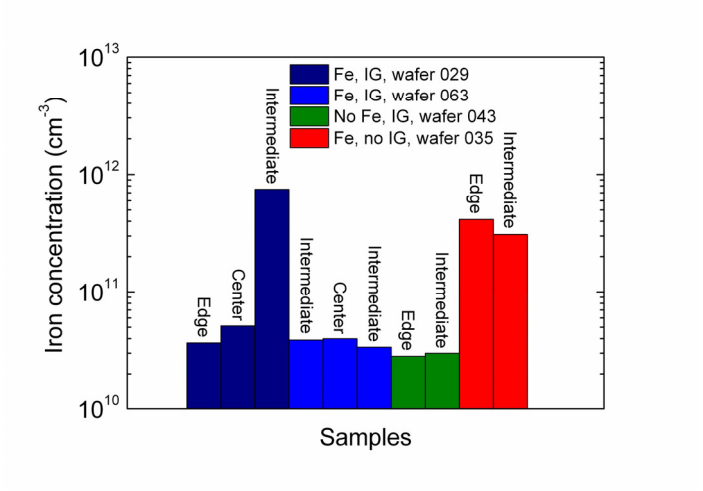

Figure 11. Iron concentration in the device layer after gettering anneal RT + 1 h at 270 °C + RT + 1 h at 700 °C. Location of the measured chip on the wafer (Edge, Intermediate or Center) is also indicated.

As discovered in Publication IV, the gettering anneal 270-700 was able to decrease the total iron concentration in the p+ layer by precipitation of iron to a high density of bulk defects. Despite the gettering to the bulk defects, the precipitation in the p+ layer during the 270-700 anneal could not be completely avoided. In Publication V, the bulk defect density created during the device process should be at least comparable to the one in Publication IV, based on the times and temperatures of the annealing steps. Nevertheless, the device layer most likely offers even more possible precipitation sites than the p+ layer, such as the implantation induced defects. Therefore, iron may have precipitated in the device layer. It has been stated that metal impurities are detrimental only when they agglomerate in relatively weakly doped regions, or form precipitates which penetrate through the boundaries between regions with different doping levels or at the gate oxide interface.[21] Thus, iron precipitation in the device layer might explain the inefficiency of the gettering anneals to improve the device performance even though the dissolved iron concentration in the device layer decreased during the gettering anneal.

In a microelectronic device process, iron gettering often occurs both by segregation and precipitation as both highly doped regions and precipitation sites in the device layer and in the bulk are present. Furthermore, the distance of the different devices to gettering sites and their sensitivity to iron contamination may vary. For example, iron segregation to heavily doped regions less sensitive to iron contamination can protect the lightly doped regions, although the gettering capability of the heavily doped regions may be limited by the small volume.[21] The variety of device structures and possible gettering sites makes the gettering in microelectronics a very complex process.

4.3 Effect of metal impurities on bulk defect formation

As described earlier, bulk defects e.g. oxide precipitates are known to offer gettering sites for metal impurities in silicon. However, it may not be the only interaction between the metal impurities and oxide precipitates. Studies have shown that iron contamination enhances oxygen precipitation in CZ silicon by accelerating the nucleation of oxygen precipitates.[57,58,59,60] On the other hand, the presence of iron has also been found to impede the oxygen precipitation.[61] Copper contamination was found to have no influence on the oxygen precipitation as copper and oxygen precipitate independently of each other.[59] In another study, copper precipitation was observed to enhance the oxygen precipitation.[62]

The influence of metal impurities on oxygen precipitation has, in turn, an impact on the internal gettering efficiency. For example, in Publication IV a high oxide precipitate density was needed to collect iron to the bulk. On the other hand, the increase in oxygen precipitation induced crystal defect density due to metal contamination would be detrimental in micro-electro-mechanical systems (MEMS). The harmful effect in MEMS is that the oxygen precipitation induced crystal defects deteriorate the quality of anisotropically etched cavity surfaces in silicon.[63] The impact of metal contamination on oxygen precipitation behavior is studied in Publication VI.

4.3.1 Effect of iron

The effect of iron on oxygen precipitation was studied in p-type CZ wafers. All the wafers were first annealed at 1050 °C. The purpose of this anneal was to reduce the effect of the wafer thermal history on the oxygen precipitation results by dissolving the as-grown oxide precipitates. Half of the wafers were then contaminated with iron to a level of 2×10^{13} cm^{-3}. Various thermal anneals, most of them two-step anneals, were applied to the contaminated and non-contaminated wafers to induce the oxygen precipitation. The temperature of the first step, i.e. the nucleation step, was varied whereas the temperature of the second step, i.e. the growth step, was always 1050 °C.

The amount of precipitated oxygen was calculated as the difference between the interstitial oxygen concentration before and after the sample preparation, measured by Fourier transform infrared spectroscopy (FTIR). Total defect densities and stacking fault densities were determined with defect revealing preferential etching from the samples with the highest amounts of precipitated oxygen.

The iron contamination does not increase the amount of precipitated oxygen in any of the applied anneals as seen from Figure 12. The only observable trend is the increase in the precipitated oxygen as a function of the initial oxygen concentration. In these wafers, the defect density is about 6×10^{5} cm^{-2}, both in iron contaminated and non-contaminated wafers. The iron contamination does not increase the stacking fault density, either.

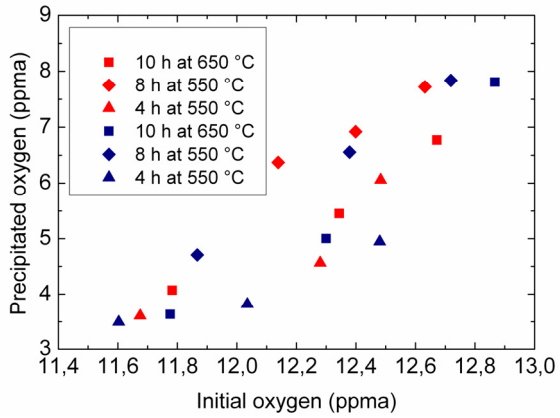

Figure 12. Precipitated oxygen in iron contaminated (red symbols) and non-contaminated (blue symbols) wafers. The nucleation anneals were as shown in the legend. The growth anneal was 10 h at 1050 °C. Copyright 2008 IOP Publishing Ltd. Reprinted from H. Talvitie, A. Haarahiltunen, M. Yli-Koski, H. Savin and J. Sinkkonen, Effect of transition metals on oxygen precipitation in silicon, Journal of Physics: Conference Series, vol. 100, p. 072045, 2008, with permission from IOP Publishing Ltd.

In previous studies it has been discovered that the presence of iron in Czochralski-grown silicon increases both the amount of precipitated oxygen and the oxide precipitate density.[57,58,59] It has been proposed that the iron atoms decorating the oxide precipitate nuclei stabilize them.[58]

The reason why iron contamination does not increase the oxygen precipitation as in most of the previous studies might be due to the low ramp-up rate chosen in our studies to promote the oxygen precipitation. The stabilizing effect of iron may then be masked by the high precipitation rate. On the other hand, in an experiment where the wafers were unloaded to room temperature after the nucleation anneal and loaded to the growth anneal at 800 °C, i.e. the ramp rates were fast, the oxygen precipitation was low also in the iron contaminated samples.

4.3.2 Effect of copper

Similar experiments on the effect of copper on oxygen precipitation were also carried out. The copper contamination level was about 6×10^{13} cm^{-3}. The wafers were illuminated to create copper precipitates before the two-step anneals for oxygen precipitation.

The results show again the increase in precipitated oxygen concentration when the initial oxygen concentration increases (Figure 13). This time there is also some evidence of increasing oxygen precipitation in copper contaminated samples after nucleation anneal for 6 h at 650 °C and growth anneal for 10 h at 1050 °C. In copper contaminated wafers the total defect density increases with the amount of precipitated oxygen.

However, further studies with different contamination levels would be needed to make definite conclusions about the effect of copper on oxygen precipitation.

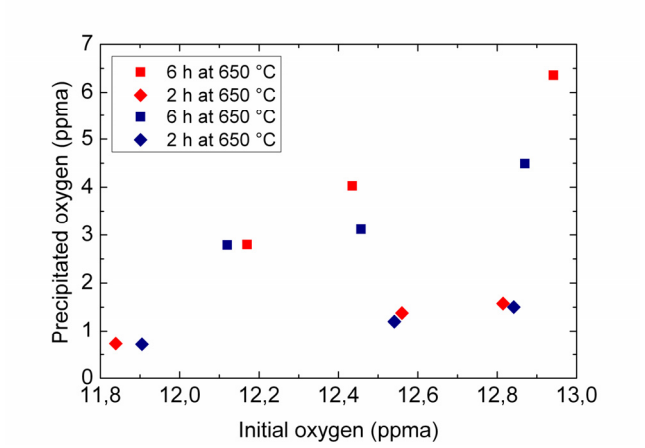

Figure 13. Precipitated oxygen in copper contaminated (red symbols) and non-contaminated (blue symbols) wafers. The nucleation anneals were as shown in the legend. The growth anneal was 10 h at 1050 °C. Copyright 2008 IOP Publishing Ltd. Reprinted from H. Talvitie, A. Haarahiltunen, M. Yli-Koski, H. Savin and J. Sinkkonen, Effect of transition metals on oxygen precipitation in silicon, Journal of Physics: Conference Series, vol. 100, p. 072045, 2008, with permission from IOP Publishing Ltd.

5 Conclusions

Gettering of iron impurities using phosphorus and boron doped silicon layers and bulk defects as gettering sites has been investigated. The metal impurity gettering is important both in microelectronics and photovoltaics as it can improve the silicon device performance. However, the desired location of the impurities in silicon wafers varies between the different applications. Thus, the understanding of iron behaviour in silicon and the control of the iron impurities are significant in order to reach the desired gettering result.

Phosphorus diffusion gettering data obtained at low temperatures enabled the determination of a more accurate segregation coefficient for iron between a phosphorus diffused layer and bulk silicon. The gettering efficiency of boron diffusion carried out with similar low-temperature anneals and comparable sheet resistance was observed to be surprisingly high compared to the phosphorus diffusion gettering results. Nevertheless, it was concluded that effective boron diffusion gettering requires more tightly controlled gettering conditions than the phosphorus diffusion gettering.

Boron implantation gettering studies showed that iron is not gettered to the boron layer only by segregation but it has also precipitated there. Studies of competitive gettering between an implanted boron layer and bulk defects revealed that with an appropriate gettering anneal iron can be collected either to the doped layer or bulk defects, depending on the desired location of iron.

Gettering anneals were applied also to a microelectronic device process and their effect on the electrical device characteristics was evaluated. The experiments showed that the gettering anneal had reduced the dissolved iron concentration in the device layer, but it had no clear impact on the device characteristics. This was explained by iron precipitation in the device layer.

Finally, the possible influence of iron and copper on bulk defect formation was investigated. Iron was not found to influence the amount of precipitated oxygen or the defect density at the studied iron contamination level. On the other hand, copper contaminated samples showed some indication of enhanced oxygen precipitation.

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Errata

Publication II: The growth and dissolution rates of iron precipitates in the thin heavily doped boron layer are multiplied by the product of the iron segregation coefficient k_{seg}(B) and the effective diffusion constant of iron D(B) normalized to the bulk diffusion constant.

Publication III: The growth and dissolution rates of iron precipitates in the thin heavily doped boron layer are multiplied by the product of the iron segregation coefficient k_{seg}(B) and the effective diffusion constant of iron D(B) normalized to the bulk diffusion constant.

Publication V: The first processing step in Table 1 should be: Ion implantation mask oxide growth for 50 min at 1050 °C to 435 nm thickness and high temperature annealing for oxygen outdiffusion for 310 min at 1100 °C

The sixth processing step in Table 1 should be: Oxidation for 180 min at 1000 °C and high temperature annealing for phosphorus drive-in and oxide precipitate growth for 1080 min at 1100 °C

The ninth processing step in Table 1 should be: Field oxide growth for 70 min at 1000 °C to 380 nm thickness

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