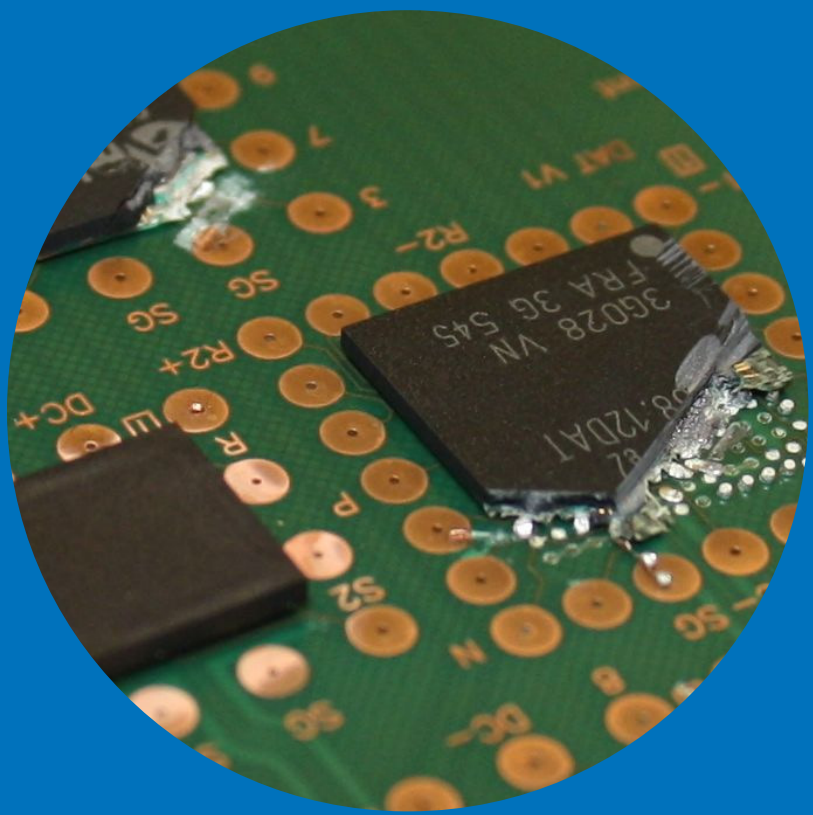
Department of Electronics

# Reliability assessment of electronic assemblies under multiple interacting loading conditions

Juha Karppinen

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# Reliability assessment of electronic assemblies under multiple interacting loading conditions

**Juha Karppinen**

A doctoral dissertation completed for the degree of Doctor of Science (Technology) to be defended, with the permission of the Aalto University School of Electrical Engineering, at a public examination held at the lecture hall S1 of the school on 14th of February 2013 at 12 o'clock.

**Aalto University**
**School of Electrical Engineering**
**Department of Electronics**
**Unit of Electronics Integration and Reliability**

**Supervising professor**
Prof. Mervi Paulasto-Kröckel

**Thesis advisors**
Prof. Tomi Laurila
Docent Toni Mattila

**Preliminary examiners**
Dr. Pascal Oberndorff, Philips Lighting, Eindhoven, The Netherlands
Dr. Olaf Wittler, Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany

**Opponents**
Dr. Pascal Oberndorff, Philips Lighting, Eindhoven, The Netherlands
Dr. Changqing Liu, Loughborough University, The United Kingdom

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# Abstract

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**Abstract**

This dissertation presents the results of multiple experimental and computational reliability assessment methods employed on electronic assemblies. It is demonstrated that the typical standardized test procedures often fail to capture the complex loading conditions of service environment and can lead to artificial results due to excessive damage acceleration. An alternative reliability assessment approach based on the use of combined loading tests derived from product service loading characterization is proposed as a solution to the problem. In this proposed approach special attention is paid to establishing a stronger correlation between the material-scientific reliability analyses and lifetime prediction methods.

Several methods on how to predict and characterize the reliability of component assemblies under different use cases and field environments are presented. Particular emphasis is placed on the reliability of board-level solder interconnections due to their complex and often unsatisfactory reliability behavior. It is shown that multiple microstructural mechanisms, such as dispersion strengthening, grain growth, strain rate hardening, fatigue and recrystallization, contribute together to the reliability performance of interconnections. The presented relationships between these mechanisms and the affecting loading conditions enable more accurate and comprehensive assessment of electronic product reliability.

**Keywords** Combined load testing, electronic assembly, solder interconnection, mechanical load, electrical load, thermal load, thermal cycling

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**Tiivistelmä**

Tässä väitöstyössä esitellään tulokset useiden eri kokeellisten ja laskennallisten luotettavuuden arviointimenetelmien sovellutuksista elektronisiin kokoonpanoihin. Tulokset osoittavat että perinteiset standardisoidut testimenetelmät eivät useinkaan anna oikeaa kuvaa nykyaikaisten tuotteiden monimutkaisien käyttöympäristöjen aiheuttamista kuormituksista, ja ne voivat johtaa karkeisiin arviointivirheisiin testeissä käytettyjen liiallisten kiihdytystekijöiden vuoksi. Ongelman ratkaisemiseksi tässä työssä esitellään vaihtoehtoinen yhdistelmätestaukseen perustuva luotettavuuden arviointimenetelmä, jossa tuotteiden todelliset käytönaikaiset rasitukset on huomioitu aiempaa todenmukaisemmin. Ehdotetussa menetelmässä kiinnitetään erityistä huomiota vahvempien riippuvuussiteiden luomiseksi materiaaliteknisten luotettavuusanalyysien ja laskennallisten elinikämallinnusten välille.

Esitelty luotettavuuden arviointimenetelmä sisältää useampia koetapoja, joiden avulla voidaan karakterisoida ja ennustaa piirilevykokoonpanojen luotettavuutta erilaisissa käyttöympäristöissä. Uuden menetelmän kehityksessä on kiinnitetty erityisesti huomiota piirilevytason juoteliitoksien luotettavuuteen, sillä näiden liitosten käyttäytyminen erilaisten rasitustilojen alaisuudessa on monimutkaista ja ne muodostavat kokoonpanoissa usein luotettavuusriskin. Työssä havainnollistetaan miten useat mikrorakenteelliset mekanismit, kuten erkautumislujittuminen, rakeenkasvu, muodonmuutosnopeuslujittuminen, väsyminen ja uudelleenkiteytyminen, vaikuttavat yhtäaikaisesti juoteliitosten kykyyn kestää rasituksia. Havaintojen pohjalta esitettyjen mikrorakenteellisten mekanismien ja vaikuttavien kuormitustekijöiden välisten vuorovaikutussuhteiden ymmärtäminen mahdollistaa kokonaisvaltaisemman ja tarkemman luotettavuusanalyysin toteuttamisen elektroniikkatuotteille.

**Avainsanat** Yhdistelmärasitustestaus, juoteliitos, elektroninen kokoonpano, mekaaninen kuormitus, sähköinen kuormitus, lämpökuormitus

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# Preface

This work has been conducted in the Electronics Integration and Reliability unit under the Department of Electronics at Aalto University. The work was financially supported by two projects, 'CRT' and 'Electromigration', which were funded by the Finnish Funding Agency for Technology and Innovation (TEKES), Academy of Finland, Nokia, Nokia Siemens Networks, Efore Plc, NXP Semiconductors, Salon Teknopaja Oy and the National Semiconductor Corporation.

I am grateful to my supervisor Professor Mervi Paulasto-Kröckel, and my previous supervisor Professor Jorma Kivilahti. Without their advice, encouragement and support, this dissertation would not have been possible.

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Finally, I would like to present my loving thanks to my family for their endless love and patience. My parents also deserve special thanks for providing unfaltering encouragement and support throughout my life.

Espoo, 2013

Juha Karppinen

# Contents

# List of Publications

This thesis consists of an overview of the following publications, which are referred to in the text by their Roman numerals.

I Laurila, T., Karppinen, J., Vuorinen, V., Li, J., Paul, A. and Paulasto-Kröckel, M.; "Effect of Isothermal Aging and Electromigration on the Microstructural Evolution of Solder Interconnections During Thermomechanical Loading", *Journal of Electronic Materials*, Vol. 41 (11), pp. 3179-3195, Springer, 2012

II Laurila, T., Karppinen, J., Li, J., Vuorinen, V. and Paulasto-Kröckel, M.; "Effect of isothermal annealing and electromigration pre-treatments on the reliability of solder interconnections under vibration loading*", Journal of Materials Science: Materials in Electronics*, in print, Springer 2012.

III Karppinen, J., Li, J. and Paulasto-Kröckel, M.; "The effects of concurrent power and vibration loads on the reliability of board-level interconnections in power electronic assemblies", *Transactions on Device and Materials Reliability,* in print, IEEE, 2012.

IV Karppinen, J., Laurila, T., Mattila, T.T. and Paulasto-Kröckel, M.; "The Combined Effect of Shock Impacts and Operational Power Cycles on the Reliability of Handheld Device Component Board Interconnections", *Journal of Electronic Materials*, Vol. 41 (11), pp. 3232-3246, Springer, 2012

V Karppinen, J., Li, J., Mattila, T.T. and Paulasto-Kröckel, M.; "Thermomechanical reliability characterization of a handheld product in accelerated tests and use environment", *Microelectronics Reliability*, Vol. 50 (12), pp.1994-2000, Elsevier 2010.

VI Karppinen, J., Li, J., Pakarinen, J., Mattila, T.T. and Paulasto-Kröckel, M.; “Shock impact reliability characterization of a handheld product in accelerated tests and use environment”, *Microelectronics Reliability*, Vol. 52 (1), pp. 190-198, Elsevier, 2012.

# Author's contribution

Publications I & II:

The author participated in the planning of the research, the failure analyses, interpretation of the results and preparation of the manuscripts. The author also conducted all of the experimental work with help from several research assistants. The main part of the manuscripts, and in particular the material scientific discussion, were written by Dr. Tomi Laurila.

Publications III-VI:

The research program was planned and the theoretical aspects were discussed by the author with the co-authors. The experimental work was planned by the author and conducted by the author with help from several research assistants. The author also carried out the statistical analyses, failure analyses and theoretical explanations of the results. The author wrote the manuscripts, which were then discussed in detail with the co-authors. The finite element modeling work in all publications was conducted by co-author Dr. Jue Li.

# List of Abbreviations and Symbols

| | |
|---|---|
| AC | alternating current |
| AF | acceleration factor |
| ATC | accelerated thermal cycling |
| BT | bismaleimide triazine |
| CFD | computational fluid dynamics |
| CTE | coefficient of thermal expansion |
| DC | direct current |
| EU | european union |
| FE | finite element |
| FEA | finite element analysis |
| FEM | finite element method |
| FR-4 | fiberglass-reinforced epoxy resin, flame retardant |
| HALT | highly accelerated life test |
| HCF | high cycle fatigue |
| HTS | high temperature storage |
| IC | integrated circuit |
| IDSA | incremental damage superposition |
| I/O | input / output |
| IEC | International Electrotechnical Commission |
| IMC | intermetallic compound |
| JEDEC | Joint Electron Device Engineering Council |
| LCF | low cycle fatigue |
| LDSA | linear damage superposition |
| min | minute or minutes |
| MTBF | mean time between failures |
| OPC | operational power cycling |
| PBGA | plastic ball grid array |
| PoF | physics of failure |
| PWB | printed wiring board |

| | |
|---|---|
| RT | room temperature (22°C / 295.15 K) |
| SnAgCu | tin silver copper solder alloy |
| TDM | topography and deformation measurement |
| UBM | underbump metallurgy |
| Wt-% | weight percentage |

| | |
|---|---|
| $a$ | crack path length |
| $b$ | fatigue strength exponent |
| $C$ | life prediction model constant |
| $c$ | life prediction model constant |
| $c_o$ | life prediction model constant |
| $c_1$ | life prediction model constant |
| $c_2$ | life prediction model constant |
| $c_3$ | life prediction model constant |
| $c_4$ | life prediction model constant |
| $D$ | damage |
| $E$ | Young's modulus |
| $E_a$ | activation energy |
| $\varepsilon_c$ | creep strain |
| $\varepsilon_f'$ | fatigue ductility coefficient |
| $\varepsilon_e$ | elastic strain |
| $\varepsilon_p$ | plastic strain |
| $\varepsilon_t$ | total strain |
| $G$ | gravitational acceleration constant of earth (9.81 m/s²) |
| $k$ | Boltzmann constant ($1.3806503 \times 10^{-23}$ m² kg/ (s² K )) |
| $K$ | correlation constant |
| m | life prediction model constant |
| $N_f$ | cycles to failure |
| $N_o$ | cycles to crack initiation |
| $R$ | process rate |
| $s_f'$ | fatigue strength coefficient |
| $T$ | absolute temperature |
| $t$ | time |
| $W$ | viscoplastic strain energy per cycle |

# 1 Introduction

Reliability is an important factor to success in the highly competitive global electronics market. Customer dissatisfaction can have disastrous financial consequences to the manufacturer: While it takes companies a long time to build up a reputation for reliability, a single problematic key product can ruin this reputation almost overnight. Besides financial issues, failure due to insufficient reliability can lead to life threatening situations in critical fields such as medical devices and avionic electronics. It is clear that in these applications reliability should be of highest priority to avoid the catastrophic consequences of failure.

In addition to challenges in maintaining good reliability, the electronic product designers are constantly striving to meet the customer demands for new features and improved performance in a smaller size. Higher operating speeds require shorter interconnection distances to minimize propagation delays and new features require higher integration in component packaging. As a consequence, the assembly sizes, inputs/output (I/O) pitches and line widths in integrated circuits (ICs) as well as printed wiring boards (PWBs) are constantly decreasing. In order to provide assurance that new designs and products fulfill their reliability target, a large number of different reliability tests are employed. However, due to today's tight time-to-market requirements and shortening product cycles, the amount of required tests should be minimized.

The reliability testing of electronics has been traditionally carried out with accelerated reliability tests, where the tested units encounter loads more frequently than in service or are subjected to higher levels of accelerating variables like temperature or voltage. These tests can currently be grouped under two categories: traditional reliability tests, in which only one loading type is used, and combined tests, in which two or more different loading types are combined. Today, the vast majority of accelerated tests are still conducted as single load tests, because the interaction effects of various combined loads are not understood well enough. [Lau12, Upa01] Multiple load tests, however, offer many potential advantages when employed

properly. As modern products are required to withstand numerous loads without failure for many years, it is increasingly difficult to obtain sufficient amount of reliability data within a reasonable amount of time. Multiparameter tests have the potential to provide the means for overcoming this difficulty. In addition to expediting the whole product testing process by replacing multiple tests, it is shown that a single multiparameter test can also create a substantially more accurate representation of the loading conditions in actual use-environment [Upa01].

The focus of this dissertation is on the development of a realistic and efficient multiparameter reliability approach for different electronic product applications. This approach is demonstrated with studies of different loading condition combinations on the damage evolution in solder interconnections in Publications I, II, III and IV. The studied loading conditions include various combinations of mechanical, thermal, thermomechanical and electrical loads. In addition to simplified board-level tests, the true loading conditions encountered in one challenging product application, the consumer handheld device, are studied in detail with product-level test characterizations in Publications IV, V and VI. These characterizations are used to assess the limits of test acceleration under board level testing. Finally, suggestions on improvements to contemporary reliability assessment methods are given based on the results obtained from the dissertation publications. Although the results of the conducted research are primarily centered on interconnection reliability, the general methodology can be applied on any electronic structure.

The dissertation is organized as follows. A brief introduction to reliability challenges in electronic products is given in Section 2. An efficient reliability design process and evaluation methods are presented in Section 3. Lifetime estimation methods for electronic assemblies are addressed in Section 4 and special considerations as well as the key material properties for reliability assessment of lead-free solder interconnections are discussed in Section 5. Finally, Section 6 gives the summary of the work including the main results and conclusions of the included publications.

# 2 Background on reliability challenges

The typical reliability trend of an electronic product population through its intended lifetime is generally divided to three consecutive time periods:

1. Infant mortality period is characterized by an initial high failure rate, which is generally caused by poor quality control in manufacturing. These initial failures are especially harmful to manufacturer reputation, which may lead to loss of sales in addition to costs associated with product warranty work.

2. Once the part of population containing early design and manufacturing has failed, the remaining population typically enters a time period of relatively constant and low failure rate. This period is described as the useful life of the product, which should meet the expectations of the market for service life of such product type. The failures during useful life are random cases of environmental or operational stresses exceeding the product strength.

3. After the useful life period the product enters the wear-out period. The wear-out period is characterized by an increasing failure rate due to the fatigue or depletion of the structures and used materials. The failure of the product should be ”graceful”. This means that the failure should preferably be predictable (e.g. early warning of wear-out from internal self-diagnostics) and that the failure should not cause injury or damage to other attached or adjacent devices.

The failures in electronic assemblies are caused by electrical, thermal, mechanical and chemical stresses occurring during service. These stresses

may originate from the external environment (for example, electrostatic discharges, ambient temperature changes and accidental product drop impacts) or be produced internally by the device itself (for example high current densities, electric power dissipation and mismatches in material thermal expansion). A brief overview of typical thermal, mechanical and electrical loads and their reliability effects are given in this section. Chemical stresses, however, are not within the scope of this dissertation.

Failures in electronic products can be classified to hard or soft failures, depending on whether the product regains its functionality after the failure-inducing stresses are removed. Soft failures are typically caused by operating the product outside the manufacturer specified environmental conditions (temperature, humidity, etc.) range. In these cases the product has usually not sustained permanent damage and becomes operational once the environmental conditions have returned to within the manufacturer's specifications. Hard failures, on the other hand, are caused by irreversible physical damage to the product. In these cases the product remains faulty until the damaged parts have been replaced or reworked. The emphasis of the research conducted in this dissertation is on hard product failures.

Hard product failures can be further categorized into two types based on severity of the imposed loading conditions:

1. Overstress failure: In the simplest case the failure occurs when the stress level exceeds the strength of the product. Examples of threshold strengths are the tensile strength of a material or the temperature level at which an electronic component begins to malfunction. Overstress failures are generally caused by either too harsh product use environmental (user error) or latent manufacturing and design defects in the product.

2. Fatigue failure: Some failures occur under cumulative effects of repeated low-level stressing. Each stress cycle causes irreversible changes in the product, which ultimately cumulate to result in product failure. An example of phenomenon leading to cumulative stress failure is the fatigue failure of interconnections under mechanical bending or vibration loading. Cumulative stresses

generally define the useful life of the product in the specified use environment.

The failure type induced under true field conditions, however, is usually a combination of cumulative and overstress failure. A high peak-stress may initiate an incipient failure that later results in a hard failure due to lower cumulative stressing. Also, low cumulative stresses may substantially reduce the strength of the product to withstand subsequent overstress conditions.

## 2.1 Thermal loading

The vast majority of electronic components can easily meet their reliability targets when operating at or near room temperature. In practice, many integrated circuits operate at substantially higher temperatures and undergo various thermal excursions depending on the operating profile of their use conditions. Temperature can be considered the most fundamental factor affecting the reliability of all electronics. Typical operating temperature ranges for several electronic device categories reported in [IPC92, Vis04, Hat99, Edd98] are given in Table 1.

**Table 1 –Typical operational temperature ranges for different electronic product types (excludes specialized sensors, which may encounter substantially higher temperatures).**

| Application | Electronics internal operating temperature range | Ambient environment temperature range |
|---|---|---|
| Military | -55 °C to 125 °C [Vis04] | -55 to 95 °C [Vis04] |
| Automotive | -40 °C to 150 °C [Hat99, Edd98] | -40 °C to 125 °C [Hat99, Edd98] |
| Industrial & telecom equipment | -40 °C to 125 °C [IPC92] | -40 °C to 85 °C [IPC92] |
| Consumer | 0 to 100 °C [IPC92] | 0 to 60 °C [IPC92] |

Temperature influences device reliability both directly and indirectly via other failure mechanisms. Temperature directly affects both the mechanical properties (such as elastic modulus, ultimate tensile strength, yield strength, and ductility) as well as electrical properties (such as resistivity and capacitance) of materials. The changes in electrical properties typically

cause soft product failures as the operational parameters of individual components or circuits drift beyond specifications. The changes in mechanical properties, on the other hand, may lead to hard product failures. For example, high temperature can lead to softening, weakening or melting of materials and device malfunctioning, while low temperatures can result in embrittlement of plastics, condensation and freezing of condensation or coolants. Furthermore, solid-state diffusion and chemical reactions are accelerated by increasing temperature. These physical processes may permanently change the mechanical properties of the materials used in electronic assemblies. This is particularly true with low melting temperature materials, which may undergo significant time-dependent microstructural changes when exposed to high temperatures [Dom11, Jeo04, Pen07]. The reliability effects of microstructural changes in solder interconnections due to thermal loads are explored in Publications I-V.

In addition to the direct effects of temperature discussed above, major reliability concerns arise from indirect mechanical stresses caused by changing temperature. Due to geometric constraints and mismatches in the coefficient of thermal expansion (CTE) between materials, so-called thermomechanical stresses are concentrated in various parts of electronic assemblies. With repeated thermal excursions these parts experience cyclic mechanical loading, which may ultimately lead to fatigue failure. Interconnection areas in particular are vulnerable to thermomechanical damage. [Lau07, Ham00, Mat04, Zha05]. The lifetime and failure mode of as-manufactured and preconditioned solder interconnections under thermomechanical loading are addressed in publications I, III, IV and V.

Some reliability effects of high temperatures on electronic assemblies encountered within the research of this dissertation [Publications I- VI] are given in Table 2.

**Table 2 - Some effects of high temperature ( < 125 °C) on parts of electronic assemblies [Publications I- VI].**

| Structure / material | Effect on material(s) | Effect on reliability |
|---|---|---|
| PWB / fiberglass reinforced epoxy resin | Notable thermal expansion | Internal thermomechanical stress between materials |
| | Change of tensile properties | Loss of mechanical support |
| Interconnections / solder | Increased material diffusion and microstructural change | Increased electro- and thermomigration, reduction of strength and load-carrying ability |
| | Change of tensile properties | Reduction of strength and load-carrying ability |
| Component packages | Notable thermal expansion | Internal thermomechanical stress, warpage and delamination |
| | Change of tensile properties | Loss of mechanical support |
| Functional parts of components | Changes in electrical properties | Unreliable operation |
| | Increased material diffusion | Increased electro- and thermomigration |

## 2.2 Mechanical loading

Mechanical loads are becoming an ever more important part of electronics reliability engineering due to the increasing amount of integrated circuitry employed in mobile applications. Mechanical loadings typically cause damage to board-level interconnections, component leads and connectors within component assemblies due to the straining of printed wiring boards, inertial forces and knocking of adjacent parts [Won05, Sea06, Var07, Mar07]. High strains may cause instantaneous overstress failures as the mechanical strength of a component or subassembly is locally exceeded, whereas repeated low amplitude bending can lead to fatigue failure. Different mechanical loads are typically divided into the three basic categories: (1) static or quasi-static mechanical bending, (2) vibration and (3) shock impact loads. These load types, the typical applications they affect, their main failure drivers and typical failure modes are given in Table 3.

**Table 3 – Common mechanical loads encountered by electronic products.**

| Load type | Applications affected | Typical failure drivers in component assembly | Failure modes in component assemblies |
|---|---|---|---|
| Shock impact | - Portable devices<br>- Automotive<br>- Some devices during transit | - Inertial loads caused by high acceleration<br>- Overstress caused by assembly bending<br>- Knocking of adjacent parts | - Interconnection / component lead overstress failure<br>- Connector detachment |
| Vibration | - Automotive<br>- Aerospace<br>- Marine<br>- Work machinery<br>- Most devices during transit | - Fatigue damage caused by cyclic bending of assembly<br>- Knocking of adjacent parts | - Interconnection / component lead fatigue failure<br>- Connector detachment |
| Static or quasi-static bending | - Portable devices | - Overstress caused by assembly bending | - Interconnection / component lead overstress failure<br>- Connector detachment |

Static or quasi-static mechanical stresses can be imposed on the printed wiring board when the whole product is bent, or for example in a situation when connector or keypad pressings directly load the device PWB. The most common destructive mechanical loads for electronic products, however, are dynamic vibration and shock impact loads.

Vibration loading can, for example, be readily found in mission-critical applications within the automotive, aerospace, marine, and heavy work machine industries. Furthermore, many products intended for stationary use endure vibrations during the logistic chain from the manufacturing line to the end user. Portable electronics, on the other hand, are susceptible to be dropped during service, which creates substantial high-strain shock loads on the product assembly [Publication VI]. Both shock and vibration loads can also excite the natural vibration modes of product PWBs [Publication VI, Won05, Sea06, Var07, Mar07,], which lead to overstress and/or fatigue failure (depending on the duration and amplitude of PWB vibration) of electrical interconnects and detaching of connectors.

The reliability effects of mechanical shock loads on the interconnections of a handheld device component boards are studied in publications IV and VI. The left part of the Figure 1 demonstrates the acceleration and strain

histories of a mobile phone PWB after a product-level drop impact from 1.2m height (see publication II for details). The effects of mechanical vibration loads on board-level interconnections are presented in publications II and III. The right part of Figure 1 shows an example of a printed wiring board excited to its first natural vibration mode by an electrodynamic shaker.

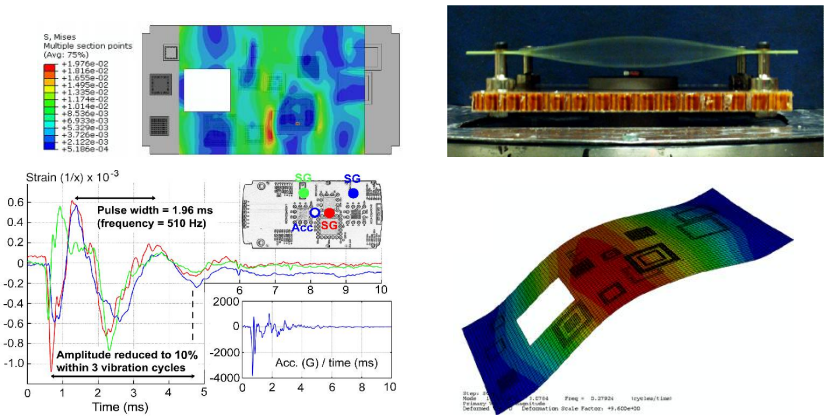


**Figure 1 – Left: Acceleration and strain histories measured from a handheld device PWB under product-level drop (see Publication II for details). Right: Bending of the device PWB under vibration loading.**

## 2.3 Electrical loading

Miniaturization of electronics has led to rapid increase of current densities in conductors and interconnections, exposing these structures to electromigration. Electromigration is a process in which the conductor material is transported due to two driving forces: (1) the momentum transfer between conducting electrons and diffusing metal ions and (2) the direct force exerted to the metal ions by the electric field. The typical current density at which electromigration effects become notable is about $10^6$ A/cm$^2$ in aluminium and copper conductors. [Ho89,Tu03] As electromigration depends on material diffusion, the temperature of the stressed conductor has a large effect on the rate of the process. Typical current densities encountered in different parts of electronic assemblies are given in Table 4 along with their known reliability effects.

**Table 4 - Typical current densities required for onset of electromigration.**

| Structure | Material | Current density | Effect of electro-migration | Effect on reliability |
|---|---|---|---|---|
| IC metallization | Copper | $> 10^6$ A/cm$^2$ [Ho89, Tu03] | Hillock and void formation | Formation of short or open circuits |
| | Aluminium / Al-Cu | | | |
| Intercon-nection | Tin-based solder | $> 10^4$ A/cm$^2$ [Tu03] | | |
| | | $> 10^3$ A/cm$^2$ [Tu03, Lau11, Publications I & II] | - Biasing of interfacial intermetallic growth<br>- Changes in solder microstructure | Embrittlement of interconnection interfaces |

Electromigration has been successfully reduced in the aluminium conductors of integrated circuits by employing bamboo structures and Cu-alloying [Ho89, Tu03]. However, new concerns are rising on the effects of electromigration within low melting temperature solder alloys. As is shown in publications I and II, electromigration becomes detectable in solder interconnections already at a current density of only about $10^3$ A/cm$^2$. Above this value electromigration causes nonuniform formation of intermetallic compounds between anode and cathode side of the interconnection. When the current density is increased to about $10^4$ A/cm$^2$ the effect of the electron flux becomes powerful enough to cause substantial material transport in interconnections [Tu03, Che10]. Unlike thin film conductors inside integrated circuits, the microstructure of solder interconnections cannot be controlled by manufacturing processes to combat the electromigration problem.

Most problematic areas for electromigration are abrupt changes in conductor geometry and interfaces of dissimilar conductor materials. Sharp changes in conductor geometry and resistivity lead to current crowding, in which the local current density may become orders of magnitude higher than the estimated average current density [Tu03,Che10]. Due to current crowding problems electromigration is rapidly becoming a reliability concern in contemporary electronic assemblies. Figure 2 shows the effects of electromigration on a solder interconnection and illustrates the problem of current crowding.

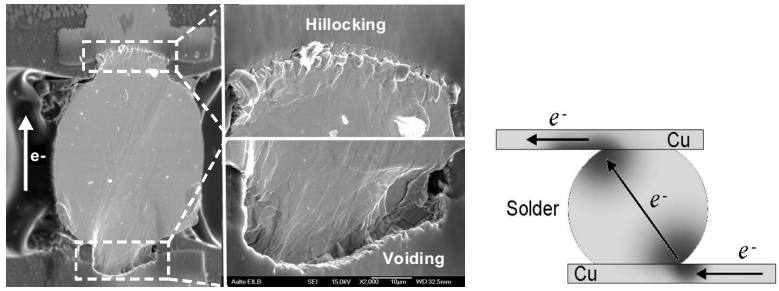


**Figure 2 – Left: SEM image of a solder interconnection exposed to $3x10^4$ A/cm² current density for 26 days. Right: Illustration of current crowding in a flip-chip solder interconnection due to geometry and interfaces of dissimilar materials.**

## 2.4 Single load – multiple stress conditions

Electronic products are seldom exposed only to a single type of stress, even if only a single loading condition is imposed on the product. A ubiquitous example of a single load causing multiple stresses is electrical power loading. When electrical current is driven through the circuitry, not only are conductors and components exposed to electromigration stress, but also to increased temperature due to resistive losses. This not only increases the local temperature of the assembly, but the resulting thermal gradients cause thermomechanical stresses between dissimilar materials. Thus, applying electrical power load to an electronic assembly generates simultaneously electrical, thermal and mechanical stresses.

Since all electronic devices dissipate heat due to electrical losses to some extent, the above-mentioned combination of electrical, thermal and mechanical stresses is unavoidable. However, the severity of these stresses depends on the design of the product. In a well-designed product these stresses are kept at a low enough level to not cause reliability concerns during the designed service life. Therefore, it is of paramount importance to consider and aim to mitigate these loads as early in the product design as possible. The formation and effect of thermomechanical stresses on a commercial handheld electronic product and power electronic test assemblies are investigated in Publications I, III, IV and V of the dissertation. Figure 3 below shows the thermomechanical stress and strain induced in a solder interconnection inside a mobile phone under power loading (see [Kar08] and Publication V for details of the experiment).

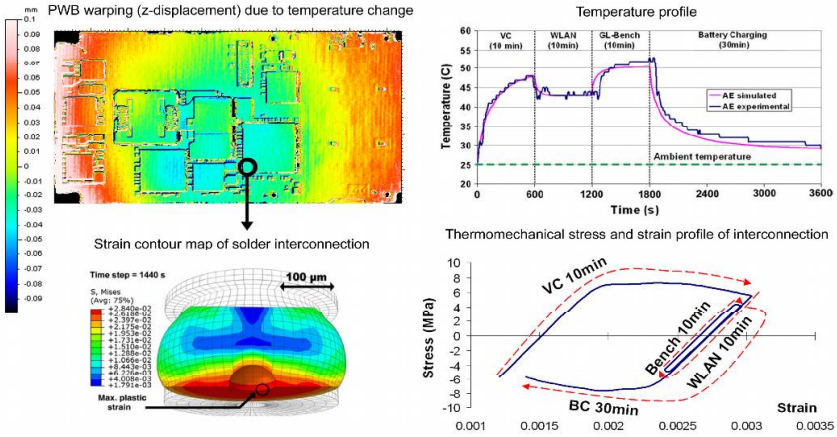


**Figure 3 - Thermomechanical stress in an interconnection due to operational power dissipation (see [Kar08] and publication I for details).**

# 3 The assembly-level reliability design process

Due to the wide range of modern electronic products, it is impossible to define a universal test method that would prove the reliability of each product in their own use environment. Therefore, the reliability design process should begin with investigations on the reliability requirements of the specific product application. The product application will typically define the service environment, lifetime, and design requirements [Mil338, Cha01].

While it is compulsory to test an electronic product in its final form to verify the fulfillment of reliability and safety requirements, it is also highly desirable to conduct reliability evaluations throughout the design cycle. Early evaluations on prototype designs can substantially expedite the detection of potential reliability problems and allow cost-effective solutions to improve the design [Mil338, Cha01]. In general, it is preferable to start reliability evaluations with the smallest testable units of a product and then progressively proceed to testing of larger systems. The early reliability evaluations can be conducted with statistical block diagram analyses, simplified prototype experiments or by employing computational methods, such as the finite element method (FEM).

The challenge in reliability assessment of smaller subassemblies is in the definition of realistic loading conditions: as the final product enclosure and fixtures may not be available, estimations on their effects to the tested unit's reliability will have to be made [Cha01, Mil338]. Conducting mechanical and thermal characterizations on similar product designs or dummy structures can refine these estimations. As an example, mechanical and thermal characterizations of a mobile phone have been conducted in [Kar08] and [Kar10]. The results of these characterizations are

subsequently utilized in Publications V and VI to estimate the reliability of the device. Figure 4 illustrates the advantages and challenges in performing reliability assessments between smaller and more complete test vehicles [Cha01].

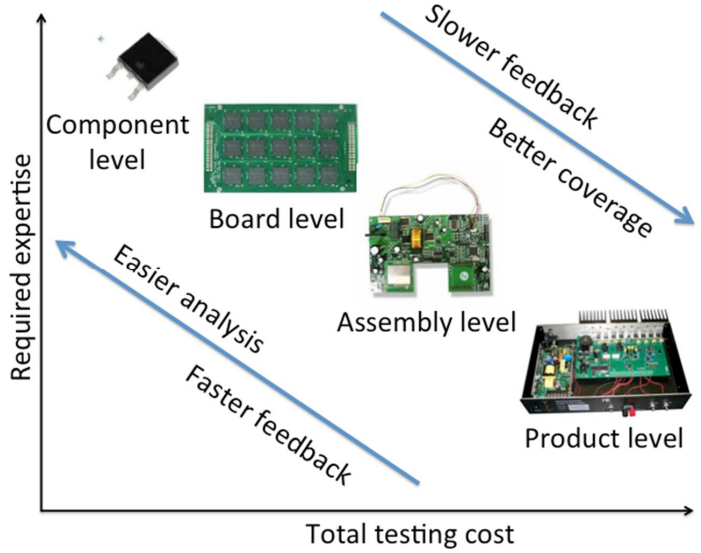


**Figure 4 –Advantages and challenges of focused and more comprehensive test vehicles (adapted from [Cha01]).**

Once the suitable loading conditions and fixturing have been determined, the response of the tested assembly to the defined loading conditions are investigated. The typical responses to be investigated are (1) detection of potential stress- and strain concentrations on the assembly, (2) detection of temperature levels and possible temperature gradients under operating conditions, (3) detection of high current densities and voltage levels and (4) assessment of materials and structures vulnerable to humidity or corrosion. These investigations help to pinpoint the most critical locations in the assembly, which may limit the reliability of the final product.

The preliminary evaluation of the assembly response to loading conditions can be followed by a more in-depth study focusing on the found critical design points. In this stage a more detailed FE-analysis (FEA) or experimental reliability test on a representative test structure is conducted to investigate whether the found critical loads form a reliability threat to the final product. For best results, this focused reliability evaluation should be

based on good understanding of the underlying physical failure mechanisms acting on the critical parts of the assembly [Lau12]. Examples of such studies on component-level test vehicles are presented in Publications I-IV of this dissertation. If the design fails the reliability evaluation, improvements need to be made to rectify the problem. Afterwards the reliability evaluation should be redone to verify that the reliability problem has been solved [Cha01, Mil338].

Once the initially weak design features in the individual subassemblies have been corrected, the first production-grade prototype batch of the complete product can be manufactured. This prototype batch is used to verify the fulfillment of the set reliability goals by employing product-level accelerated reliability tests. A flow chart of the presented reliability design process is shown in Figure 5. The process steps to which the research done in this dissertation offers new insight are marked with black rectangular borders. The critical assessment of loading conditions and accelerated test design are discussed in this section. Analytical lifetime estimations and physical failure mechanisms are discussed in the following sections.

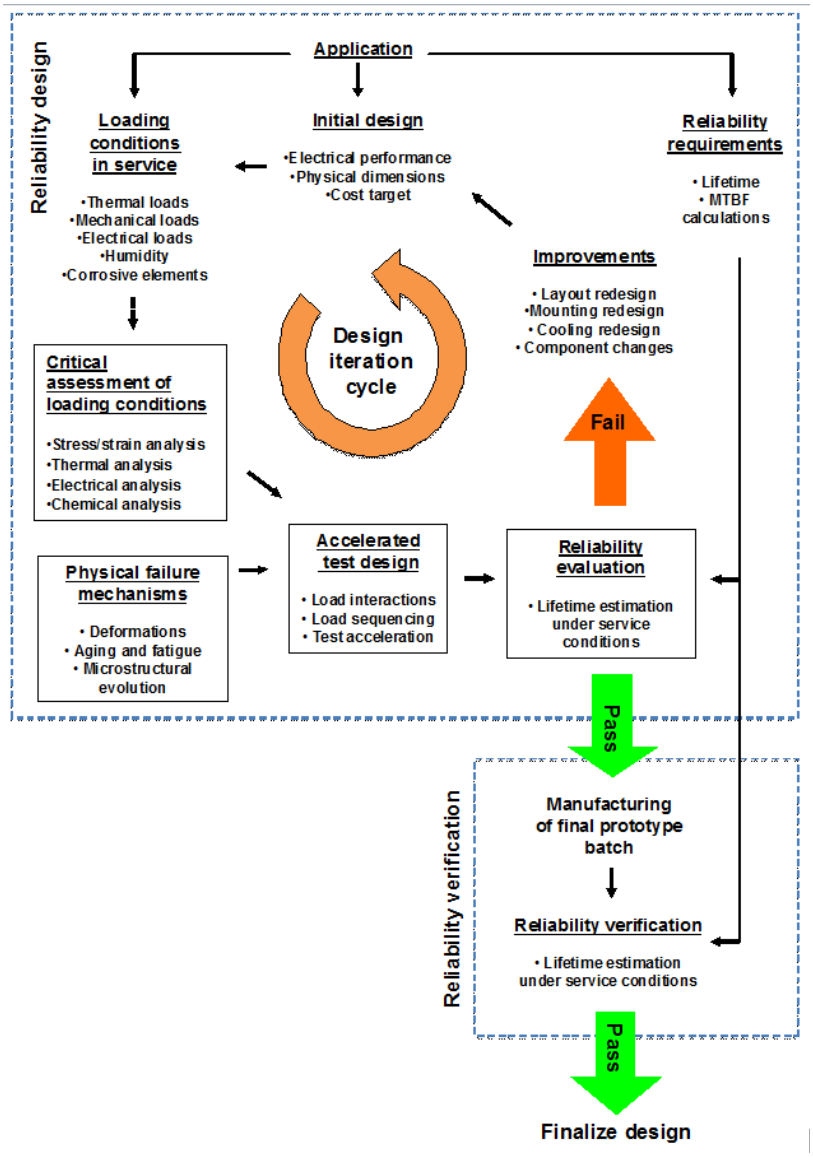


**Figure 5 – The reliability design process suggested for best efficiency.**

## 3.1 Critical assembly-level assessment of loading conditions

As was discussed previously, reliability engineering should begin early in the product development cycle to achieve the best time and cost efficiency. An efficient workflow for conducting the critical assessment of loading conditions during product design is shown schematically in Figure 6 and described below in more detail. The workflow is based on findings from the

studies within this work and aims to provide a comprehensive reliability evaluation of an electronic product in the design stage. The use of computational methods early in the product design can help avoid possible design flaws without the added costs of physical prototyping. However, the simulation results should always be verified with some control experiments.

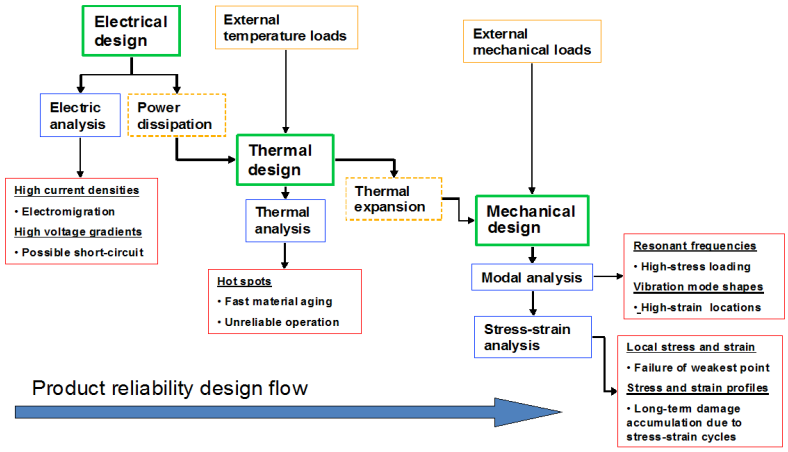


**Figure 6 – A workflow for efficient assembly-level reliability design process.**

*Electrical analysis*

The first opportunity to start reliability assessment is already in the electrical design stage of the component assembly. In addition to functional design, electrical analysis should be used in conjunction with component board layout drafts to determine possible reliability problems with local high power- and current densities. Also large voltage differences between adjacent parts should be avoided in order to reduce the possibility of short circuits due to breakdown of insulating layers.

*Thermal analysis*

After the initial electrical design and layout of a product or subassembly has been completed, a preliminary thermal analysis with computational fluid dynamic (CFD) or FE modelling methods can be conducted using the calculated power dissipation values and ambient temperature as input parameters. CFD and FE programs employ iterative heat transfer calculations on simplified 3D models derived from the component layout files. The thermal analysis is conducted to investigate the temperature gradients and possible hot spots caused by the combination of external thermal loads and internal power dissipation loads. Thermal analysis can be conducted experimentally by employing thermocouples, thermistors or non-contact infra-red imaging on the test assembly under thermal and power loading. Experimental thermal analysis has been employed in Publications I-V of this dissertation to characterize thermal loads induced by power cycling and thermal cycling tests on board-level solder interconnections.

*Thermomechanical analysis*

Once both electrical and thermal analyses show positive results on the designed assembly, the thermomechanical stresses are assessed either experimentally (if a mechanical prototype is available) or with FE simulations. If computational methods are used, the thermal profile from thermal analysis is loaded to the employed FE-tool in order to assess the thermomechanical stresses. FE-modelling results are highly sensitive to the accuracy of the employed material models and the applied boundary conditions. Therefore, the results should be verified experimentally

whenever possible. Thermomechanical stress and strain analysis have been successfully employed in Publication V of this dissertation to estimate the lifetime of a BGA component inside a mobile phone. Thermomechanical strains can also be measured experimentally by with strain gages or by employing precise non-contact imaging techniques, such as the Topography and Deformation Measurement (TDM) system [Fay04] used in Publication V and [Kar08] or Moiré interferometry [Zha00].

*Modal analysis*

The analysis of mechanical vibration and shock impact loads is usually started by conducting a modal analysis of the sample assembly. In modal analysis the dynamic response of the assembly is measured or calculated under vibration or impulse excitation. If mechanical properties (mass and modulus) of the used materials are known, FE analysis can be used to efficiently calculate the resonant mode shapes and frequencies of the structure. Experimental modal analysis can be conducted with transducers (typically accelerometers, strain gages and load cells), or non-contact via laser vibrometry. Typical excitation methods include mechanical vibration, impulse or acoustic signals exerted on the studied sample. The analysis of the signals usually relies on Fourier analysis. The resulting transfer function will show one or more resonances, whose characteristic mass, frequency and damping can be estimated from the measurements. Both experimental and FE modal analyses have been employed in Publications IV and VI of this dissertation to determine critical resonant frequencies of a mobile phone component board.

*Mechanical analysis*

After the critical natural frequencies of the assembly are found using modal analysis, stress and strain analyses under these worst-case loading conditions can provide insight into possible mechanical reliability problems in the PWB, component packages and interconnections. The most efficient method for stress and strain analysis is to employ computational FE-analysis verified by several experimental strain measurements. The strains can be measured experimentally by employing strain gage sensors on mechanical prototypes. Detailed information on the stress-strain conditions of the studied assembly is often a necessary prerequisite for the use of

subsequent damage models and lifetime estimations [Lee00]. Stress-strain analyses of critical electronic structures, in this case solder interconnections, have been conducted by employing FE modelling in Publications II and III.

## 3.2 Accelerated test design

The objective of accelerated reliability tests is to generate similar failure modes that would occur under normal product operating conditions in a considerably shorter timescale. This is accomplished by subjecting the test units to higher than usual levels of accelerating variables like temperature, voltage or mechanical stress. Caution should be exercised when selecting an accelerated test condition, since the accelerated loading may exceed the capabilities of the device and materials, inducing failures (overstress) failures that would not occur under normal use conditions.

Numerous testing methods have been standardized for the different needs of a wide spectrum of products and components. The test subjects can be exposed to loadings that are chemical, mechanical, thermal or electrical in nature or to a combination of the aforementioned loads, all depending on the presumed operation conditions of the subjects. Expected service life figures and expected loading conditions for several different electronic product types are given in Table 5.

**Table 5 – Service life and loading condition expectations of electronic product types [IPC92].**

| Product type | Expected service life | Expected loads |
|---|---|---|
| Automotive | >10 years | - Mechanical shock, vibration<br>- Power cycles<br>- Thermal cycles |
| Avionics | >20 years | |
| Military | >10 years | |
| Space | 5-20 years | |
| Telecommunications | 7-20 years | - Power cycles<br>- Thermal cycles |
| Computers | >5 years | - Power cycles |
| Consumer / portable | 1-3 years | - Power cycles<br>- Mechanical shock, vibration and<br>- bending |

In order to reduce uncertainty and simplify the assessment of imposed loading conditions, most accelerated reliability studies are conducted on component board level. Furthermore, in many cases component-level testing is undertaken to begin characterizing product's reliability when full system level test units are unavailable or prohibitively expensive. In the following subsections the most common accelerated board level tests for thermal, mechanical and electrical loads as well as their combinations are introduced and discussed.

### 3.2.1 Thermal- and thermomechanical tests

High temperature storage (HTS) tests are typically used to determine the effect of time and temperature, under storage conditions, on thermally activated failure mechanisms of electronic devices. During the test the samples are placed in elevated temperature test chambers without applied electrical stress.

The reliability effects of thermomechanical stresses on electronic assemblies are typically evaluated using Accelerated Thermal Cycling (ATC) tests. In ATC tests the samples are placed inside thermal cycling chambers, which allow the ambient temperature to be changed according to a preset thermal cycle profile. The thermal profile is defined by the maximum and minimum temperatures, temperature ramp rates and dwell times. The

accelerated thermal cycling test methods correspond well with true loading (i.e. the worst case scenario) experienced by electronics moved from one ambient temperature to another. However, due to negligible thermal gradients present in ATC testing, it cannot properly capture the thermomechanical stresses induced by internal heat dissipation of electronic devices. For this reason the thermomechanical stresses caused by operational power dissipation are best assessed with power cycling tests [Publication V, Lau07]. Accelerated thermal shock test is otherwise similar to the ATC test, except the temperature ramp rates are significantly faster. The faster ramp rates enable higher time compression during the test. Table 6 shows the most common test standards, loading conditions, expected failure types and typical test durations of the presented three tests.

**Table 6 - Test standards, loading conditions and expected failure types of common thermal tests.**

| Test type | Standards | Loading conditions | Expected failure | Typical test duration |
|---|---|---|---|---|
| High tempera-ture storage | JESD22-A103C IEC 60068-2-2 | Damp isothermal heat in an oven or thermal chamber. $T_{max}$ = 85°C – 300°C. | Component package damage due to aging, embrittlement of plastic parts. | From several hours to several months per batch. (10 hours – 2000 hours) |
| Thermal cycling | JESD22-A104C IEC 60068-2-14 | Isothermal temperature cycling $T_{min}$ = -60°C - 0°C, $T_{max}$ = 60°C - 200°C, Ramp rate < 15°C / min, 0.5 to 4 cycles per hour. | Fatigue failure of board-level interconnections, IC wire bonds and internal failure of component packages. | |
| Thermal shock | JESD22-A106B | Same as above, except ramp rate > 15°C / min. | | |

### 3.2.2 Mechanical tests

Shock impact tests are typically conducted by attaching the component boards into a test apparatus, where the drop test table moves vertically on guide rods to hit a strike surface. After the impact the test board vibrates according to its natural bending modes. The most damaging bending modes are typically the first and the second mode [Mar07, Publication IV & VI], which generate the most of the total displacement and strain. In general, the higher the frequency of the mode, the smaller the bending amplitude becomes.

Vibration tests have been conventionally conducted with either pneumatic or electromagnetic shaker systems. In both cases the test specimen is attached to an excitation table, which moves according to a predetermined signal. Depending on the system, the shaker may be able to excite the sample over all three or just one axis. Standardized vibration tests rely on frequency sweeps and random vibration to excite all the natural modes of the sample. However, if the natural vibration modes of the tested structure are known, the test time can be greatly reduced by concentrating the vibration load on these frequencies.

Bending tests are typically conducted on tensile pull machines, which are fitted with jigs to enable controlled curvature 3- or 4-point bending of the sample. Bending tests are typically overstress tests, in which the destructive limit of the assembly is investigated.

Table 7 shows the most common testing standards, loading conditions, expected failure types and typical durations of the discussed three tests.

**Table 7 - Test standards, loading conditions and expected failure types of common thermal tests.**

| Test type | Standards | Loading conditions | Expected failure | Typical test duration |
|---|---|---|---|---|
| Shock impact | JESD22-B104C JESD22-B110A JESD22-B111 IEC 60068-2-77 | Half-sine shock impact, 0.2-30ms duration, 5 - 10,000 G acceleration. | Board-level interconnection overstress or fatigue failure. | Several minutes to hours per single sample. |
| Vibration | JESD22-B103B IEC 60068-2-6 | Frequency sweep from 1-20Hz to 500-5000Hz at 0.001 - 500 G acceleration or 0.0127 - 1.5mm displacement. | Board-level interconnection fatigue or overstress failure. Component lead failure. | Several hours to several weeks per single sample. |
| Bending (3- or 4-point) | JESD22-B113 IEC 60068-2-21 | 1-3 Hz frequency 4-point bending of PWB, 2-4 mm displacement at center. | Board-level interconnection overstress failure. | Several minutes per single sample. |

### 3.2.3 Electrical tests

Electromigration testing is conducted by driving a predetermined amount of electrical current through the test sample. The tests are usually executed with much higher current densities than specified in service conditions to accelerate the test. Due to the high current densities involved, Joule heating must be taken into account when designing the test [Publications I and II]. The increased temperature will further accelerate failure due to faster diffusion and chemical reactions.

Power cycling tests are primarily conducted to investigate the thermomechanical loading induced by internal power dissipation of the

tested assembly. Unlike accelerated thermal cycling, the thermal loading induced by power cycling is highly nonuniform and corresponds well with the internal thermal loading under true service conditions. Although power cycling induces thermal, mechanical and electric stresses, the tests are typically defined by temperature profiles similar to accelerated thermal cycling. The limitations for power cycling load amplitude and frequency are generally dependent on the tested circuitry, although additional test acceleration may be achieved by using external heating elements. Power cycling test may also be conducted on non-functional assemblies by using solely external heating elements. In this case possible design problems with Joule heating and electromigration of the circuitry are not captured. Table 8 shows the common testing standards, loading conditions, expected failure types and typical durations of electromigration and power cycling tests.

**Table 8 - Test standards, loading conditions and expected failure types of common thermal tests.**

| Test type | Standards | Loading conditions | Expected failure | Typical test duration |
|---|---|---|---|---|
| Electro-migration (constant bias) | JESD61A.01<br>JESD202 | Constant DC or AC current at specified current density. | Conductor failure or short due to voiding and hillocking. | Several hours to several months per test batch (10-2000 hours). |
| Power cycling | JESD22-A122<br>JESD22-A105C | Thermal response of power cycle (measured from surface)<br>$T_{min}$ =10 - 40°C,<br>$T_{max}$ = 100 - 125°C,<br>2-6 cycles per hour. | Board-level interconnection fatigue failure due to thermo-mechanical loading, assisted by electro-migration. | |

## 3.3 Combined loading test design

Electronic products are seldom exposed only to a single type of stress or strain. For example portable products might be dropped during their

operation (i.e. when their components are running hot) while automotive, avionic and military products can be constantly exposed to concurrent vibrations and thermal excursions. Multiple loading tests have, therefore, been developed to simulate the real operational loadings as realistically as possible and to address all relevant failure mechanisms as in the use environment. The combining of several loadings is also expected to increase the rate of damage accumulation and thus decreasing the associated testing time and costs.

The most popular multiple load test method employed is the Highly Accelerated Life Test (HALT) originally presented by Hobbs [Hob00]. In HALT procedure electronic products or subassemblies are subjected to thermal shocks or increasing temperature and random multiaxial vibration. The objective of the HALT test is to cause failure by subjecting the sample to simultaneous, progressively increasing mechanical and thermal loads. Despite its name, the HALT method focuses on finding latent flaws and design errors in electronic assemblies through overstress failures. Thus, the method cannot be used for true lifetime or reliability assessments, as the stress conditions and failure mechanisms can differ substantially from those found in the service environment [Suh07, Mil338].

Despite the potential advantages associated with multiple loading tests, the methods are still seldom utilized for lifetime and long-term reliability evaluations. Although extensive research results have been documented for lifetime evaluations under to single load tests, limited research has been conducted on predicting failures caused by combined loads. Disagreement still surrounds the complex interactions between combined loadings and it is often unclear how to choose and set up test parameters in the most effective way or how to extrapolate the test results to actual use environments [Upa01, Mat11]. Different load frequencies (such as the low frequency loading in thermal cycling and the high frequencies in vibration testing) and amplitudes between the loading conditions confuse the matters even more. In this section some of these issues are discussed based on the current knowledge and findings of this dissertation.

In combined load testing the different load components may be combined consecutively, concurrently or in a mixture of consecutive and concurrent stresses. The choice of load sequencing has a profound impact on the

achieved test results, and the decision should be made according to the estimated true service environment.

### 3.3.1 Consecutive tests

Consecutive tests are generally easier to employ than concurrent test, as standardized single load test conditions may be applied directly. In most studies employing consecutive electrical, thermal and mechanical loads, the thermal and electrical loadings are conducted first. The sequence is based on the idea that the thermal end electrical loads cause irreversible material degradation due to accelerated aging processes, which has a marked impact on its mechanical reliability. However, it is important to realize that the impact of the preconditioning may not be monotonous. As is shown in Publication IV, conducting 1000 power cycles prior to shock impact loading actually improved the reliability of solder interconnections. A larger amount of power cycles, on the other hand, resulted in sharply declining shock impact reliability. This reliability trend is shown in the Figure 7. Others have reported similar results on the application of thermal loads as preconditioning for mechanical shock loads [Pen07]. Furthermore, the typical sequence may not always offer an accurate representation of the true loading case. For example, some products may experience harsh mechanical loads during transportation prior to becoming operational. Sitaraman and Perkins have studied the sequencing of consecutive vibration and thermal cycling tests [Per08]. They concluded that the combined loading was substantially more destructive when thermal cycling was applied prior to vibration loading.

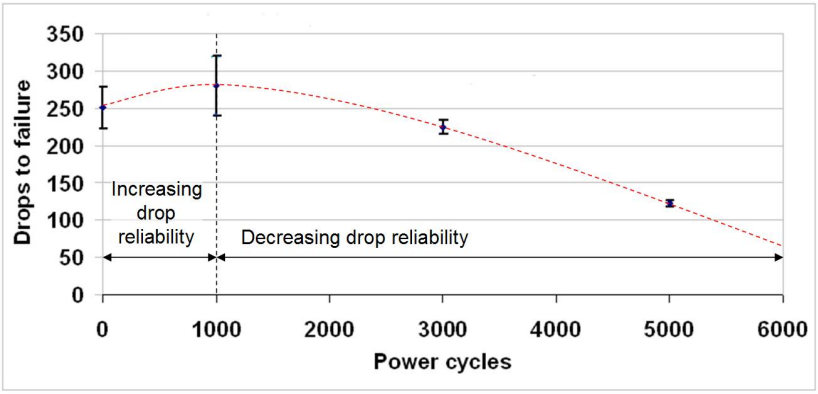


**Figure 7 – The reliability of component interconnections under consecutive power cycling and drop tests.**

It is worth noting that consecutive tests generally take a longer time to conduct than concurrent load tests or individual load tests (which may be executed simultaneously). Therefore, the value of consecutive tests is in improving the understanding of relevant damage mechanisms and determining the contribution of each loading condition to the failure. Once the primary failure mechanisms under the consecutive loads have been determined, the subsequent tests can be optimized to give faster results by focusing only on the relevant mechanisms. An example of such case is the consecutive electromigration, isothermal annealing and vibration test conducted in Publication II. The lifetime results and cross-sectional images of failed specimen from the study are shown in Figure 8. Although the annealing and electromigration pretreatments did not markedly affect the reliability of board-level interconnections under the subsequent vibration test, the cross-sectional analyses of the failed specimen provided new insight to the interacting of the different failure mechanisms. Based on the attained information on failure mechanisms, future studies with similar specimen and loading conditions can be expedited.

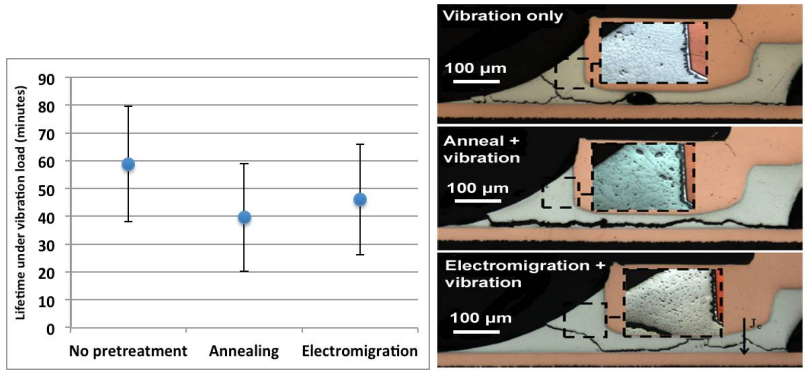


**Figure 8 – Left: The lifetime of pre-aged component interconnections under vibration tests. Pre-aging methods were isothermal annealing (750h at 125 °C) and electromigration stressing (750h at 1960 A/cm²). Right: cross-sectional images of the failed interconnections.**

### 3.3.2 Concurrent tests

Concurrent tests offer the highest damage acceleration and can be used to represent harsh operational environments, such as those found in the aviation and automotive industries. The design of realistic concurrent tests requires a profound understanding of the stresses and failure mechanisms induced by the combined loadings. One of the most common, and often misused, method of employing concurrent tests is the careless combination of high ambient temperature to mechanical or electrical loads. This method is based on the idea that the increased temperature will accelerate the accumulation of damage and lead to more efficient testing. This approach is flawed for several reasons. Firstly, the temperature affects both the mechanical and electrical properties of the tested assembly, which may lead to failure mechanisms never encountered under true service environment. In some cases the change in failure mechanisms can even reverse the stress amplitude - reliability trend [Upa97]. Secondly, the interactions and accumulation of stresses between the combined loads may not be properly accounted for. As an example, several published electromigration studies have used elevated temperature for test acceleration, yet appear to have failed to consider the effects of Joule heating [Yam06, Xu08].

In order to avoid the above mentioned oversights, the design of concurrent tests should always begin with a thorough assessment of all the stresses and failure modes caused by the individual loading conditions. The cumulative effects of the combined loads should be evaluated and compared with information on the failure behavior of the materials used in

the test assembly. The combination of vibration and power cycling loads has been employed in this manner in Publication III. The experimentally determined failure mode map of the tests, which defines the limits of vibration load amplitude for each different failure mode, is shown in Figure 9 below. Impressive test acceleration could be achieved with confidence when the concurrent vibration and power cycling tests were executed carefully. The test acceleration possibilities characterized in Publication III are shown in Figure 10.

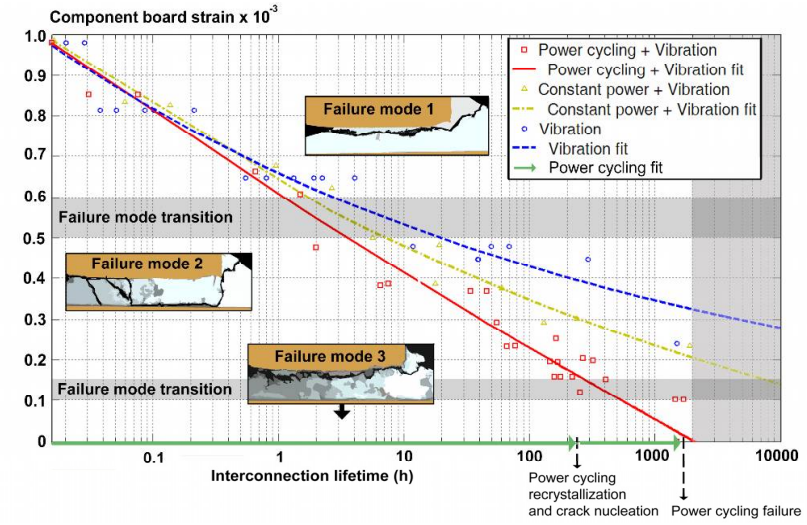


**Figure 9 – The lifetime trends and failure mode envelopes of a critical interconnection under concurrent electrical and mechanical vibration loading [Publication III]. Reprinted with permission from IEEE.**

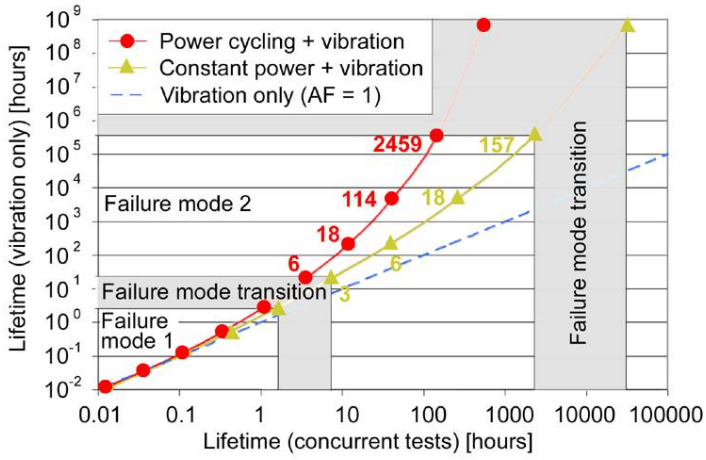


**Figure 10 – Test acceleration possibilities in concurrent electrical and vibration load tests determined by failure mode transition limits: Interconnection lifetime under combined tests plotted against the interconnection lifetime under room temperature vibration [Publication III]. Reprinted with permission from IEEE.**

Concurrently combining loads with vastly different stress levels (e.g. overstress and fatigue loads) and time scales (e.g. mechanical shock and thermal or power cycling) is particularly challenging. In order for the slower-accumulating fatigue load to have any measurable effect on the test result, the faster loading will have to be either reduced in amplitude or applied later in the test. These solutions lead to new questions: do the lowered amplitude loads offer a good enough representation of the true load case and how long should the fatigue load be applied before the first occurrence of the overstress load? This specific problem on the concurrent combination of shock impact and power cycling loads on board-level interconnections has been studied in Publication IV.

# 4 Lifetime estimation

Arguably the most challenging aspect of accelerated life testing is to estimate the field reliability based on accelerated test results. This requires an up-front knowledge of acceleration factors between the test and the use condition, as the accuracy of reliability prediction for use conditions is directly dependent on the accuracy of the acceleration factors (AF) used.

There are currently three approaches to develop an acceleration factor model. The first and most accurate approach is to experimentally test samples under various accelerated and actual use conditions. This approach is not only expensive but also impractical as it may take years to get data from actual use condition testing. The second and least accurate, but quick and straightforward approach is to conduct accelerated tests by varying the load parameters and then fitting an experimental or statistical model on the results. Since multiple runs of the accelerated tests need to be completed in a reasonable time, the estimation of field reliability is based on extrapolation of the fitted model with little verification. The first approach is employed in Publications V and VI of this dissertation in order to study the failure mechanisms occurring in solder interconnections of a mobile phone under use conditions. The second approach is used in Publication III to evaluate test acceleration of concurrent thermal and vibration loads within a specified strain range.

Between these two extremities is the third approach, damage mechanism based life prediction, in which the time and temperature dependent behavior of the used materials and the geometric details of the assembly are taken into account. The fundamental assumption in this approach is that the employed material constitutive relations accurately capture the material responses to field and accelerated loading conditions. Most of the damage mechanism based life prediction models establish a power law relationship

between a damage metric to the number of cycles required to meet a certain failure criterion. A unique value of quantified damage and specific failure definition are used to represent the full history of the assessed structure. Most models that address fatigue failures require stress-strain data in order to predict service life.

The damage-based life prediction models currently represent the most advanced method employed to calculate lifetime estimations of electronic assemblies. The most popular models are briefly introduced in the following pages. The accumulated strain and accumulated strain-energy models are applied and compared against experimental results in the Publication V of this dissertation.

## 4.1 Temperature-dependent damage processes

For static isothermal loading the most widely used method to assess damage acceleration is using the Arrhenius' law (eq.1),

$$R = Ke^{\frac{-E_a}{kT}}, \qquad (1)$$

in which R is the process rate, K is a constant, $E_a$ is the activation energy for the process, k is the Boltzmann's constant, and T is the temperature in Kelvins. The Arrhenius relation works well in these types of loadings because many of the different material phenomena, such as solid-state diffusion and chemical reactions, share this similar temperature-rate dependency. The acceleration factor (AF) between two temperatures for identical damage process can be simply expressed by eq.2

$$AF = e^{-(E_a/k)(\frac{1}{T_{use}}-\frac{1}{T_{test}})}, \qquad (2)$$

in which $T_{use}$ is the temperature in field conditions and $T_{test}$ is the test temperature.

Most mechanical and thermomechanical damage models can be divided into two major categories, based on the fundamental mechanism viewed as being responsible for inducing damage: (1) strain-based and (2) energy-

based. Both damage model types are discussed briefly below. The most popular models from these categories are collected in Tables 9 and 10 along with notes on their applicability, assumptions and required experimental constants.

*Strain-based models*

The strain-based models predict failure based on calculated or experimental determinations of the applied plastic shear strain. Power laws frequently referred to as 'modified Coffin-Manson equations' are commonly used to assess the reliability of electronic structures. The Coffin-Manson equation considers only plastic deformation [Man53, Cof54], which limits its application to low cycle fatigue (LCF) loading. The Coffin-Manson model can be combined with Basquin's equation [Bas10] to account for elastic deformations in high cycle fatigue (HCF) loading. The resulting model is commonly referred to as the "Total strain model" [Kil91].

The original Coffin–Manson fatigue life relationship was modified by Engelmaier [Eng82] into a simplified model for life cycle prediction of solder joints. The model has proved to be a useful tool, but it also has several deficiencies and over-simplified assumptions associated with it. For example, the Engelmaier model is only applicable to certain package types, does not account well for solder joint geometry, and cannot handle the creep deformation of solder joints correctly [Cha09]. Despite its limitations, the Engelmaier model still remains one of the most widely used models for prediction of solder joint reliability [Cha09].

**Table 9 - Common strain-based damage models.**

| Model name | Damage equations | Appli-cation | Legend |
|---|---|---|---|
| Coffin-Manson | $\frac{\Delta\varepsilon_p}{2} = \varepsilon'_f (2N_f)^c$ | LCF (plastic strain) | $N_f$ =cycles to failure, $\varepsilon'_f$=fatigue ductility coefficient, $\Delta\varepsilon_p$ =plastic strain range, c =experimental constant. E =Young's modulus, b =fatigue strength exponent, $s'_f$=fatigue strength coefficient, $\Delta\varepsilon_e$ =elastic strain range. |
| Total Strain | $\frac{\Delta\varepsilon_p}{2} = \frac{s'_f}{E}(2N_f)^b + \varepsilon'_f (2N_f)^c$ | HCF +LCF | |
| Engelmaier | $N_f = \frac{1}{2}\left[\frac{\Delta\varepsilon_t}{2e'_f}\right]^{\frac{1}{c}}$, $c = c_0 + c_1 T_{sj} + c_2 \ln\left(1 + \frac{360}{t_{dwell}}\right)$ | Tempe-rature cycling (LCF) | $N_f$ =cycles to failure, $\varepsilon'_f$=fatigue ductility coefficient, $\Delta\varepsilon_t$ =total strain range, $T_{sj}$ =mean cyclic temperature, $t_{dwell}$ = temperature dwell time in days, $c_0$,$c_1$,$c_2$ = experimental constants. |

*Energy-based models*

The energy-based fatigue models are the newest models in use today, and are based on calculating the overall stress-strain hysteresis energy of the system or solder joint. Among the energy-based methods, Darveaux's model [Dar00] is arguably the most popular one [Zha03]. In Darveaux's model the total fatigue life us divided to the time associated with crack initiation and the time associated with crack growth. The error in lifetime

estimate using the Darveaux model is reported to be within +/- 25% for solder interconnections of plastic ball grid array (PBGA) packages. [Dar00] Other energy-based models include Liang's model [Lia97], which closely resembles the Engelmaier and Total Strain models, albeit substituting the damage criterion from strain to stress-strain energy, and Syed's model [Sye01], which specializes in creep deformation of solder interconnections.

**Table 10 - Common energy-based damage models.**

| Model name | Damage equations | Appli-cation | Legend |
|---|---|---|---|
| Darveaux | $N_f = N_0 + \frac{a}{da/dN}$, $da/dN = C_3 \Delta W^{c_4}$, $N_0 = C_1 \Delta W^{c_2}$ | LCF | $N_f$ = cycles to failure, a = crack path length, da/dN =crack growth per cycle, $N_o$ =crack initiation, $\Delta W$ =viscoplastic strain energy/cycle, $C_1$-$C_4$ =material constants. |
| Liang | $N_f = C(W_{SS})^{-m}$ | LCF | $N_f$ = cycles to failure, $W_{ss}$ = stress-strain cycle energy density, C + m = temperature dependent material constants. |
| Syed | $N_f = \left(0.022 D_{gbs}\right)^{-1} + \left(0.063 D_{mc}\right)^{-1}$ | LCF (creep) | $D_{gbs}$ =Accumulated equilevant creep strain / cycle for grain boundary creep, $D_{mc}$ = same as above for matrix creep. |

*Constitutive relations*

The accuracy of all the above-mentioned accumulated damage models are largely defined by their respective constitutive material relations. Constitutive relations describe the response of the assessed material to different loads, and are used to calculate the required stress and/or strain metrics for the damage model. The most common constitutive relation is given by eq.3:

$$\varepsilon = \varepsilon_e + \varepsilon_p + \varepsilon_c ,$$

(3)

in which ε is the total strain, $\varepsilon_e$ is the elastic strain component, $\varepsilon_p$ is the plastic strain component and $\varepsilon_c$ is the creep strain component. Each of these components is assessed separately using its own constitutive relation. However, in actual life testing this separation can be difficult and lead to inconsistent results. To address this issue, new unified constitutive models, such as the Anand model [Ana85], have been developed for the most critical materials.

## 4.2 Considerations on life prediction accuracy

Building accuracy in a life prediction model is an arduous task. This is partly due to variations in the fatigue process itself and partly due to material variations and modeling assumptions. The situation is most complicated for solder interconnections because of the nonlinear material behavior, complex joint shapes, 3-dimensional structures, and multi-axial loading conditions. Besides solder, a circuit board assembly also includes materials such as copper in metal traces and layers, silicon dies, epoxy-based mold compounds, die attach adhesives and underfills, FR-4 & Bismaleimide triazine (BT) substrates, and solder mask polymers. All of these materials have temperature dependent behavior, anisotropic properties and some are viscoelastic in nature. The accurate properties of most materials used in electronics are still largely unknown.

Although finite element analysis can handle most of the aforementioned complexities rather accurately, these factors make the analysis computationally intensive and inefficient. In order to increase analysis efficiency, or make it even attainable in some cases, a number of assumptions and simplifications have to be made. Individual material layers are often omitted, and detailed features of metallizations are rarely incorporated. There are usually singularities at the edges of the model, where volumetric averaging of values has to be used [Sye96]. Damage-free material properties are typically modeled, even though it is known that most of the life of the assembly is spent under degrading physical properties. All of these factors, both experimental and analytical, combine to produce error in the predicted life.

## 4.3 Combination of damage models for multiparameter loading

Applying the lifetime estimation models discussed in the previous section to multiple loading conditions brings in a new challenge: How should the combined damages be assessed? The most straightforward method is the linear superpositioning of normalized accumulated damage, known as the Linear damage superpositioning approach (LDSA) or the Palmgren-Miner rule [Pal24, Min45]. However, the accuracy of LDSA has been largely debated due to its highly simplified approach to handling damage interactions. To address this issue, Dasgupta and Upadhyayula introduced the incremental damage superpositioning approach (IDSA), which corrects some critical shortcomings of the LDSA model [Upa01]. In this section these two superpositioning methods are briefly discussed.

### 4.3.1 Linear damage superpositioning (LDSA)

Linear damage superposition rule is a first-order approximation for damage calculation and fatigue life prediction under multiple loadings. The hypothesis of the rule is that the normalized damage fractions of the total consumed life can be superimposed linearly. The rule states that the damage fraction at any stress is linearly proportional to the ratio of the number of cycles to the total number of cycles that would produce failure.

The linear damage superposition rule has several severe shortcomings:

- The rule is insensitive to the sequence of different loads in consecutive tests.
- The rule assumes that all loading conditions affect the same damage mechanisms and that the failure occurs only due to this single mechanism.
- The rule does not consider any interactions between the loading conditions in concurrent tests (eg. temperature effects on material mechanical properties are not considered when combining thermal and mechanical loads).

Despite its shortcomings, the linear superpositioning rule works well for loads of varying amplitudes at similar frequencies. However, interactions between stresses with different time scales are not captured. The linear superpositioning approach is illustrated in Figure 11 below.

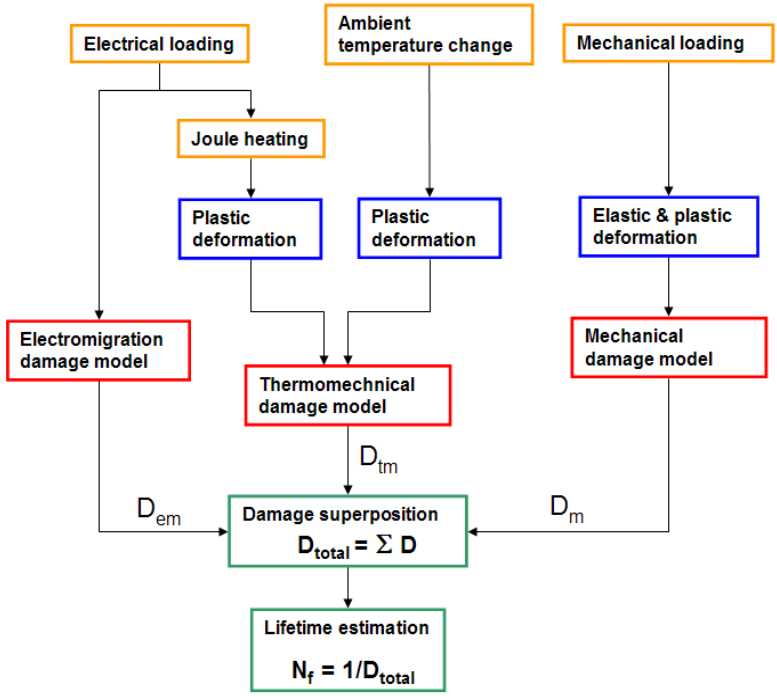


**Figure 11 – The linear damage superpositioning approach.**

### 4.3.2 Incremental damage superpositioning (IDSA)

The incremental damage superpositioning approach can be considered as a variant of the linear superpositioning approach, which is broken down into increments to account for varying stress levels and time scales. In IDSA the rate of damage accumulation due to faster HCF loads (such as vibration or shock) is quantified as a function of applied temperature. Furthermore, bias due to slowly changing LCF loading (such as thermal cycling) mean stress is considered when estimating the damage accumulated due to the fast HCF loading. These features allow IDSA to quantify the macroscopic interactions between HCF and LCF loadings with vastly different load frequencies.

IDSA consists of four steps summarized as follows:

1. Thermal characterization of the specimen

2. Mechanical characterization of the specimen under various temperatures

3. Stress analysis for all affecting loads

4. Superpositioning of mechanical and temperature-induced damages.

The IDSA approach is shown in Figure 12.

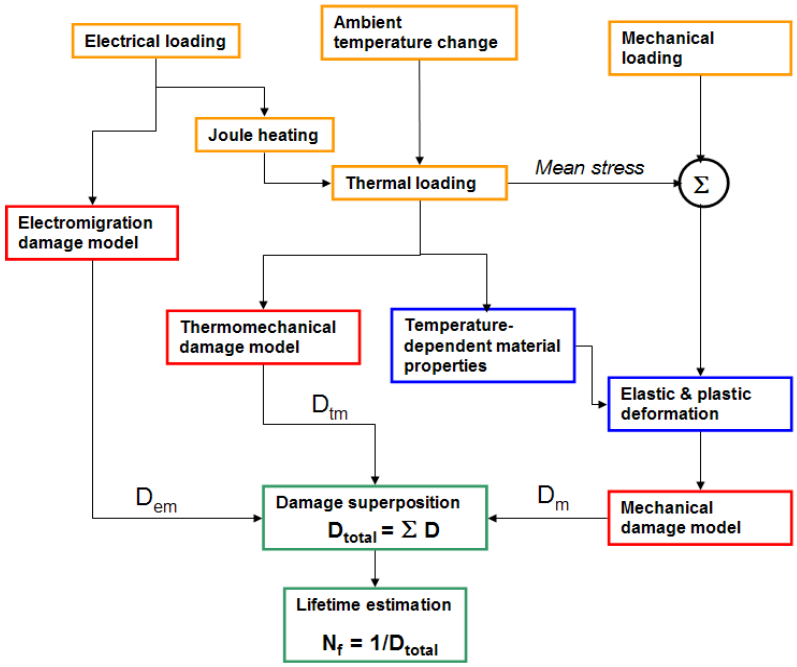


**Figure 12 – The incremental damage superpositioning approach (Adapted from [Upa01]).**

## 4.4 Micromechanical physics of failure approach for lifetime analysis

All the lifetime estimation approaches presented above use phenomenological macroscopic damage prediction models, in which the

true underlying physical processes and microstructural changes are not considered. The macroscopic damage models are most often based on empirical curve fittings to experimental data and the damage indicators are chosen through qualitative understanding of the associated failure mechanisms. These macroscopic models are relatively easy to employ and give reasonably accurate estimations when employed within the limits of experimental validations. However, they are highly risky when applied on cases beyond the experimental validations, which provide the many damage model constants. In order to properly extend reliability prediction beyond experiments, the true physical and microstructural phenomena have to be included in the modelling process.

Dasgupta and Upadhyayula have presented a physics of failure (PoF) based model approach to estimate fatigue failure of solder interconnections under mechanical and thermomechanical loads [Upa01]. The PoF modelling approach is shown in Figure 13 and executed as follows:

1. Cyclic history of the microscopic shear stress, material microstructure and temperature of interest are determined. A transition model is used to assess the microscopic stresses from observed macroscopic stresses or strains.

2. A model for microstructural evolution is applied to capture the effects of time, temperature and stress/strain history on the relevant material models.

3. For a given microstructural state, the damage accumulated due to cyclic deformation is computed and compared against criterion for fracture.

4. Steps 1-3 are repeated for the next loading cycle and the consequent microstructural changes and material parameters are updated until the accumulated damage has enabled crack initiation and propagation to fail the specimen.

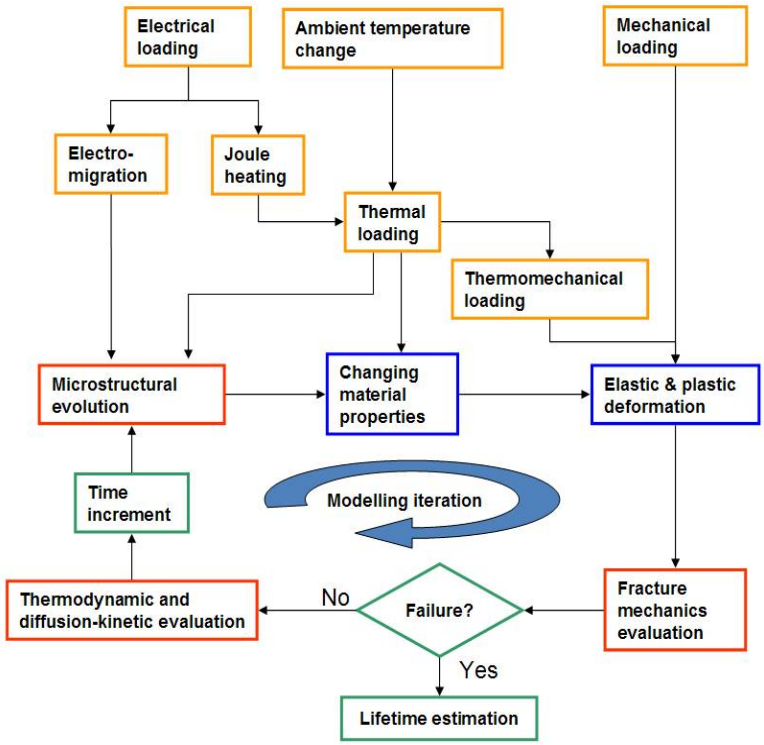


**Figure 13 – A micromechanical physics of failure approach for multiple loads**

The physics-based approach is unquestionably the most realistic and comprehensive method to evaluate reliability and, provided that the material-physical evaluations are accurate, can be used to extrapolate test cases beyond experimentation with reasonable confidence. Furthermore, the physics-based approach has the built-in ability to assess multiple interacting loads, removing model extrapolation uncertainties inherent with the damage superpositioning approaches. However, the physics-based approach has yet to gain widespread use due to several reasons:

- The approach requires that the entire fatigue history of the specimen has to be incrementally simulated, since the incremental damage is a function of the assessed material's microstructural state. This requires a high amount of computational resources for even small samples with short lifespan. Employing the PoF method on complete circuit assemblies with years of estimated service life is currently unfeasible.

- The development of materials and processes for microelectronics manufacturing has increased tremendously during the last decades. As a result, the aging and microstructural evolution of many materials are still largely unknown and under research. Therefore, all the physical models required to employ the PoF approach do not exist or are inaccurate.

The aforementioned shortcomings of the PoF approach will diminish with time due to availability of increased computing power and the continuous material-scientific research conducted on electronic materials. Therefore, it is probable that in the future the physics-based approach will supersede today's analytical models. This will substantially improve the accuracy of lifetime analysis and markedly reduce the amount of required experimental testing.

# 5 Reliability of lead-free SnAgCu solder interconnections

It is generally recognized that one of the most challenging parts in the reliability assessment of a contemporary electronic assembly are the board-level solder interconnections. This is due to the almost exclusive use of tin-based solder materials, which exhibit a complicated dependency on temperature, time and deformation rate in their mechanical properties. Because of the vulnerability and complicated reliability behavior of tin-based solder interconnections under electrical, thermal and mechanical loads, they were chosen as the focal point of the conducted reliability research. Thus, the reliability assessment methodology presented in this dissertation has been demonstrated on board-level solder interconnections.

The main reasons for the use of tin based solders are their good compatibility with other common electronic materials, reasonably low melting temperature and excellent suitability to low-cost, high-volume production. Despite their low mechanical strength, solder interconnections are responsible for not only electrical, but also mechanical and thermal connections between components and PWBs. Due to the banning of lead-containing solder in the EU markets since July 2006 [EC02], the traditional tin–lead solders have been replaced with other tin-rich alloys. From these alloys, the near-eutectic SnAgCu has emerged as the most promising candidate for general–purpose replacement of tin–lead in surface mount reflow processes [Ma09].

In this section the mechanical properties and microstructural phenomena of SnAgCu solder affecting the reliability of board-level interconnections are presented. It is demonstrated throughout the dissertation publications that understanding the time, rate and temperature-dependent behavior of

solder interconnections is a necessary prerequisite to conducting accurate board-level reliability predictions.

## 5.1 Microstructure and its evolution in solder interconnections

The mechanical properties of metals are highly dependent on the microstructures formed during fabrication processes. Changes in solder joint microstructure directly impact their reliability, and thus the operational life of electronic assemblies. The current solder alloys are primarily based on tin due to its appropriate reactivity with the typical electronics contact metallizations.

### 5.1.1 Solidification structure (after reflow)

The solidifications structure of eutectic or near-eutectic SnAgCu solder in electronic interconnections is typically dendritic. Because of the low solubility of silver and copper in solid tin, most of the silver and copper in SnAgCu solder react with tin to form $Ag_3Sn$ and $Cu_6Sn_5$ intermetallic phases in the matrix of β-Sn. In the eutectic structure of $Ag_3Sn$ + $Cu_6Sn5$ + β-Sn, these two phases appear as finely dispersed particles [Lew02]. Furthermore, the solder reacts with the contact metallization of the printed wiring board and component underbump metallurgy during soldering. These interfacial metallizations are partially dissolved in the liquid solder and form intermetallic compound layers during solidification.

In addition to the fine IMC precipitates forming the eutectic structure, several larger primary $Ag_3Sn$ and $Cu_6Sn_5$ intermetallic precipitates can typically be found in cross-sections of SnAgCu-interconnections. These precipitates are formed early in the solidification of the liquid tin solder, as the solder is cooled and becomes locally supersaturated with the alloying elements [Lau05]. The formation of these large primary intermetallic precipitates is generally undesirable: they present little known advantages, but provide interfaces for easier crack nucleation and propagation. An optical microscope image from a cross-section of as-solidified eutectic Sn4.8Ag0.7Cu solder interconnection on Cu UBM and PWB metallization is shown in Figure 14.

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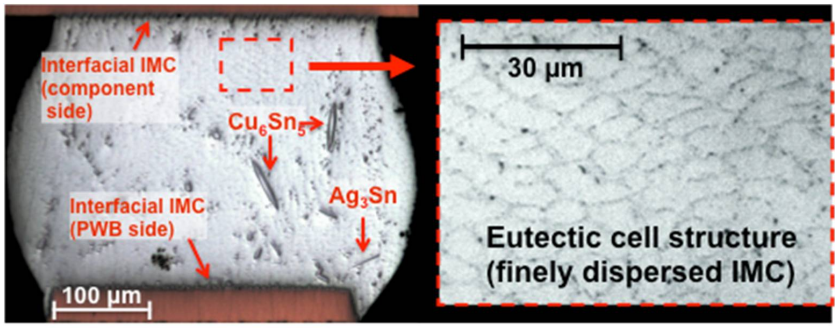


**Figure 14 – The microstructure of an as-solidified Sn4.8Cu0.7 solder interconnection on Cu/Cu terminations.**

During the reflow process, when the partially dissolved component underbump metallurgy and printed wiring board contact metallization begin to solidify, one or more intermetallic compound layers are formed at the interface. Depending on the reflow time and temperature, excessive growth and spalling of IMC layers may take place [Lau05, Lau10] Furthermore, cross-interactions of the metals on the two sides of the joint may affect the microstructure and composition of the complete interconnection. The interfacial layers are typically mechanically brittle due to the highly covalent character in their bonding [Lau05, Lau10]. This brittleness may cause reliability problems if the interconnections are subjected to high strain rate loading conditions.

### 5.1.2 Effect of solidification structure on properties of SnAgCu solder

The size of grains within a material have an effect on the mechanical strength of the material. The grain boundaries are structurally more disordered than the inside of the grain, thus they prevent the dislocations from moving in a continuous slip plane as shown in Figure 15a. This impeding of dislocation movement increases the yield strength of the material. The higher the applied stress required to move the dislocation, the higher the material yield strength. Thus, there is an inverse relationship between grain size and material yield strength [Her96].

Under mechanical loading, the finely dispersed Ag3Sn particles hinder the ability of the solder alloy to deform plastically due to the Orowan mechanism shown in Figure 15b. The higher the Ag content in a SnAgCu solder (up to 3-wt%), the higher the elastic modulus and hardness of the

alloy becomes [Kel11]. Consequently, lower Ag solder joints perform better under high strain-rate mechanical loading conditions [Lai04, Lai06, Kim06]. The Cu6Sn5 particles in the eutectic SnAgCu structure have a similar effect as the $Ag_3Sn$ crystals, but less significant due to the larger size of Cu6Sn5 crystals. The Orowan mechanism is illustrated in Figure 15.

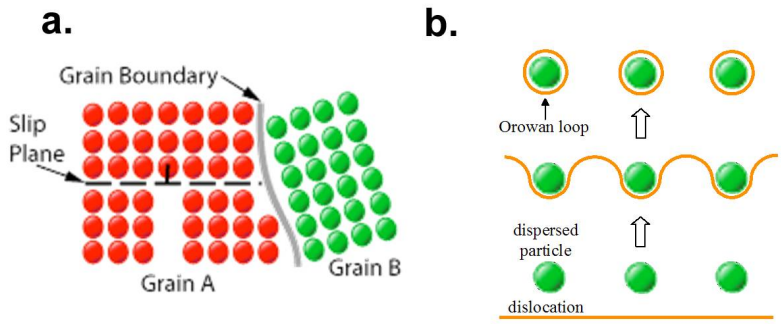


**Figure 15 – Strengthening mechanisms: a) grain boundary strengthening and b) precipitation strengthening.**

### 5.1.3 Evolution of solder microstructure under service

The as-manufactured SnAgCu solder interconnections are not in an equilibrium state because of the high cooling rate of the typical soldering processes [Lau05]. The tin matrix of the eutectic structure is supersaturated with silver and copper at room temperature. Thus, there is a driving force for the nucleation of $Cu_6Sn_5$ and $Ag_3Sn$ intermetallic precipitates. This process requires the atoms to diffuse only over short distances, and the thermal activation energy needed is low. Since the precipitation of these compound phases is by solid state diffusion, they are very small in size and thus have significant strengthening effect.

With longer aging times, another change occurs in the microstructure – coarsening of the IMC particles. Driven by the minimization of surface free energy, the precipitate particles merge into larger ones. This thermodynamically-driven spontaneous process occurs because larger particles are energetically more stable than smaller particles. Therefore, the number of smaller particles continues to shrink, while larger particles continue to grow. High temperature can significantly enhance this process. According to the Orowan relation, the larger the dispersive particles, the smaller their strengthening effect. The coarsening process requires the

atoms to diffuse over longer distances and thus takes a relatively long time. The grain and IMC precipitate coarsening process is shown in Figure 16 from cross-sections of interconnections exposed up to 15,000 power cycles (see Publication IV for details).

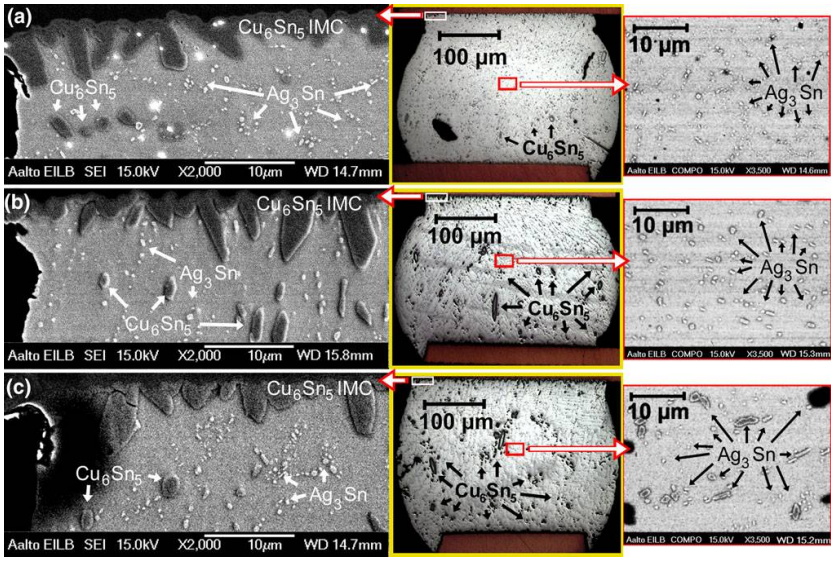


**Figure 16 – The coarsening of Sn4.8Cu0.7 solder interconnection: a) as reflowed b) after 5000 power cycles and c) after 15000 power cycles [Publication IV]. Reprinted with permission from Elsevier.**

*Recovery and recrystallization*

Recovery and recrystallization are competing restoration processes, which both release the increased internal energy of deformed material.

Recovery is a process by which deformed tin grains can reduce their stored energy by removing or rearranging defects in their crystal structure. These defects are introduced by plastic deformation of the material and act to increase the yield strength of a material. Since recovery reduces the number of defects the process generally results in reduction of material strength and increase in ductility [Lin86]. Recovery competes with recrystallization, as both are driven by the stored energy, but is also thought to be a necessary prerequisite for the nucleation of recrystallized grains [Lin86].

Recrystallization is a process, in which new stress-free crystals are formed within the deformed microstructures, and the new crystals grow in size consuming the deformed grains. Similar to the recovery process, recrystallization usually causes reductions in the strength and hardness of material and a simultaneous increase in the ductility. In the recrystallized region a continuous network of high angle grain boundaries provides favorable sites for cracks to nucleate and propagate intergranularly, which can accelerate failures in solder interconnections [Hen04, Mat04]. Figure 17 shows a completely recrystallized Sn3.0Ag0.5Cu solder interconnection, which has failed due to intergranual crack propagation (see Publication I for details on the experiment).

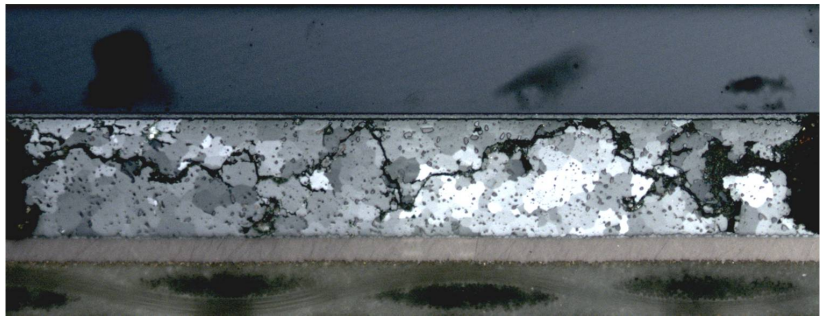

**Figure 17 – A cross-sectional polarized light microscopy image of a recrystallized Sn3.0Ag0.5Cu solder interconnection, which has failed due to intergranual cracking.**

*Growth of intermetallic layers*

After solidification, the interfacial IMCs grow thicker and new IMC layers may form at the interface, depending on the temperature to which the assemblies are exposed [Lau05]. Under high current density electromigration plays a significant role in the growth of the IMC layers. Due to the electron flow, the conductor atoms are typically pushed from the cathode towards the anode, resulting in void formation near the cathode and enhanced IMC formation at the anode interface. The growth of intermetallic layers due to high temperature exposure and/or electromigration is detrimental to the mechanical shock impact reliability of solder interconnections.

## 5.2 Mechanical properties of SnAgCu solder interconnections

At and above room temperature the macroscopic deformation behavior of SnAgCu solder is considered ductile [Kel11]. This is mainly due to tin's homologous temperature (ratio between service temperature and melting temperature in Kelvin) exceeding 0.5, which enables time-dependent structural changes, such as creep and dynamic recovery, to occur. Thus, under most service conditions the tin-rich solder accommodates strains and stresses by plastic deformation.

In addition to the bulk solder material, solder interconnections consist of metallization on contact surfaces and the intermetallic layers that form between the contact metallization and solder during manufacturing. The intermetallic layers provide good adhesion between the solder and terminal metallization. However, in contrast to the SnAgCu solder material, intermetallic phases are mechanically hard and brittle [Hay09]. Therefore, the ductile solder material has to absorb mechanical loads in order to avoid brittle failure of the interfacial intermetallic layers.

Assessing the physical properties of solder interconnections is complicated by the fact that, as was discussed in the previous section, the solder material and intermetallic layers undergo constant changes in microstructure even at room temperature [Ma09]. The evolution of solder microstructure affects the mechanical properties and response of interconnections to loading conditions. Therefore, the properties of solder interconnections are heavily dependent on their age and load history after manufacturing. Some basic mechanical characteristics, such as plastic deformation, dynamic recovery and fracture of solder interconnections are briefly discussed here.

### 5.2.1 Plastic deformation

Time-independent (ie. instantaneous) deformation of tin at various temperatures is presented in Figure 17 by stress–strain diagrams, in which the elastic and plastic behaviors are differentiated by the yield stress. At stress levels equal to or higher than the yield stress, deformation is not recoverable upon release of stress and the material is deformed plastically. When loading exceeds the yield stress, the stress has to be increased for

additional strain to occur. This strain hardening effect is typical for ductile materials at high homologous temperatures. However, at high homologous temperatures plastic deformation occurs even below the material yield strength due to time-dependent plastic creep deformation. Due to the low melting point of tin, the SnAgCu solder exhibits time-dependent plastic deformation even under low mechanical loadings at almost all practical service temperatures. Creep behavior of SnAg solder in different temperatures is shown in Figure 18.

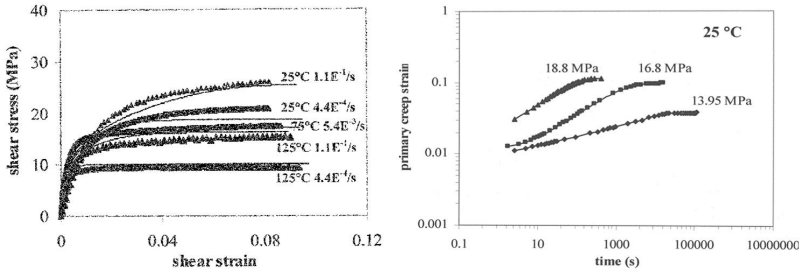


**Figure 18 – The time-independent deformation (left) and time-dependent creep deformation (right) of Sn3.9Ag0.6Cu solder [Zha04]. Reprinted with permission from Springer.**

### 5.2.2 Strain rate hardening

Since the homologous temperature of Sn at room temperature is over 0.5, the mobility of vacancies in the tin lattice is appreciable. This mobility enables dynamic recovery of the tin microstructure, which has been plastically deformed under mechanical loading. The effectiveness of dynamic recovery depends on the material temperature and rate of plastic deformation, as recovery itself depends on the material's diffusion rate. The balance between recovery and deformation-induced work hardening determines the mechanical strength of the solder at different strain rates. The amount of strain rate hardening occurring in tin-based solders is notable at room temperature and above [Mar07, Ama02, Che00].

### 5.2.3 Fracture

Fracture in solder interconnections can be either ductile or brittle. Ductile fracture requires a relatively large amount of energy, as the material undergoes significant plastic deformation during crack propagation. Brittle fracture, on the other hand, requires little to no plastic deformation of the material during crack propagation. The tendency towards brittle fracture is

increased at low temperatures and high strain rates due to the strain rate hardening effect of SnAgCu-solder material. When the strength of the strain rate hardened solder exceeds the fracture strength of the interfacial intermetallic layers, the intermetallic layers may experience brittle failure. A brittle failure of a solder interconnection is shown in Figure 19 (see Publication IV for details on the experiment).

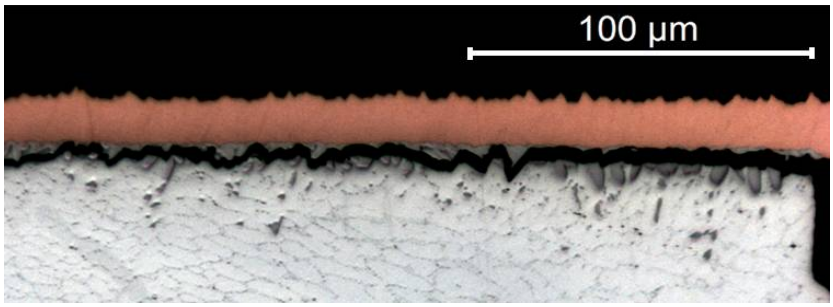


**Figure 19 – A brittle failure of solder interconnection subjected to shock impact loading.**

Typical ductile fracture mechanism of SnAgCu-solder under mechanical shear loading is microvoid coalescence [Kan06]. The fracture mechanism occurs by microvoid nucleation, growth and coalescence to form cracks under plastic strain. As the deformation continues, the voids enlarge, which consumes most of the energy required for fracture. The final step of the fracture mechanism is coalescence of the numerous voids in the direction of maximum shear stress, resulting in macroscopic crack formation. The resultant fracture surface is highly irregular in appearance. Ductile failure of a solder interconnection due to mechanical vibration is shown in Figure 20 (see Publication III for details).

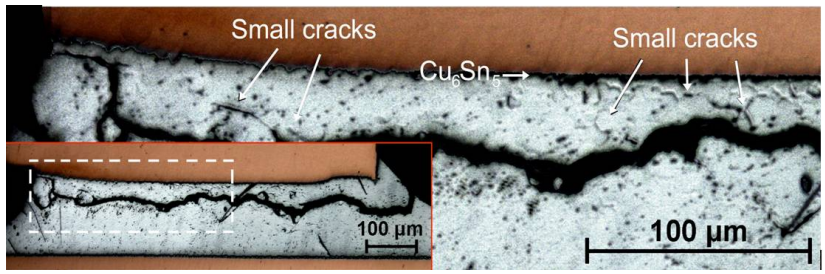


**Figure 20 – A ductile fracture of SnAgCu solder interconnection subjected to mechanical vibration.**

### 5.2.4 Fatigue

Solder interconnections subjected to cyclic loading may experience fracture even at stress levels below the solder yield strength due to fatigue. Fatigue failure is a three–stage process involving crack nucleation, crack growth, and final failure. Fatigue cracks nucleate preferentially at locations where stresses can concentrate on the surface of a material. If suitable crack nucleation sites are not available, plastic deformation will produce intrusions and extrusions on the surface of the material. Tensile stress produces a plastic zone at the tip of the crack and makes the crack tip stretch plastically by a finite length. The following compressive cycle pushes the crack forward, making the new surface fold forward. This same mechanism repeats on every cycle and the crack propagates until the material fails completely. At some stage in the growth of a fatigue crack the area of the undamaged region will be small enough to allow an ordinary brittle or ductile fracture to occur. An example of such a mixed-mode failure of a solder interconnection under low amplitude mechanical vibration is shown in Figure 21 (see Publication III for details of test execution).

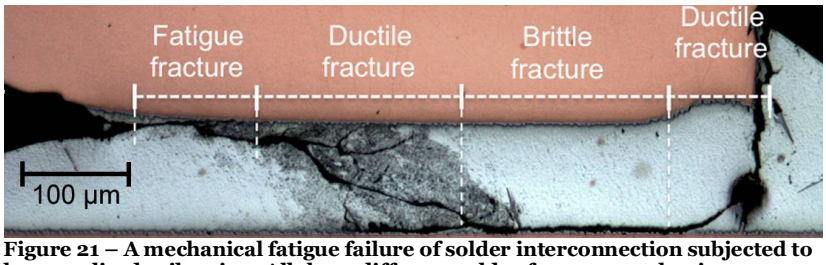


**Figure 21 – A mechanical fatigue failure of solder interconnection subjected to low amplitude vibration. All three different solder fracture mechanisms (fatigue, ductile and brittle) can be distinguished.**

### 5.2.5 Anisotropy

Tin has a highly asymmetric body-centric tetragonal crystal structure, which causes the individual tin grains within SnAgCu solder structure to have anistropical mechanical, electrical and thermal properties [Sub04, Tel03]. Therefore, the physical properties of individual solder joints may differ between each other depending on the orientations of the tin grains forming the solder joint. Furthermore, the differences in mechanical properties between adjacent tin grains may cause internal strain gradients when the solder interconnection is exposed to external loads.

## 5.3 Summary of observed SnAgCu solder interconnection behavior under combined reliability test cases

The microstructural evolution and changing mechanical properties of SnAgCu solder interconnections under individual and combined tests employing electrical, thermal and mechanical loads are collected in Table 11. Most of the interactions presented in the table are based on observations done within this work, but results of some combinations are also taken from literature published elsewhere. It is especially noteworthy that under some consecutively combined tests the reliability of solder interconnections is improved as compared with results from individual test cases.

**Table 11 – Reported microstructural and reliability effects of combined loads on board-level SnAgCu solder interconnections.**

| Preconditioning or primary test | Isothermal annealing | Steady-state electromigration testing | Power cycling | Thermal cycling |
|---|---|---|---|---|
| **Key load parameters** | Temperature | Current density, temperature | Current density, temperature cycle profile | Temperature cycle profile |
| **Effect on solder microstructure and mechanical properties** | | Formation of voids and hillocks: Reduction of load-bearing contact area | Recrystallization of solder grain structure: Formation of favorable paths for crack propagation | |
| | | Biasing of interfacial IMC layer growth: Reduction of interfacial IMC fracture toughness, loss of adhesion between contact metallization and solder | | |
| | Coarsening of solder cell structure, growth of intermetallic precipitates, growth of interfacial intermetallic layers: Reduction of solder bulk yield strength and ultimate tensile strength. Reduction of interfacial IMC fracture toughness. | | | |
| **References** | Publications I & II | | Publications III-V | Publications I & V |

| | | | | |
|---|---|---|---|---|
| **Effect of primary test on failure mode under vibration loads** | Crack path shift towards interface | Crack path shift towards bulk | Crack path shift towards interface (no recrystallization) or crack path shift towards recrystallized bulk | Crack path shift towards bulk |
| **Effect of primary test on vibration reliability** | Negative | Negative | Negative | Negative |
| **References** | Publication II | | Publication III | [Qio8, Eck10] |

| | | | | |
|---|---|---|---|---|
| **Effect of primary test on failure mode under mechanical shock** | Crack path shift towards interface | Crack path shift towards interface | Crack path shift towards interface (no recrystalli-zation) or crack path shift towards recrystallized bulk | Crack path shift towards solder bulk |
| **Effect of primary test on shock impact reliability** | Negative | Negative | Negative / Positive | Positive |
| **References** | [Peno7] | [Xuo6] | Publication IV | [Mato6] |

| | | | | |
|---|---|---|---|---|
| **Effect of primary test on failure mode under thermal cycling** | None | None | | |
| **Effect of primary test on thermal cycling reliability** | Negligible | Positive | | |
| | Publication I | | | |

# 6 Summary

In this work a physics of failure reliability assessment approach is presented based on the individual and cumulative reliability effects of thermal, mechanical and electrical loading conditions on electrical assemblies. The effectiveness of the approach has been demonstrated by assessing the reliability of board level SnAgCu solder interconnections under multiple board-level test conditions.

The physics of failure approach requires detailed information on the effects of different loading conditions on the behavior of the studied specimen. To meet this requirement, a set of consecutive and concurrent tests combining thermal, electrical and mechanical loads have been conducted on component board test assemblies. The test cases revealed that the severity of individual loads has to be carefully selected when combining multiple loads, as most standardized tests were too highly accelerated and led to artificial results. Additionally, the role of time- and temperature-dependent microstructural evolution of solder material became pronounced when assessing long-term reliability under multiple loading conditions. In order to successfully employ combined loadings in reliability assessments, the load profiles should be derived from the true service conditions of the product application. Therefore, product-level characterizations were conducted in publications V and VI.

The results of this dissertation provide insight in designing more comprehensive reliability tests as well as achieving higher levels of test acceleration without compromising the validity of results. It is shown that when executed carefully, the use of combined loading tests can yield impressive benefits in reduced testing times and aid in detection of potential reliability issues.

The thesis consists of six publications, of which the main results and conclusions are summarized as follows.

In Publication I, entitled "**Effect of Isothermal Aging and Electromigration on the Microstructural Evolution of Solder Interconnections During Thermomechanical Loading**" the effect of annealing and electromigration pre-aging treatments on the microstructural evolution of SnAgCu solder interconnections under thermal cycling was investigated. The results showed distinct differences in the microstructural changes between samples with no pre-treatment, samples that experienced thermal annealing and those, which have had DC-current stressing as the pre-treatment. The finite element method was employed to characterize the loading conditions imposed on the solder interconnections during cyclic stressing. The growth of intermetallic reaction layers were analyzed by utilizing quantitative thermodynamic calculations coupled with kinetic analysis. It was shown that the DC-current and thermal annealing pretreatments significantly influenced the behavior of the solder interconnections under slow cyclic loading. The slightly stronger effect of DC current stressing on the microstructural evolution could be rationalized by considering the influence of electron flow on the size and amount of IMC precipitates and eutectic structure inside the solder matrix. The interfacial reaction layer growth was also influenced by the flow of current.

Publication II, entitled "**Effect of isothermal annealing and electromigration pre-treatments on the reliability of solder interconnections under vibration loading**", presented the effects two pre-treatment methods, isothermal annealing and DC-current stressing, on the reliability of solder interconnections under vibration loading. The results showed that: (1) isothermal annealing and DC-current stressing both compromised the reliability of interconnections during testing in comparison to the samples without pre-treatment and (2) the crack propagation path through the interconnection changed as compared to the samples without pre-treatments. The experimental results were rationalized with the help of microstructural investigations and finite element (FE) analysis. The FE-analysis indicated that the highest stresses were experienced by interconnections consistent with the experimental results. The electromigration stressing and thermal annealing pre-treatments both softened the solder interconnections by inducing

microstructural changes, which was reflected in the reduced reliability under vibrational loading. The pronounced effect of electromigration stressing is attributed to the smaller amount of finely dispersed interdendritic eutectic structure in the interconnection after the treatment.

Publication III, entitled "**The effects of concurrent power and vibration loads on the reliability of board-level interconnections in power electronic assemblies**" concentrated on the effects of concurrent vibration and electrical power loads on the solder interconnections of a surface-mount power transistor package. Both cyclic and constant power loadings were separately combined with vibration over a wide amplitude range. Single load vibration and power cycling tests were conducted for comparison. In addition to lifetime analysis, the failure modes occurring under each test case were carefully studied from cross-sectional samples and the failure mechanisms were rationalized with the help of finite element calculations and microstructural analysis. A substantial reduction in interconnection lifetimes was observed in the combined load tests as compared with the lifetime under single load tests. The failure modes were dependent mainly on the amplitude of the mechanical vibration, which affected the strain distribution within the critical solder interconnections. Notable evolution was observed in the solder microstructures, which under some test cases even led to localized recrystallization.

In Publication IV, entitled "**The Combined Effect of Shock Impacts and Operational Power Cycles on the Reliability of Handheld Device Component Board Interconnections**", the combined effects of thermomechanical and shock impact loads on the board level interconnections of a high-density component board were studied. The used power cycling profile was derived from the operational cycle of the commercial device studied in the publication V. None of the test boards exposed to only power cycling loading failed during the full 15000 cycle (416 days) test period. The thermomechanical loading, however, affected the microstructure of the solder interconnections by (1) enhancing the growth of interfacial intermetallic compound layers and (2) driving the coalescence of intermetallic particles inside the solder bulk. These microstructural changes initially improved drop test reliability, but longer exposure time caused the drop reliability to deteriorate. The lifetimes and

failure modes of the test boards were found to be similar in concurrent and consecutive test combinations. The reliability trend was found to be the same for both board- and product-level tests.

Publication V, entitled "**Thermomechanical reliability characterization of a handheld product in accelerated tests and use environment**", investigated the thermal and mechanical loading conditions encountered by solder interconnections inside a commercial handheld device under operational power cycling (OPC) and standardized accelerated temperature cycling (ATC) tests. The results from FEA showed that the interconnection deformations during the OPC test were mostly in the elastic region of the solder material, whereas those during the ATC tests reached well into the plastic region. The lifetime test results were consistent with the FEA results, as the device failed due to solder interconnection fracture under the ATC conditions within 18 days of testing, but under the OPC conditions remained operational even after 460 days of continuous testing. Based on these results, it was concluded that thermomechanical loading alone does not cause major reliability concerns in these products and that the standardized ATC tests grossly overestimate the associated reliability risk.

Publication VI, entitled "**Shock impact reliability characterization of a handheld product in accelerated tests and use environment**", concentrated on the mechanical loading conditions encountered by solder interconnections inside a commercial handheld device during accidental drop to a concrete surface. These loading conditions were then compared with those induced under the standard JEDEC JESD22-B111 condition B board-level drop test. The results showed that, even though the test board design and supporting method had a marked influence on the loading conditions and lifetime of solder interconnections, the primary failure mode and mechanism remained the same in all the conducted test cases. It was further concluded that the shock impact loading conditions could be compared using three basic metrics: (1) the maximum component assembly strain rate, (2) the maximum assembly strain amplitude and (3) the damping of the assembly. The lifetime in the board-level tests as compared with the lifetime in product-level drop test was only 4% in case of the JEDEC board and 18% in case of the specialized board. The characterized

loading conditions leading to these results were similar to those published by other research groups.

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Reliability is an important factor to success in the global electronics market. In addition to loss of sales, product failure due to insufficient reliability can lead to life threatening situations in fields such as medical and avionic electronics. However, as modern products are required to withstand numerous loads for many years of service, it is becoming increasingly difficult to obtain a sufficient amount of reliability data within a reasonable amount of time.

The focus of this dissertation is on the development of a more realistic and efficient reliability assessment approach for electronic product applications. The studied loading conditions include combinations of mechanical, thermal and electrical loads. Improvements to contemporary reliability assessment methods are given based on results from multiple research projects. Although the presented results are centered on interconnection reliability, the general methodology can be applied on any electronic structure.

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