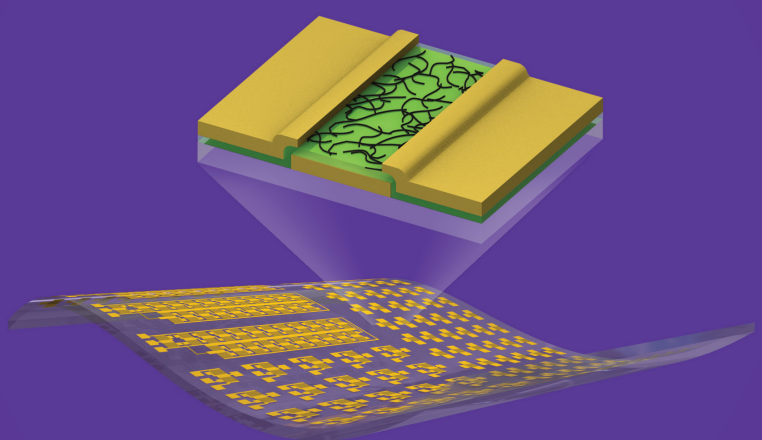
Department of Applied Physics

Carbon Nanotube Thin Film Transistors for Flexible Electronics

Marina Y. Timmermans (née Zavodchikova)



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Marina Y. Timmermans (née Zavodchikova)

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Abstract

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Abstract

The main objective of the emerging field of flexible macroelectronics is to develop scalable and cost effective routes to incorporate active circuit elements such as thin film transistors (TFTs) onto large-area flexible substrates. This dissertation reveals the promising potential of single-walled carbon nanotube (CNT) networks, synthesized using a floating catalyst (aerosol) chemical vapor deposition method, as an active layer material for TFTs. Direct dry or transfer printing techniques were developed for the deposition of as-grown CNTs in the form of random networks at room temperature and under atmospheric pressure onto any type of substrate, including heat-sensitive flexible materials. Patterned assembly of nanotubes and a lithography-free device fabrication technique were demonstrated. The results presented in this dissertation propose an alternative solution to remove existing manufacturing bottlenecks by capitalizing on the superb properties of pristine CNTs and minimizing the intermediate steps in the process flow between the nanotube synthesis and application, with the purpose of lowering manufacturing costs.

The CNT growth conditions were optimized to produce high-quality, long nanotubes (up to 10 μm) with a narrow diameter distribution (mean diameter around 1.1 nm). The nanotube network material was integrated directly from the gas-phase synthesis reactor into TFTs with the channel lengths up to 100 μm. The effect of network morphologies, obtained by four different aerosol-based nanotube deposition techniques, on device performance was studied. The results demonstrated that long, partially aligned nanotubes with larger junction area and controlled density exhibit superior characteristics. Optimized CNT TFTs showed simultaneously high on/off current ratio of 6×10^6 and carrier mobility of 35 $cm^2V^{-1}s^{-1}$ based on a parallel plate model for the gate capacitance estimation. When evaluated by a more rigorous analytical model, the highest mobility reached 1236 $cm^2V^{-1}s^{-1}$ with concurrent on/off ratio of 1.5×10^4, making these TFTs attractive for post-silicon technologies.

Successful operation of CNT TFTs and functional integrated circuits on flexible and transparent plastic substrates was shown. Future scalability of the fabrication process, for example, by using high-throughput printing techniques, opens new routes toward the realization of large-area flexible electronics.

Keywords carbon nanotube network, thin film transistor, aerosol synthesis, nanotube deposition, patterned assembly, morphology, flexible integrated circuit

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Espoo, July 2013
Marina Y. Timmermans

Contents

Thesis publications

This dissertation consists of an overview and the following publications (note, Marina Y. Timmermans published previously under her maiden name Marina Y. Zavodchikova):

I. Zavodchikova, M.Y., Nasibulin, A.G., Kulmala, T., Grigoras, K., Anisimov, A.S., Franssila, S., Ermolov, V., Kauppinen, E.I., 2008. Novel carbon nanotube network deposition technique for electronic device fabrication. Physica Status Solidi (b), 245 (10), 2272-2275

II. Zavodchikova, M.Y., Kulmala, T., Nasibulin, A.G., Ermolov, V., Franssila, S., Grigoras, K., Kauppinen, E.I., 2009. Carbon nanotube thin film transistors based on aerosol methods. Nanotechnology, 20, 085201

III. Sun, D., Timmermans, M.Y., Tian, Y., Nasibulin, A.G., Kauppinen, E.I., Kishimoto, S., Mizutani, T., Ohno, Y., 2011. Flexible high-performance carbon nanotube integrated circuits. Nature Nanotechnology, 6, 156-161

IV. Timmermans, M.Y., Grigoras, K., Nasibulin, A.G., Hurskainen, Franssila, S., Ermolov, V., Kauppinen, E.I., 2011. Lithography-free fabrication of carbon nanotube network transistors. Nanotechnology, 22, 065303

V. Timmermans, M.Y., Estrada, D., Nasibulin, A.G., Wood, J. D., Behnam, A., Sun, D., Ohno, Y., Lyding, J. W., Hassanien, A., Pop, E., Kauppinen, E.I., 2012. Effect of carbon nanotube network morphology on thin film transistor performance. Nano Research, 5 (5), 307-319

Author's contribution

I. The work was carried out in collaboration with the Microfabrication group at Aalto University and the Nanoscience Laboratory at the Nokia Research Center in Finland. The author of this dissertation carried out the majority of the research work, wrote the manuscript and corresponded with the referees of the paper.

II. The work was done in collaboration with the Microfabrication group at Aalto University and the Nanoscience Laboratory at Nokia Research Center in Finland. The author contributed greatly to all parts of the research work, carried out nanomaterial preparation, developed the deposition technique for integrating the material into devices, contributed significantly to device fabrication and electrical measurements in collaboration with the Microfabrication group, analyzed the results, wrote the manuscript and corresponded with the referees.

III. The work was done in collaboration with the Ohno group at Nagoya University in Japan. The author of the dissertation contributed to the research work by performing and optimizing nanomaterial preparation and characterization, discussing the techniques and results with the primary author on a regular basis, participating in device fabrication and electrical measurements during the research visits at different stages of the collaboration, and taking part in drafting, revising and correcting the manuscript.

IV. The work was done in collaboration with the Microfabrication group at Aalto University and the Nanoscience Laboratory at Nokia Research Center in Finland. The author is responsible for the majority of the work, carried out nanomaterial preparation, patterned assembly and characterization, contributed to the conceptual development and practical implementation of the fabrication technique proposed by the Microfabrication group, performed most of device fabrication and electrical measurements, wrote the manuscript and corresponded with the referees of the paper.

V. The work was done in collaboration with the Pop Laboratory and Beckman Institute at the University of Illinois in USA, the Ohno group at Nagoya University in Japan and the National Institute of Chemistry in Slovenia. The author planned the work, coordinated the international research cooperation, carried out nanomaterial preparation, developed most of the deposition methods, performed all the device fabrication and electrical characterization in collaboration with the Pop Laboratory during the research visit (apart from the noise measurements), analyzed the results (apart from the image processing with MATLAB), wrote the main part of the paper with contributions from co-authors, and corresponded with the referees.

Other publications

The author has also contributed to the following publications:

I. Sun, D., Timmermans, M.Y., Kaskela, A., Nasibulin, A.G., Kishimoto, S., Mizutani, T., Kauppinen, E.I., Ohno, Y. 2013. Moldable all-carbon integrated circuits. To be published in Nature Communications.

II. Vijayraghavan, A., Timmermans, M.Y., Grigoras, K., Nasibulin, A.G., Kauppinen, E.I., Krupke, R., 2011. Imaging conduction pathways in carbon nanotube network transistors by voltage-contrast scanning electron microscopy. Nanotechonology, 22 (26), 265715

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IV. Tian, Y., Timmermans, M.Y., Kivistö, S., Nasibulin, A.G., Zhu, Z., Jiang, H., Okhotnikov, O.G., Kauppinen, E.I., 2011. Tailoring the diameter of single-walled carbon nanotubes for optical applications. Nano Res., 4(8), 807-815

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aerosol method. Inorganic Materials: Appl. Research, 2 (6), 589-595. Published in Russian in Voprosy Materialovedeniya, 2010, 63 (3), 95-104

X. Rinkiö, M., Johansson, A., Zavodchikova, M. Y., Toppari, J., Nasibulin, A. G., Kauppinen, E. I., Törmä, P., 2008. High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric. New J. Phys., 10, 103019

XI. Rinkiö, M., Zavodchikova, M.Y., Törmä, P., Johansson, A., 2008. Effect of humidity on the hysteresis of single walled carbon nanotube field-effect transistors**.** Phys. Status Solidi (b), 245**,** 2315

XII. Zavodchikova, M.Y., Johansson, A., Rinkiö, M., Toppari, J.J., Nasibulin, A.G., Kauppinen, E.I., Törmä, P., 2007. Fabrication of carbon nanotube field-effect transistors for studies of their memory effects. Phys. Status Solidi (b), 244, 4188

Abbreviations and symbols

2D	two-dimensional
AFM	atomic force microscopy
ALD	atomic layer deposition
a-Si	amorphous silicon
c-AFM	conductive atomic force microscopy
CMOS	complementary metal-oxide semiconductor
CNT	carbon nanotube
CNTN	carbon nanotube network
CO	carbon monoxide
CPC	condensation particle counter
CVD	chemical vapor deposition
DF	dissolving the filter
DMA	differential mobility analyser
ESP	electrostatic precipitation
PEN	polyethylene naphthalate
PET	polyethylene terephthalate
PMMA	polymethyl methacrylate
poly-Si	polycrystalline silicon
PTF	press transfer from the filter
RIE	reactive ion etching
SEM	scanning electron microscopy
SWCNT	single-walled carbon nanotube
TEM	transmission electron microscopy
TFT	thin film transistor
TMA	trimethyl aluminum
TP	thermal precipitation
μ	charge carrier mobility
D	carbon nanotube network density
I_D	source-drain current
I_{OFF}	device off-state current
I_{ON}	device on-state current
L_{CNT}	carbon nanotube length
L_{ch}	device channel length
W_{ch}	device channel width
V_{DS}	source-drain voltage
V_{GS}	gate voltage

1. Introduction

After decades of steady and incremental progress, the field of electronic materials and devices is currently undergoing revolutionary changes. Innovative new materials with novel properties are poised to disrupt the world of conventional silicon-based semiconductor technologies, driven by the future demand for large-area, flexible and inexpensive devices. Rollable displays, active sensory skins and electronic textiles are just a few examples of such novel applications. Recently, carbon nanotube networks (CNTNs) have been proposed as a new class of material with superior properties for the emerging field of electronic systems that involve thin film transistors (TFTs) on large-area mechanically flexible substrates, often referred to as flexible macroelectronics. A CNTN is composed of a large quantity of electrically interconnected carbon nanotubes (CNTs) and presents a promising path for the realization of near-future flexible electronic applications, taking advantage of unique properties of individual CNTs while overcoming the manufacturing challenges of their precise assembly.

The fabrication of flexible TFT arrays is challenged by the trade-off between the processing temperature and device performance. The motivation behind this research work is to provide a potential solution to this problem, by developing a low-temperature process to prepare a high-quality, sub-monolayer CNTN as an alternative material to be integrated into flexible TFTs with minimized process steps. Compared with existing TFT channel materials, such as amorphous silicon and polycrystalline silicon, metal oxides or organic materials, CNTNs demonstrate the advantages of being compatible with cost efficient large-scale processing at room temperature, exhibiting high device performance and stability, and possessing the capability to enable novel device features such as high flexibility, transparency, and stretchability. The focus of this dissertation is to investigate the potential of random CNTNs, synthesized using a floating catalyst (aerosol) chemical vapor deposition method, as an active semiconducting material for TFTs.

One of the major advantages of aerosol-based CNTN formation technology is that the CNT synthesis is continuous and scalable. In addition, the deposition process is performed at room temperature directly from the ambient-pressure vertical flow aerosol reactor, in a quick and simple manner, and, hence, at potentially lower cost. Low-temperature material formation enables device fabrication on flexible plastic substrates that would melt at the high temperatures typically required for the manufacture of silicon-based transistors. Therefore, the final goal of this work is to demonstrate flexible CNT TFTs and integrated circuits. Future development of this technology is expected to enable the realization of scalable and continuous

routes to fabricate inexpensive, flexible electronic devices, possibly using high-speed roll-to-roll manufacturing processes. This dissertation contributes toward making the newly emerging field of flexible macroelectronics based on CNTNs a reality in the foreseeable future.

The structure of the dissertation is as follows. Following this introductory chapter, Chapter 2 describes the structure and electronic properties of single-walled CNTs, which are the fundamental components of a CNTN. Chapter 3 introduces the reader to a CNTN material, its formation techniques, electrical properties, and application as a semiconducting TFT channel. The details of the experimental work described in this dissertation, including nanotube synthesis and deposition technology, TFT fabrication and characterization techniques, are described in Chapter 4. Chapter 5 presents the main results of the experimental work. Floating catalyst (aerosol) technology for synthesis and deposition of CNTNs was suggested as an alternative method for CNTN formation, which allows to overcome existing manufacturing challenges. TFTs integrating as-synthesized CNTNs with optimized properties have been demonstrated, and show high performance. Successful operation of CNT TFTs and integrated circuits on flexible and transparent substrates is reported. Finally, the future prospects and challenges of integrating CNTNs as an electronic material are discussed. The final chapter presents the conclusions of the work.

2. Carbon nanotubes

2.1 An overview

CNTs are hollow, seamless cylinders of rolled-up one-atom-thick graphite sheet called graphene, with diameter of a few nanometers, and length from less than 100 nm up to several centimeters [1]. This material is one of the most exciting discoveries in materials science in the last 50 years [2]. The story of CNTs began as early as 1950s, when the development of electron microscopy techniques allowed the direct observation of their tubular structures, as was first shown by Radushkevich and Lukyanovich [3]. However, the outstanding electronic and optical properties of CNTs were yet to be discovered, and the applications were mainly focused on carbon-based composite materials [4]. It was not until almost four decades later that CNTs sparked world-wide scientific interest. Since the landmark publication of Iijima from the NEC Laboratories (Japan) in 1991, which recognized the scientific importance of these nanoscale objects [5], the nanotube field has been progressing at a breathtaking pace. Nanotubes of the type described by Iijima were made of several concentric cylindrical graphene shells, similar to the Russian Matrioshka doll, which became known as multi-walled carbon nanotubes (Figure 1 (a, b)). Two years later, Iijima and Ichihashi from NEC [6], and Bethune and colleagues from IBM Almaden Research Center [7] independently reported the experimental discovery of single-walled carbon nanotubes (SWCNTs), comprised of a single graphene layer wrapped to form a hollow cylinder (Figure 1 (c)). SWCNTs proved to have exceptional electrical, optical, and mechanical properties, which further motivated research in the field, making CNTs the subject of intensive study for a wide range of new, interesting applications. There has been significant worldwide growth in CNT-related commercial activity in the last decade, with current CNT production capacity exceeding several thousand tons per year [8]. Current commercially available products incorporating CNTs include rechargeable batteries, automotive equipment, sporting goods, ship hulls, thin-film heaters, membrane water filters, transparent conducting films for touch panels and many other applications with market opportunities continuing to expand [8]. This dissertation focuses on exploiting one of the potential SWCNT application areas for an emerging field of thin-film electronics. From this point, we will use the acronym CNT to refer specifically to SWCNTs, unless stated otherwise.

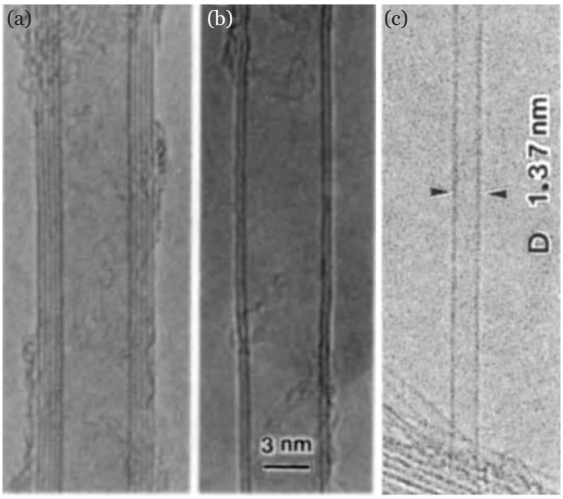


Figure 1 High-resolution TEM images of multi-walled and single-walled CNTs observed by Iijima in 1991 and 1993, respectively. (a) CNT consisting of five graphitic sheets, diameter 6.7 nm, and (b) CNT with two graphitic sheets, diameter 5.5 nm. © 1991 Nature Publishing Group. Reprinted with permission from [5]. (c) Single-sheet CNT, diameter 1.37 nm. © 1993 Nature Publishing Group. Reprinted with permission from [6].

2.2 Electronic properties of carbon nanotubes and transistor application

Before discussing the applications of CNTs, it is important to examine their microscopic structure and properties. CNTs are considered to be nearly one-dimensional (1D) structures, owing to their high length to diameter ratio. This unique 1D structure leads to reduced scattering and very high carrier mobility, with the possibility to achieve the near-ballistic transport regime. These outstanding properties of CNTs largely originate from the peculiar electronic structure of graphene. Figure 2 (a) shows the two-dimensional (2D) graphene sheet, the wrapping of which into a tubular form can be considered to conceptually construct a CNT. A nanotube can be described by a vector, called the chiral vector:

$$\vec{C} = n\vec{a}_1 + m\vec{a}_2,$$

where n and m are integers, $\vec{a}_1$ and $\vec{a}_2$ are the unit cell base vectors of the hexagonal honeycomb lattice. The chiral vector defines the circumference of the nanotube, and allows determination of its diameter d, as $|\vec{C}| = \pi d$. The tube axis is perpendicular to the chiral vector. The angle between $\vec{C}$ and $\vec{a}_1$ is called the chiral angle or angle of helicity (θ), which shows the tilt angle of the hexagons with respect to the direction of the tube axis. The nanotube structure can be uniquely described by the pair of integers known as chiral indices (n, m). All CNTs can be classified as chiral or achiral. Achiral CNTs, which can be superimposed with their

own mirror image, can be either armchair or zigzag, depending on the geometry of their circular cross-section. When the chiral vector lies exactly between the two unit vectors so that $n = m$, the CNT is called "armchair" ($\theta = 30°$). When the chiral vector follows one of the two unit vectors, so that $m = 0$, the nanotube is said to be of "zigzag" type ($\theta = 0°$). And otherwise, when $n \neq m$, the nanotube is called chiral ($0° < \theta < 30°$) (Figure 2 (b)).

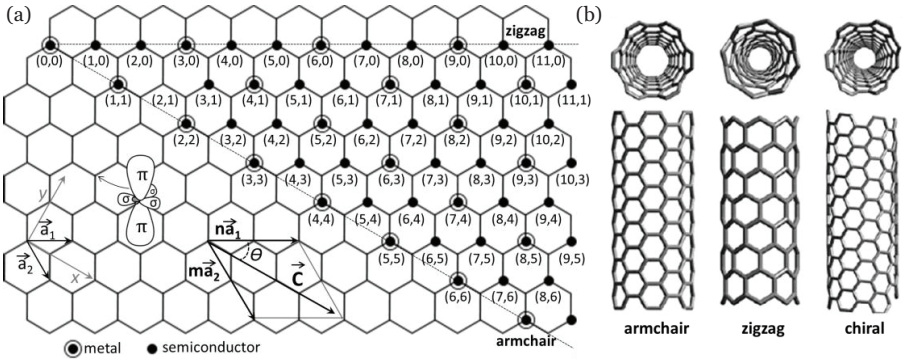


Figure 2 (a) Graphene honeycomb sheet with unit cell vectors $\vec{a}_1$ and $\vec{a}_2$. The chiral vector $\vec{C}$ represents a possible wrapping of the 2D graphene sheet into a tubular form. The circumference of a nanotube is given by the length of the chiral vector. The chiral angle θ is defined as the angle between the chiral vector and the zigzag axis. Inset: illustration of the formation of σ and π bonds from the sp^2 orbitals. (b) Models of SWCNTs exhibiting different chiralities.

The structure of a CNT is characterized by the so-called sp^2 hybridization, analogous to graphene. Of the four valence electrons in carbon atom (occupying the 2*s* and 2*p* orbitals), one of the 2*s* electrons hybridizes with two of the 2*p* electrons, forming three sp^2 orbitals at 120° to each other in a plane. The sp^2 orbitals create strong σ bonds between carbon atoms in the graphite plane. The σ bonds are responsible for the strength and mechanical properties of graphene and CNTs. The remaining $2p_z$ electrons form the π bonds, where the electron cloud is distributed perpendicular to the surface of the nanotube (see inset in Figure 2(a)). This π bonding gives rise to delocalized electrons, which are weakly bound to the nuclei and are responsible for the electronic properties of graphene and CNTs.

In order to obtain the electronic structure of CNTs, we need to take into account the confinement of electrons around the circumference of the nanotube when the graphene sheet is rolled into a cylinder. Such confinement of electrons in the nanotube restricts their motion to only two directions along the tube axis (forward and backward), which determines the unique electrical properties of CNTs. Thus, in a CNT the wavevector *k* is quantized along the circumferential direction due to the periodic boundary condition:

$$\vec{k}\,\vec{C} = 2\pi q\,,$$

where $\vec{C}$ is the chiral vector and q is an integer. Allowed energy states of the nanotube are determined by the specific values of $\vec{C}$ and q, which define parallel lines in reciprocal k space, continuous along the tube axis, but quantized along the circumference. Each line provides a one-dimensional energy sub-band by cutting the 2D graphene band structure. Figure 3 (a) shows the band structure and the hexagonal shape of the first Brillouin zone of graphene, as well as the allowed states of a (3, 3) nanotube as cuts of the graphene band structure. It can be seen in Figure 3 (a) that the valence and conduction bands of graphene touch at six points, Fermi points, lying at the Fermi energy.

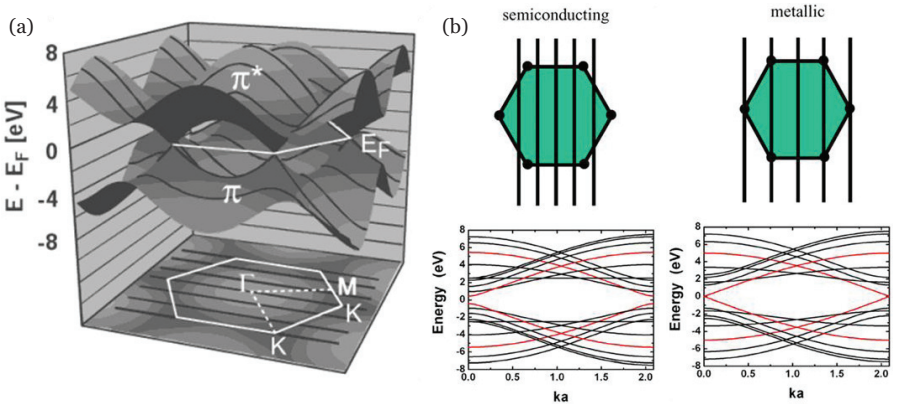


Figure 3 (a) Top: band structure of a 2D graphene sheet. Bottom: the first Brillouin zone of graphene. The black lines represent the allowed states of a (3,3) nanotube. They are cuts of the graphene band structure that are selected by quantizing the wavevector in the circumferential direction. © 2002 American Chemical Society. Reprinted with permission from [10]. (b) Top: illustration of the first Brillouin zone of graphene, and the allowed wavevector lines leading to semiconducting and metallic nanotubes. Bottom: examples of band structures for semiconducting and metallic zigzag nanotubes. © 2006 IOP Publishing. Reproduced by permission of IOP Publishing from [11]. All rights reserved.

One of the most important properties of CNTs, their ability to be either semiconducting or metallic, depends on whether or not the lines pass through the graphene Fermi points (see Figure 3 (b)). In the case when one of the lines of the quantized wave vector passes through one of the graphene Fermi points, the nanotube is metallic. When no lines intersect the Fermi points, the CNT is semiconducting, with the bandgap determined by the two lines that are closer to the Fermi points. The chiral indices n and m or, essentially, the orientation of the wrapped graphene sheet with respect to the tube axis, determine whether the lines pass through the Fermi points or not. This leads to the condition for the (n, m) CNT to be metallic when $n - m = 3i$, where i is a nonzero integer. All other CNTs are semiconducting, representing 2/3 of the as-grown nanotubes.

Metallic nanotubes have generated significant research attention due to their high current densities and outstanding mechanical properties, which are attractive

for application as interconnects [12, 13]. Semiconducting CNTs were proposed as promising active elements in field-effect transistors (FETs) [14-16]. Extensive studies on the transport properties of CNTs have been performed since the first demonstration of CNT transistors in 1998 [14]. It was shown that the performance of most CNT FETs is dominated by the gate modulation of the Schottky barriers at the electrode-nanotube interface, the heights of which are primarily determined by the energy difference of the work function of the metal contacts, and the conduction/valence band edge of the CNT [17, 18]. A significant research effort was devoted to reducing this barrier, and achieving ohmic contacts to semiconducting nanotubes. For example, contacting semiconducting CNTs by high work function palladium was shown to minimize the barriers for transport through the valence band of nanotubes, approaching the ballistic transport for short nanotubes [19].

From the application's point of view, unipolarity or ambipolarity of current-voltage characteristics is an important aspect of nanotube transistors. Earlier studies have shown ambipolar behavior in Schottky barrier CNT FETs under a vacuum environment or with a top gate electrode, when hole-carrier transport is permitted under the application of negative gate voltage, and electron-carrier transport at positive gate voltage (see Figure 4) [20, 21]. For the realization of CNT-based complementary metal-oxide semiconductor (CMOS) technology, one of the ambipolar regions of the CNT should be suppressed. For example, similar performance for p- and n-type CNT FETs with electron and hole mobilities of over 3000 $cm^2V^{-1}s^{-1}$ on the same undoped nanotube was demonstrated, therefore taking advantage of the intrinsic symmetry in the band structures of the CNT [22]. Typically, under ambient conditions electron conduction in unpassivated CNT FETs is suppressed, presumably due to oxygen or water adsorbates, which results in predominantly p-type behavior [23, 24]. In order to allow the nanotube devices to exhibit n-type behavior, various strategies have been adopted as recently reviewed in [25]. By careful design of the transistor threshold voltage, utilization of ambipolar behavior for CMOS-like logic circuits, without the need for doping processes, was also proposed [26].

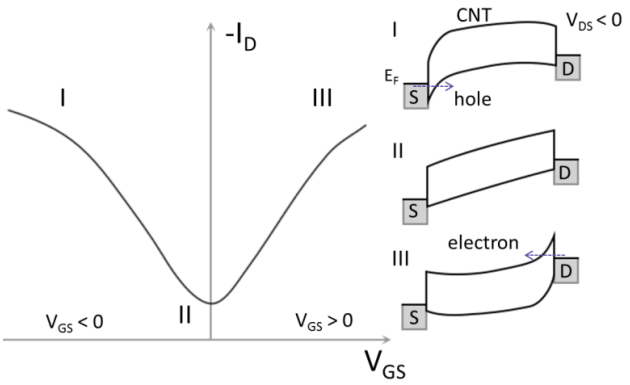


Figure 4 Schematic illustration of an ambipolar behavior of a CNT FET based on an individual semiconducting CNT. The diagrams demonstrate the bending of a nanotube valence and conduction bands near the nanotube/metal interface with respect to the applied gate voltage.

In general, individual CNTs have shown the potential to replace or supplement silicon technology. These nano-scale structures have shown mobility up to 79,000 $cm^2V^{-1}s^{-1}$ at room temperature, and a ratio of on-state current to off-state current of approximately 10^6–10^7 [27]. In 2012, the scaling behavior of CNT transistors to below 10 nm with superior low-voltage performance was first reported [28]. These impressive experimental results confirm the capability of individual CNTs to outperform silicon devices at extremely short lengths, allowing further miniaturization of electronic components. However, it should be noted that, despite the remarkable electronic, thermal, and mechanical properties of CNTs, integration of devices based on individual CNTs into commercially viable products has, thus far, had limited success. Controlled processing and scaling-up constitute the main production difficulties, due to the challenges of positioning single CNTs at desired locations, and the variability of nanotube electrical properties depending on their chirality and diameter. A realistic and cost-effective approach toward the realization of near-term practical applications is the use of systems comprising a large number of tubes in the form CNTNs, as discussed later in this dissertation.

2.3 Synthesis of carbon nanotubes

Inspired by the fascinating properties of CNTs, extensive efforts have been focused on the controlled synthesis of these man-made structures in larger quantities, in order to tap their full commercial potential and realize a viable CNT industry. CNTs can be synthesized through either physical or chemical methods.

Physical methods require high energy input for the evaporation of a solid carbon source, typically graphite. This can be achieved by either arc discharge or laser ablation. The *arc discharge* method is the simplest and most common method of nanotube synthesis, which led to the original discovery of CNTs. It involves the growth of CNTs during the direct current arc discharge evaporation of carbon from

graphite electrodes, in the presence of inert gas (helium or argon) at atmospheric or sub-atmospheric pressure [29]. The addition of metal catalysts is required for the synthesis of CNTs (typically Fe, Co, Ni, Y, or Mo) [30]. In the *laser ablation* synthesis method, a graphite target doped with a small amount of catalyst metal is vaporized, using a high-power laser in a reactor preheated to high temperatures. Therefore, physical CNT synthesis methods have high energy consumption, since they require high temperature for the evaporation of carbon from a solid carbon target (>3000°C). Even though these techniques produce reasonable yields of CNTs (~70%), the synthesized nanotubes are typically tangled into bundles, and the crude product also contains nanoscale impurities, making CNT purification a mandatory process step [31]. Therefore, chemical methods for producing CNTs are becoming increasingly favorable due to the number of potential advantages over the physical techniques, including scalability and relatively mild synthesis conditions for easier control over the growth process [30].

Chemical methods are based on the catalytic decomposition of carbon-containing precursors through chemical reactions, also generally known as chemical vapor deposition (CVD) processes. The main advantage of this technique is the growth of CNTs at essentially low-temperatures (~600–1000°C). In addition, chemical synthesis allows scaling-up to industrial production levels at a relatively low cost, with enhanced control over the morphology and structure of the produced nanotubes [32]. These reasons explain why the CVD method is currently widely used for commercial CNT production. Since chemical methods can be used either with or without a substrate, they can be classified into substrate-supported CVD and floating catalyst (aerosol-unsupported) CVD, respectively [33, 34]. In the *substrate-supported* method, carbon precursor decomposition and the growth of CNTs occur on the surface of catalyst particles located on a substrate. In the *floating catalyst* (aerosol-unsupported) method, CNT formation takes place on the surface of catalyst particles suspended in a gas, i.e., on aerosol particles. This technique is also known as the gas-phase CVD method. Thermal decomposition of ferrocene, commonly mixed with thiophene vapors, and dissolved in different carbon sources, is one of the most popular aerosol-unsupported CVD methods for the synthesis of CNTs. A prototype of such a synthesis reactor was demonstrated by Endo in the 1980s, for the growth of carbon fibers [35]. The first laboratory-scale demonstrations of aerosol CNT synthesis occurred in the late 1990s [36]. Catalyst and carbon sources are fed into the reaction region continuously, so CNTs can be grown continuously, which is very important for large-scale synthesis from an industrial perspective. Another advantage of aerosol technology is the direct collection of as-synthesized CNTs and the absence of support material, which further reduces the number of time-consuming process steps associated with nanotube purification and dispersion. This is why gas-phase production of nanotubes, known as the “HiPco” process (from high-pressure carbon monoxide

(CO)), developed by Nikolaev et al. in 1999 [37], is currently one of the most commonly used techniques for the commercial growth of bulk quantities of CNTs. The focus of this work is the application of CNT networks grown by aerosol technology which in contrast to the HiPco process, employs ambient pressure synthesis reactors with a laminar gas flow. The experimental details of CNT synthesis are described further in Chapter 4.

3. Carbon nanotube thin film transistors

3.1 The advent of carbon nanotube network macroelectronics

Silicon based electronics have shown significant progress over the last few years, characterized by an ongoing extension of Moore's law towards continuous miniaturization, increasing circuit density, and improving both cost and performance as device dimensions are reduced. In contrast to established silicon-based microelectronics, the development of large-area electronics or macroelectronics is driven by increasing the substrate size at lower cost, rather than device density [38].

TFTs are fundamental building blocks for state-of-the-art large-area electronics, the development of which was originally driven by flat panel display technology. Hidden behind glass plates and not typically visible to the device user, TFTs surround us in our daily lives, at home and at work, driving the displays of our mobile phones, computers, and large-area televisions. The history of the TFT is the longest among electronic devices. The first TFT patents were published in the 1930s by Lilienfeld [39] and Heil [40], suggesting the basic TFT operation principles, i.e. controlling the current flow in a material by means of a transverse electrical field [41]. After only a few decades, the first TFTs based on polycrystalline cadmium sulfide were produced [42]. At the end of the 1970s, after a period of decline in TFT development activity, the first demonstration of a TFT using amorphous silicon (a-Si) as the active material to drive a liquid crystal display (LCD) appeared [43]. At that time, a-Si turned out to be a suitable material that met the requirements of the LCD and existing manufacturing methods [44]. Later on, however, polycrystalline silicon (poly-Si) emerged as a substitute for a-Si technology for high performance devices. Figure 5 shows a schematic of the major milestones achieved in the history of TFTs.

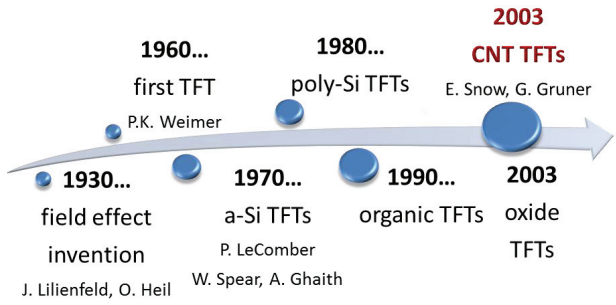


Figure 5 Schematic of the historic milestones achieved with TFTs.

A-Si and poly-Si are ubiquitous materials, currently used for TFTs in many commercial applications. Although it is one of the most economically significant semiconductors, a-Si has, however, relatively poor carrier mobility (less than 1 $cm^2V^{-1}s^{-1}$) and electrical instability, which limit the potential applications of this material [44]. A smaller fraction of TFTs, e.g., for small high-resolution displays, are currently made from poly-Si, which has higher mobility (around 100 $cm^2V^{-1}s^{-1}$) and degrades more slowly during the operational lifetime than a-Si, but suffers from high manufacturing costs and non-uniformity of the threshold voltage [44]. Moreover, silicon-based transistors typically require fairly high process temperatures and employ sophisticated vacuum processing, as well as possess limited flexibility and optical transmittance.

New materials therefore compete for entry into the mainstream, attempting to resolve existing challenges in conventional applications. Replacement of existing materials is the original driving force. At the same time, novel materials can offer unique characteristics capable of disrupting the world of silicon-based semiconducting technologies, and open doors to completely new applications and capabilities in the near future. Current TFT research is motivated by the emerging field of flexible macroelectronics, with lightweight, robust and inexpensive electronic products, which can be folded or rolled up for storage when not in use, as well as stretched or conformally wrapped onto arbitrarily curved surfaces. The development of the TFT technology with improved device performance and cost-effective fabrication methods compatible with flexible substrates, would open up a large number of novel macroelectronic applications, as shown in Figure 6.

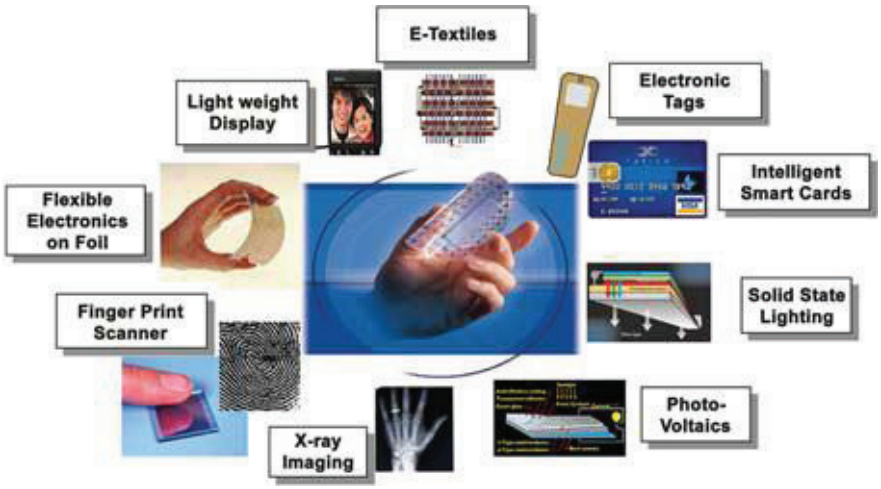


Figure 6 Applications enabled by flexible TFT arrays. © 2005 IEEE. Reprinted with permission from [38].

Low temperature processability and relatively high device performance are important features desired for the emerging flexible TFT technology. Simplifying the equipment and reducing the number of processing steps would open up the

prospect for lowering device manufacturing costs. That is why numerous research efforts are focused on the development of a semiconductor material that can be deposited onto a flexible plastic substrate using fast, low temperature and non-vacuum processes, and, at the same time, exhibit high charge carrier mobility. Organic semiconductors have been widely explored in recent years as promising materials for flexible electronics. The advantage with the organic materials is the possibility of low temperature deposition at low cost, using processing methods developed in the printing industry for large-area lightweight plastic substrates. In spite of a significant progress in recent years, performance of organic electronic devices is limited by a low mobility of charge carriers in organic materials. In addition, organic semiconductors exhibit processing difficulties due to their insolubility or air sensitivity under ambient conditions.

Recent studies have focused on integrating networks of CNTs into TFTs, with very promising outcomes for industrial scale-up. Since the first demonstration of TFTs with nanotube networks as the channel material, by Snow et al. [45] and Gruner et al. [46] in 2003, CNT TFTs have attracted extensive attention as promising building blocks for emerging flexible macroelectronics. CNT TFT technology offers valuable attributes such as high performance, low temperature processing and potential low cost. Figure 7 shows the general increase in the number of publications involving the application of CNTNs as a thin film electronic material starting from the year 2003.

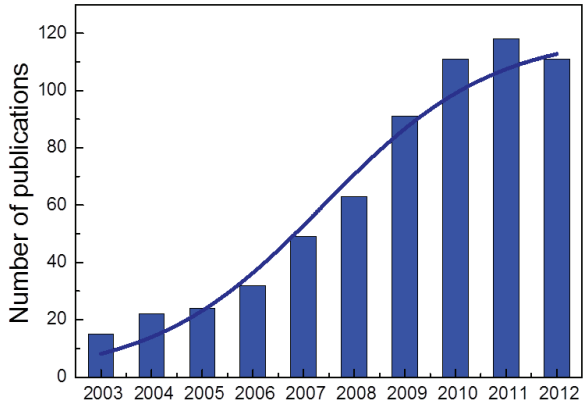


Figure 7 Growth trend in the number of publications on CNTNs as a thin film electronic material published annually from 2003. Data obtained from the ISI Web of Knowledge using a keyword search[1]. Note, online database for 2012 is not fully complete.

[1] Keyword search contains ("carbon nanotube") and (network or ensemble or "thin film") and (electronics or macroelectronics or "thin film transistor").

3.2 Carbon nanotube network as an electronic material

A CNTN material consists of electrically interconnected CNTs collectively behaving as a random web. By ensemble averaging over a large quantity of nanotubes comprising the network, variations in chirality and geometry between the individual tubes are reduced and better device reproducibility can be achieved [47]. A network with a random distribution of CNTs presents the most straightforward cost-effective way to realize such a material, electrically continuous over macroscopic dimensions.

Significant research efforts have been devoted to the development of large-scale alignment of CNTs [48-52]. CNT alignment enables high current outputs when multiple parallel individual nanotubes bridge source and drain electrodes, forming direct transport pathways. For example, Rogers et al. [53] have demonstrated integration of perfectly aligned CNT horizontal arrays into transistors and integrated circuits, where nanotubes were grown by CVD on a quartz wafer and later transferred to a flexible substrate. However, metallic CNTs in the as-grown nanotube array cause off-state leakage currents, and therefore additional procedures for their removal, e.g., electrical breakdown [54] or chemical functionalization [55, 56], are needed. This hinders practical applicability of such devices due to limitations in scalability, reproducibility, and possible device performance degradation. This is why random orientation of nanotubes within the network where individual CNTs do not directly bridge the source and drain electrodes is more attractive for obtaining high on/off current ratios when implementing electronically heterogeneous (1/3 metallic and 2/3 semiconducting) nanotubes.

An attractive feature of CNTNs is that they combine many of the unique properties of individual CNTs with the processing capabilities of mass fabrication methods [57]. Due to the high conductivity of its individual components, high conductivity of a nanotube network is expected, and mainly limited by tube-to-tube junction resistance [58]. CNTNs are compatible with large-area, low cost device fabrication techniques, such as transfer or printing methods. Similar to a spider web, a film of CNTs is a highly flexible material. Fault tolerance of CNTNs ensures the network operation by rearranging the pathways for the current flow in case of a break in one of the conducting paths within a network [58]. Thin CNT films are almost invisible to the eye owing to their high transparency. The combination of such unique properties of CNTNs provides possibilities for new applications, including flexible and transparent electronic systems.

A random CNTN material can behave as either metallic or semiconducting depending on the network density. As the density of CNTs in the network increases from a sparse coverage to a dense continuous coverage, the transport transitions from semiconducting to metallic behavior [59]. This is an interesting feature of

CNTNs which enables a wide range of applications ranging from lightweight, flexible and transparent conducting films to active electronic devices [60]. CNTN material with higher CNT density, also referred to as a "thin film", is at the forefront of material research aimed at replacing doped metal oxide films such as tin-doped indium oxide (ITO), currently widely used for transparent conducting electrodes in various optoelectronic devices. ITO has limited flexibility, and a depleted raw material supply, resulting in the continuous cost increase of indium [61]. In our laboratory, we have recently demonstrated a method to prepare and apply chemically-doped CNTNs that reach a sheet resistance of as low as 84 Ω/□ at 90% optical transmittance, characteristics superior to the typical performance of ITO on flexible polymer substrates [62]. In fact, CNT thin films as transparent conducting materials have already made the first steps towards commercial success [63]. Application of sparse monolayer or sub-monolayer random CNTN as the semiconducting component of electronic devices is the main focus of this dissertation. A number of key technological challenges still need to be overcome to integrate CNT TFTs in commercial products. As the next step toward the realization of highly flexible and stretchable devices, a number of reports have successfully combined both highly conductive CNT films as passive electrodes and interconnects, and lower density networks as active TFT channels [64-66].

3.3. Nanotube network formation techniques: progress and challenges

Since the first demonstration of random CNTN material as a transistor channel, significant efforts have been made in CNT TFT device research. One of the major bottlenecks on the path toward integrating CNTNs for flexible electronics is the development of low temperature material deposition techniques compatible with plastic substrates. Depending on the processing technique, there are two widely used approaches for the preparation of CNTNs at low temperatures for use in active electronic devices. Until now, CNTNs have been mainly produced by either localized synthesis processes on the catalyzed substrates (substrate-supported CVD growth) or by remote synthesis processes, depositing CNTs from their liquid suspensions (solution deposition methods).

Substrate-supported CVD is a widely used method for the growth of CNTs directly on the substrate. The CNTs that result from this process exhibit a high level of structural perfection, long average tube lengths, high purity and relative absence of tube bundles [67]. Among other advantages of this process is the possibility to control the tube density, morphology, alignment, and position to an extent that is not achievable with solution deposition [68]. By randomly dispersing catalyst nanoparticles, or patterning catalytic islands to control the roots of CNTs grown by CVD, parallel assembly of CNT devices at specific locations in the circuit

can be achieved [69]. High quality devices have been obtained using localized growth of CNTNs directly on the substrates [45, 53, 70-74]. However, high growth temperatures (600°C–1200°C), high vacuum, and a reactive environment, as well as possible undesirable by-products deposited on the substrate surface during the growth process, constitute the major challenges for the compatibility of this process with emerging plastic electronics applications. The first demonstration of a flexible CNT TFT in 2003 by Bradley et al. [46] employed a technique for the transfer of CVD-grown CNTNs from a silicon substrate to flexible polyimide support by means of lifting off CNTs attached to flexible films together with metal electrodes. There has been substantial effort to develop techniques for the transfer of sparse CNTNs, in a random or aligned configuration, from their growth substrates, typically high-melting-point semiconductors (e.g., silicon) or insulators (e.g., quartz), onto a wide range of heat intolerant flexible substrates for transistor applications. These techniques typically require the utilization of a certain transfer medium, e.g., polydimethylsiloxane (PDMS) stamps [75, 76], thermally activated adhesive tapes [77], or polymethyl methacrylate (PMMA) films [78]. It was found that a thin layer of metal (typically Au), coating as-grown nanotubes, can assist the transfer process, but requires, however, subsequent removal by chemical etching [75, 77]. Utilizing a transfer printing method of random CNTNs CVD-grown on SiO_2/Si wafers, Cao et al. demonstrated impressive pioneering research work on the fabrication of medium-scale CNT thin film integrated circuits on flexible plastic substrates [79]. In spite of high performance devices achieved with as-transferred CVD-grown nanotubes, the need for a suitable CNT transfer medium and associated laborious transfer processes, as well as possible complications with the nanotube transfer efficiency, uniformity, and contamination, could, to some extent, limit the large output and low cost of such methods.

Solution deposition methods, as opposed to direct CNT growth on the substrate, offer room temperature processing advantages, scalability and are compatible with a wide variety of large-area, flexible, and transparent substrates. CNTs are typically synthesized by one of several bulk methods, and then dispersed into aqueous surfactant solutions. Using this approach, nanotubes can be further purified, and sorted by length [80, 81], diameter [82], electronic type (metal/semiconductor separation) [50, 83], and even chirality [84, 85], prior to deposition. A detailed review on post-synthetic strategies for preparing monodisperse CNT samples is found in the paper by Hersam [86]. Current commercial availability of semiconductor-enriched CNTs facilitates their exploitation for TFTs, and, thus, development of various solution deposition methods. For an overview of the progress and prospects of semiconductor-enriched CNT random networks in devices, we refer the reader to recently published review papers by Rouhi et al. [87] and Wang et al. [88]. The most commonly used methods of depositing CNTNs from their liquid suspensions for TFT fabrication include: printing [89-92]; spin-

coating [50, 93]; vacuum filtration [83]; and spray- [94-96] or dip-coating [71, 97-99]. Other possible methods include, for example, evaporation self-assembly proposed by Engel et al. [51], and Langmuir-Blodgett or Langmuir-Schaefer techniques recently used by Cao et al. [100], which allow assembly of semiconducting CNTs into dense aligned arrays for high-performance TFT fabrication. An overview of various CNT thin film deposition methods can be found in the paper by Hur et al [59].

Printing CNTNs and simply immersing the substrate into the nanotube solution have attracted the most widespread interest for solution-processed TFTs, owing to the potential scalability of these techniques. Printing nanotubes allows targeted positioning of CNTNs within a reasonable resolution, suitable for large-area devices with moderate performance. In 2010, Ha et al. demonstrated flexible digital circuits, based on semiconducting CNTNs deposited using aerosol-jet printing, such as inverters, a 5-stage ring oscillator, and NAND logic gates [90]. A number of promising results have been reported recently, demonstrating fully printed CNT TFTs by the inkjet technique [89, 101-105], and their application as, for example, current switches for organic light-emitting diodes [91]. However, the fabrication speed of inkjet printing is relatively slow. The gravure printing technique, recently demonstrated for printing of CNT TFTs and integrated circuits by Noh et al. [92, 106], offers a more cost-effective approach for large-scale and high-throughput applications. However, the performance of as-printed devices requires further optimization.

Most of the solution-based deposition methods start with preparation of stable suspensions of CNTs. However, the process of obtaining well dispersed nanotubes, especially in larger concentrations for realistic applications, is complicated due to the tendency of nanotubes to aggregate, forming entangled structures of large bundles and ropes. This occurs because nanotubes are hydrophobic, and have smooth surfaces resulting in strong van der Waals bonding between them [107]. Typically, high power sonication of CNTs in surfactant-stabilized aqueous solutions is used to prepare homogeneous CNT dispersions, which results in nanotube length reduction and possible degradation of their electronic properties [108]. Thus, transistors that use solution-processed CNTs generally show inferior performance in comparison to CVD-grown nanotubes, due to possible structural defects induced as a result of purification and suspension procedures [109]. In addition, the solution deposition process presents some practical challenges in control of the CNTN uniformity over large areas. One example is a possible formation of ring stains when the ink droplet dries on a solid surface [103]. Therefore, substrate functionalization with amine-containing molecules or polymers, such as aminopropyltriethoxysilane (APTES) [50, 71, 103, 110] or poly-L-lysine [111], became a commonly used method to improve the adhesion of CNTs. Finally, due to the presence of additives around the nanotubes after solution

deposition, various sample cleaning methods are required for removing residual surfactant, which may degrade the electrical performance of nanotube devices [111-113]. Treatments at high temperature in air (above 180°C) for few hours, and subsequent rinsing with isopropyl alcohol (IPA)/deionized water [103], or vacuum annealing [111], have been shown to be the most effective. A schematic of a typical solution-based CNTN formation process flow is shown in Chapter 5.

Various current CNTN formation methods present unique opportunities and challenges. We have demonstrated a third approach to deposit CNTNs, based on the *floating catalyst* (*aerosol) method*, which provides an alternative solution to some of the major obstacles and limitations of the other two commonly used techniques. This CNTN preparation technology is presented in detail later in this dissertation (Chapter 4). A good review, categorizing all of the state-of-the-art nanotube network formation techniques into three main groups (solid-phase, liquid-phase and gas-phase), with focus on the applications in flexible TFTs, was recently published [114].

3.4 Electrical characteristics of carbon nanotube networks

3.4.1 Density dependence

A random network of CNTs represents a complex electronic system that can be characterized by different types of disorder, which are associated with a large number of conducting pathways separated by randomly distributed charge transfer barriers at the nanotube junctions, with various barrier heights [115]. In order to interpret the mechanism of conduction through a network of CNTs, a CNTN is commonly approximated as a 2D random network of straight conducting sticks, which form the channel between the source and drain electrodes of the TFT. This network is electrically conducting if the density of conducting sticks exceeds a percolation threshold. A percolation threshold is the minimum density at which at least one continuous conducting path is formed between two points in the network [45, 116]. A simplified picture for CNTNs is that charge flows along the nanotube as far as possible, and has to transfer onto the next nanotube at the point of contact between two sticks [117]. The conductivity of a random network of sticks near the percolation threshold, D_{perc}, can be described by the following scaling law:

$$\sigma \propto \left(D - D_{perc}\right)^{t},$$

where σ is conductivity, D is the density of sticks, and t is a dimensionless index determined by the spatial arrangement of CNTs in the network (t=1.33 for an ideal theoretical film in two dimensions, and t=1.94 in three dimensions) [118]. For an infinite 2D homogeneous percolation network, D_{perc} obtained from numerical simulations is expressed as

$$L_S\sqrt{\pi D_{perc}} = 4.236,$$

where L_S is the length of the sticks [119]. Due to the large aspect ratio of CNTs (L_{CNT}/d>1000), very low CNTN densities are needed to achieve the percolation threshold. However, the results of classical percolation theory are only relevant for homogenous (constant conductivity), infinite-sized samples, with perfect tube-to-tube coupling. Conductivity in random CNTNs is, however, a more complex phenomenon, not readily explained by the classical percolation theory of conducting sticks. Alam and colleagues have devoted significant research efforts to generalizing the stick-percolation model to be applicable for interpreting the performance of finite-sized percolating CNTNs used in TFTs [117, 120, 121].

Our study has focused on thin nanotube networks with the device channel length *(L_{ch})* larger than the nanotube length *(L_{CNT})*, consistent with macroelectronics applications. For long channels, L_{ch}»L_{CNT}, there are no tubes that directly bridge the source and drain electrodes [120]. In this case, percolative transport is the dominant conduction mechanism, where charge carriers percolate from source to drain through the network of many parallel conducting paths, each consisting of multiple nanotubes in series, and tube-to-tube contacts play a significant role. In order to apply CNTNs in devices, it is important to consider how electrical properties of CNTNs depend on nanotube and device parameters in the regime of percolating conduction. Stick-percolation theory anticipates that for a device based on a network of sticks with uniform density, the drain current follows the finite size scaling relationship [121]:

$$I_D \propto \frac{1}{L_S}\left(\frac{L_S}{L_{ch}}\right)^m.$$

The scaling exponent m is a universal constant, which depends only on the areal stick density D, and stick length L_S, as $m(DL_S^2)$. m decreases monotonically with increasing DL_S^2 [122]. At high density, the network behaves as a classical 2D conductor, with most of the sticks participating in transport, and $m=1$; therefore the drain current is inversely proportional to the channel length (Ohmic behavior). On the other hand, when the network density approaches percolation threshold, not all of the sticks continue to be involved in the current carrying process from source to drain, and unconnected areas are formed. They start to arrange new percolating paths as the channel length is reduced, effectively increasing the channel width. Therefore, the current increases faster with L_{ch} than the classical scaling law, i.e., $m>1$ [122]. The form of the power law observed experimentally may vary due to a number of factors, including heterogeneity in tube electronic properties, tube-to-tube contact strength, CNTN morphology (curled or twisted CNTs instead of straight sticks assumed in the model), and variation of CNT lengths in the network [123].

The coexistence of both metallic and semiconducting nanotubes in CNTNs adds complexity to the understanding of their transport properties. Current CNT synthesis methods typically yield a mixture of metallic and semiconducting nanotubes. Therefore, control over the density of heterogeneous CNT networks is critical for device applications. In a TFT integrating higher density CNTNs, conducting paths through metallic nanotubes are formed with finite probability, resulting in a drastic increase in the off-state current. In this case, metallic CNTs can directly short the source and drain electrodes. Therefore, transport through interconnected metallic nanotubes will diminish the device on/off ratio, yet enable high on-state current capability and charge carrier mobility. In contrast, decreasing the network density in the channel would enable higher on/off ratios to be achieved, but, in contrast to thicker CNTNs, on-state current and mobility will be lower. This leads to a trade-off between charge carrier mobility and on/off ratio in CNT TFTs. An optimized device is expected to have a total density of CNTs (D_{CNT}) above the percolation threshold (D_{perc}), but a density of metallic CNTs (D_M) below the percolation threshold, as shown schematically in Figure 8 (a) in contrast to Figure 8 (b), so that the transport is mainly dominated by percolation along semiconducting CNTs [123, 124].

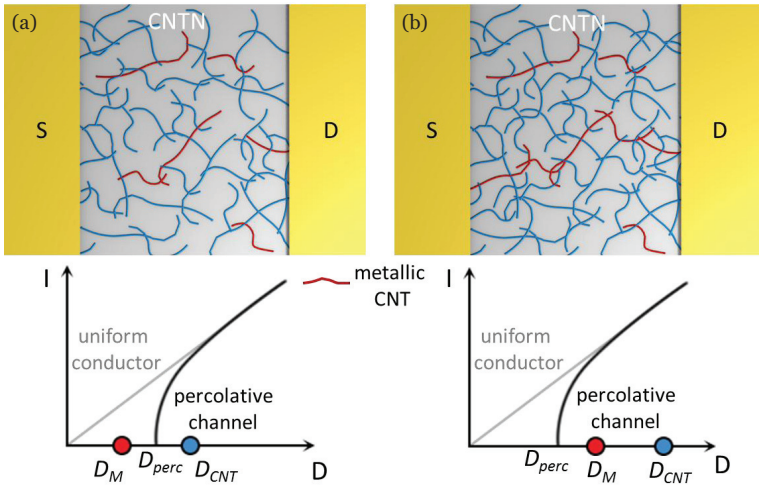


Figure 8 Schematics illustrating the CNTN as a transistor channel, with the total density (D_{CNT}) above the percolation threshold (D_{perc}), but (a) the density of metallic nanotubes (D_M) below D_{perc}; and (b) the density of metallic nanotubes above D_{perc}. The panels below schematically show the current variation with the changing nanotube density for the uniform conductor and percolative CNTN channel, for which the formation of at least one continuous electrical path is required for the conduction ($D_{CNT} > D_{perc}$).

3.4.2 Nanotube geometry dependence

Conductivity of a CNTN is generally expected to have a power law dependence on the average length of the CNT, i.e., $\sigma \propto L_{CNT}^{\alpha}$, with α varying from zero for negligible junction resistance between the tubes, to 2.48 for the dominating

junction resistance, according to simulations on networks of randomly distributed conducting sticks near percolation [125]. Conductive atomic force microscopy (c-AFM) studies on nanotube networks observed a sharp decrease in the conductance at the junction between nanotubes, revealing the dominating role of junctions in overall network resistance [126-129]. In agreement with the experimentally observed model where the junction resistance between tubes is much higher than the on-state resistance along the tube, Hecht et al. found that $\sigma \propto L_{CNT}^{1.46}$ for solution-deposited laser ablated tubes [125]. This indicates that longer CNTs are favorable to reduce the number of nanotube junctions within the network. The resistance of the tube itself is expected to be comparable to the junction resistance when the tube length approaches 20–30 μm taking into account the experimentally observed CNT resistance scaling with length at around 6 kΩ/μm [125, 130].

Typically, all CNTN formation techniques produce bundles of CNTs with various bundle diameters (D_b), since CNTs tend to aggregate due to the van der Waals interactions. The conductivity of a network is expected to vary as $\sigma \propto D_b^{-\beta}$, with β=2 as the upper limit to the exponent [125]. The role of debundling in controlling the performance of CNTNs was studied experimentally by means of c-AFM [129, 131], however no studies of nanotube junctions considering the gating effect are available yet. It is important to note that the presence of a metallic CNT stacked in a bundle with a semiconducting CNT may lead to an unfavorable electrostatic screening effect frustrating the gate modulation of the adjacent semiconducting nanotube which influences the device on/off ratio [132]. Considering individual nanotube diameter comprising the CNTN within the TFT channel it was suggested that narrow diameter CNTs provide improved device performance in terms of on/off ratio [133]. Moreover, as discussed in this dissertation, the Y-type CNT intermolecular junction morphology is favorable in terms of reduced contact resistance, in comparison with X-type junctions.

3.5 Thin film transistors integrating a carbon nanotube network

3.5.1 Operation mechanism

The structure of a CNT TFT consists of three main parts: a CNTN layer as a semiconducting channel, three electrodes, and a dielectric layer. The source and drain electrodes directly contact the CNTN, while the gate electrode is separated from the CNTN by a thin dielectric film. CNT TFT is a three-terminal device. Depending on the application purposes and performance requirements, different CNT TFT architectures are used, determined by the location of the gate (bottom-gate or top-gate), as well as the location of the source and drain electrodes (below or on top of the semiconductor material). Bottom-gate TFT structures, where a

CNTN is deposited on top of a gate electrode and dielectric, are the most straightforward to fabricate and are widely used as a simple platform for characterizing and comparing the properties of CNT TFTs.

The voltage applied to the gate electrode controls the current flow between source and drain electrodes. Metallic CNTs are conducting at all gate voltages, while the conductivity of semiconducting CNTs can be modulated by the gate in a TFT. Upon application of a transverse electric field to the network, semiconducting tubes become electrostatically doped, increasing the amount of percolating pathways within a network, and, thus, both metallic and semiconducting CNTs participate in the channel conduction [134].

Typically CNT TFTs exhibit predominantly p-type behavior in an ambient environment, in which case the charge flow in the transistor channel is dominated by holes (positive charges). In this case, charge will be allowed to flow between source and drain when a negative voltage is applied to the gate. The standard FET model is widely used to describe the operation of TFTs. At low source-drain voltage (V_{DS} <(V_{GS}–V_{th})) when the applied gate voltage (V_{GS}) is above the threshold for conduction in the channel ($V_{GS}>V_{th}$), the source-drain current (I_D) increases linearly with V_{DS}, and can be approximated by:

$$I_D = \frac{W_{ch} C_g}{L_{ch}} \mu (V_{GS} - V_{th}) V_{DS} .$$

Here, C_g is the gate capacitance per unit area, μ is the device mobility, L_{ch} is the channel length, and W_{ch} is the channel width. The value of mobility (μ) in this linear regime can be calculated from the transconductance (g_m):

$$g_m = \left(\frac{dI_D}{dV_{GS}} \right)_{V_{DS}=const} = \frac{W_{ch} C_g}{L_{ch}} \mu V_{DS} .$$

This formula is commonly used to calculate the device mobility of CNT TFTs, which also includes such device-specific effects as contact resistance between the semiconductor material and the electrodes etc. [27, 135]. In this traditional approach the CNTN is treated as a homogeneous bulk material as discussed further in this chapter. At larger V_{DS} values (V_{DS} >(V_{GS}–V_{th})) the device current reaches the saturation region, given by the equation:

$$I_D = \frac{W_{ch} C_g}{2L_{ch}} \mu (V_{GS} - V_{th})^2 .$$

C-AFM studies have revealed that modulation of the junction resistance at the contact between CNTs dominates the operation of TFTs based on sparse random networks [128, 129]. Since the networks typically consist of both metallic (M) and semiconducting (S) nanotubes, M–M, M–S and S–S junctions are expected to contribute to the overall junction resistance. Fuhrer et al. have shown that metallic tubes make relatively good contact with each other (M–M junction), and semiconducting tubes contact well to other semiconducting tubes (S–S junction),

with the junction resistance about 200–400 kΩ at low bias voltage [136]. The contact between metallic and semiconducting nanotubes is about two orders of magnitude more resistive [136]. This is due to the Schottky barrier, expected to form at the junction between a semiconducting and a metallic CNT, which would modulate the conduction between the tubes (M–S junction), as well as through the semiconducting tube itself (M–S crossing) [137, 138]. The presence of isotype p–p heterojunctions at S–S crossings between nanotubes with different bandgaps within a network was later shown experimentally [139].

The operation of CNT TFTs is therefore explained by both gate modulation of the Schottky barriers between metallic and semiconducting nanotubes (M–S junctions), as well as modulation of the semiconducting tube conductivity itself, by either controlling the charge carrier concentration, or by modulating the current flow through the Schottky barriers in semiconducting tubes formed by overlaps with metallic tubes (M–S crossings) [137]. It was shown that the resistance at the contact between the CNTN and the metal electrodes plays a less significant role in determining the transport of random CNTN TFTs compared to channel resistance, in contrast to transistors based on individual nanotubes [140].

3.5.2 Performance characteristics

The geometry of the CNT TFT is defined by the channel length (L_{ch}), width (W_{ch}), and the thickness of the gate insulator (t_{ox}). CNT TFT characteristics are commonly benchmarked with other technologies by evaluating the device mobility, μ (a measure of how fast the charge carriers in a device can travel within the semiconductor material under an electric field), and the ratio between device on-state current, I_{ON}, and off-state current I_{OFF} (a measure of how efficiently the current can be modulated by the gate voltage). The goal is to achieve larger values for these performance metrics simultaneously. Besides high mobility and on/off ratio, to manufacture high-performance devices based on CNT TFTs it is important to obtain high on-state current levels per micron of gate width (current density), steep sub-threshold slope, and uniform threshold voltage, as well as good stability and uniformity of TFT performance. The gate capacitance coupling between a planar electrode and a CNTN is critically important for transistor operation and device performance estimation [141]. Higher capacitance enables lower operating voltages, which is important for practical applications. Typically, a CNTN is treated as a classical thin film material for which the gate-to-channel capacitance is evaluated as:

$$C_{g,p} = \varepsilon_0 \varepsilon / t_{ox},$$

where ε_o is the vacuum permittivity, and ε is the relative dielectric constant of the gate insulator (so-called *parallel plate* model, Figure 9 (a)). This method enables a simple and approximate evaluation of the device performance level, but results in overestimation of the gate capacitance for low density networks. As such, the

device mobility values appear to be underestimated. For the case of a parallel plate model, the current scaling exponent *m,* introduced earlier, is assumed to be one, i.e., $I_D \sim C_{g,p}/L_{ch}$, as for the continuum thin film material. When sub-monolayer CNTNs are used as a semiconducting material for the transistor, where the average spacing between CNTs is large compared to the thickness of the gate insulator, the gate capacitance per unit area is lower in comparison with continuous, planar channels. In the case of low surface coverage, electrostatic coupling between sparse CNTs and the gate electrode is enhanced because the electric force lines are focused on the nanotubes, which have diameters in the nanometer range [140]. Cao et al. have introduced an analytical expression for the gate capacitance, which depends on the linear density of CNTs (tube-tube separation, Λ_o), diameter of the nanotubes (average tube radius, R), distance between the gate and the channel (oxide thickness, t_{ox}), and the intrinsic quantum capacitance of nanotubes ($C_Q \sim 4.0\times10^{-10} F/m$ [142, 143]) (the so-called *rigorous* cylindrical model, Figure 9 (b)) [141]:

$$C_{g,r} = \left\{ \frac{1}{2\pi\varepsilon_0} \ln\left[\frac{\Lambda_0}{R} \frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi} \right] + C_Q^{-1} \right\}^{-1} \Lambda_0^{-1}.$$

It is worth noting that this equation was obtained for aligned arrays of CNTs, but can also be used as a qualitative guide for a more accurate determination of mobility for random CNTNs. Capacitance-voltage (C–V) measurements for the direct evaluation of the gate capacitance of a flexible CNT TFT, and, as a result, a more accurate device mobility estimation in comparison with the above described models, was recently demonstrated [144, 145].

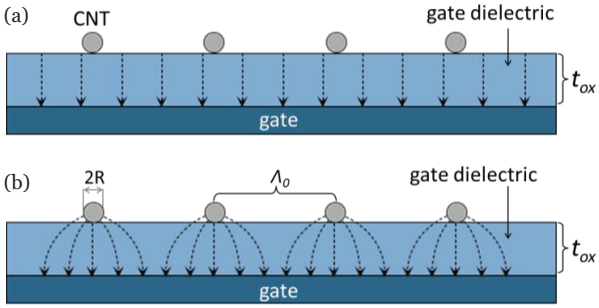


Figure 9 Schematics of a device cross-section and electric field lines corresponding to (a) parallel plate model and (b) rigorous model for the gate capacitance estimation.

High device on/off ratio (low off-current) is an important parameter for the application of CNT TFTs in display pixel switching or their integration in logic circuits. Low device on/off ratio would lead to poor contrast and result in static power consumption, which is detrimental for larger-scale integration. For certain macroelectronic applications, a large on/off ratio in transistors is more important than high on-state current values [146]. The presence of metallic nanotubes will

reduce the device on/off ratio, as metallic CNTs are always on, even when the device is in the off-state. Therefore, increasing the density of heterogeneous CNTs increases the probability to form continuous all metallic tube paths between source and drain. This results in the decrease of the average device on/off ratio, with a significant drop around the percolation threshold of metallic CNTs in the network [123].

In the device on-state, the total network density is defined by both metallic and semiconducting CNTs which participate in charge transport, while in the off-state, the current only flows through metallic nanotubes and the effective network coverage becomes $\sim DL_S^2/3$. This is why the experimental current exponent m, which scales roughly inversely with the network coverage DL_S^2, will be different for on- and off-states of the device, i.e., $m_{on}<m_{off}$ [122]. Therefore, the on/off ratio of the device increases with the exponent ($m_{on}-m_{off}$) as a function of the channel length, L_{ch}:

$$I_{ON}/I_{OFF} \sim (1/L_{ch})^{m_{on}-m_{off}}.$$

For lower density networks, the I_{ON}/I_{OFF} dependence on L_{ch} increases rapidly in comparison with the higher density networks, for which m is relatively constant [122].

Finally, alignment of CNTs in a network is an important parameter that enables higher current outputs, as increased alignment of nanotubes along the TFT channel reduces the number of tube-to-tube junctions. However, for long channel devices (in comparison with CNT average length) there is an optimal alignment level that depends on device geometry. Increasing the degree of alignment actually reduces the probability of forming percolating pathways between source and drain electrodes. Therefore, in certain cases a random network configuration was shown to be close to optimal [147].

4. Experimental methods

4.1 Synthesis method

The CNTs that form the networks described in this work were synthesized using an ambient pressure floating catalyst (aerosol-unsupported or gas-phase) CVD method [148]. The experimental setup consists of a precursor feed system, a furnace with a ceramic tube (22 mm internal diameter), and CNT collection/analysis devices, as shown in Figure 10. The vertical furnace configuration is employed for the continuous production of CNTs. The CO carbon source and the ferrocene catalyst precursor are injected at the top of the furnace, and the nanotube material is collected at the bottom of the reactor.

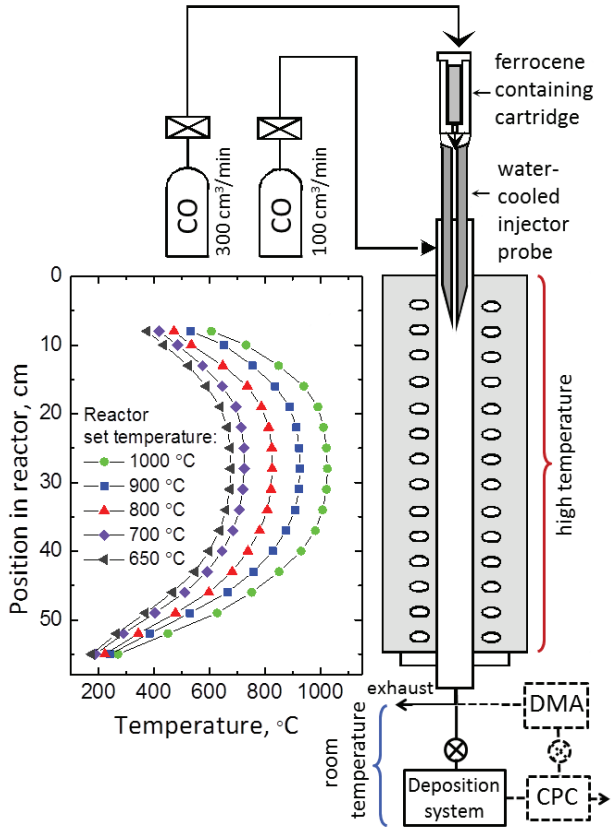


Figure 10 Schematic representation of the experimental setup along with the reactor wall temperature profile as a function of the set temperature. Water-cooled probe is inserted 6.5 cm deep in the reactor. The temperature profiles were measured by positioning a K-type thermocouple (SAB Bröckskes GmbH and Co., KG, Germany) at various locations in the reactor.

Carbon precursor decomposition and the growth of CNTs occur during flight, on the surface of catalyst particles suspended in a flow of carbon-containing gas at elevated temperatures. Therefore, the term 'floating catalyst' is used. The iron catalyst particles for nanotube growth are produced by thermal decomposition of ferrocene vapour ($Fe(C_5H_5)_2$, 99%, Strem Chemicals) in a CO atmosphere. Ferrocene is vaporized by continuously passing a flow of CO (with a flow rate of 300 cm^3min^{-1}) through a cartridge filled with a mixture of powdered ferrocene and silicon dioxide (as the inert filler) at room temperature. The flow containing ferrocene vapor (partial vapor pressure 0.7 Pa) is then introduced into the high temperature zone of the reactor through a stainless steel water-cooled injector probe, and mixed with an additional CO flow (flow rate 100 cm^3min^{-1}). The water-cooled injector probe is maintained at 24°C with the outlet located inside the heated furnace, which ensures the large temperature gradient necessary for fast heating of the vapor-gas mixture and production of catalyst particles. The position of the injector probe with respect to the furnace inlet was optimized, and kept constant at 6.5 cm during the growth of CNTs for this study [149, 150]. The set temperature of the reactor furnace was varied in the range between 650°C and 1000°C. The maximum wall temperature of the reactor depends on the probe position and is about 25°C higher than the set temperature for the probe position of 6.5 cm, determined based on the thermocouple measurements inside the reactor (see Figure 10). Further we use the measured maximum wall temperature to describe the synthesis temperature in our study.

CNTs, formed on the surface of the catalyst particles, are carried by a CO flow in the downward direction, and instantaneously collected at the outlet of the reactor. The collection is performed at room temperature either directly onto the substrate of interest or filtered through a membrane filter for subsequent transfer, as described in more detail in the following section. Collection of the synthesis product directly from the gaseous phase, rather than peeling off CNTs from the cooler parts of the furnace, is a significant advantage of our aerosol synthesis system, providing a continuous growth process [34, 151]. An on-line technique utilizing a differential mobility analyzer (DMA, TSI 3081) and a condensation particle counter (CPC) was employed prior to CNTN deposition in order to detect the CNT formation and distinguish nanotubes from catalyst particle aggregates [148]. This method allows to receive a direct feedback to the synthesis process and find optimal conditions for the CNT growth [33].

4.2 Carbon nanotube network deposition techniques

We have developed four methods to effectively deposit CNTNs directly from the gas-phase synthesis reactor at room temperature. Figure 11 illustrates the deposition techniques used in our study.

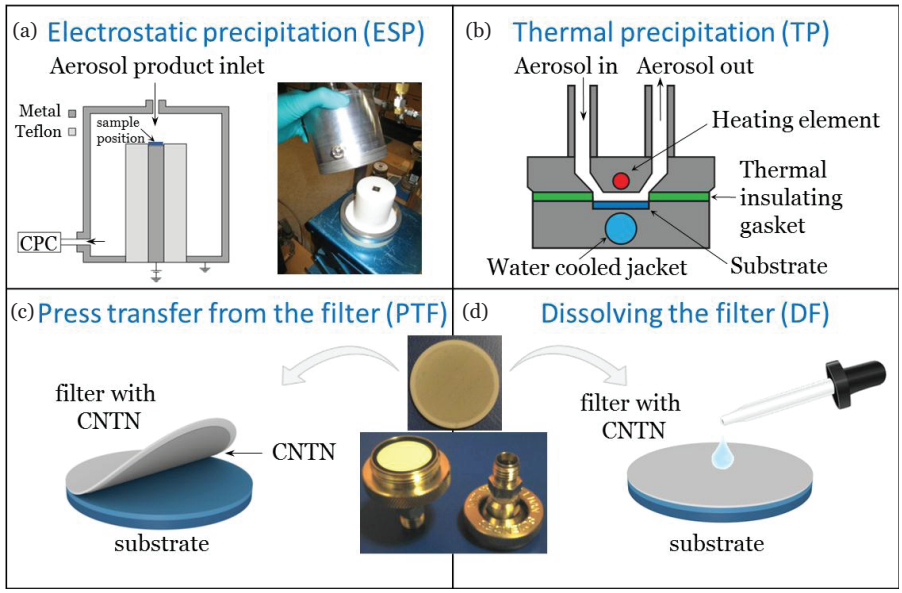


Figure 11 Schematic illustration of the four CNTN deposition methods, which largely define the morphology of the network at fixed synthesis conditions: (a) electrostatic precipitation (ESP); (b) thermal precipitation (TP); (c) press transfer from the filter (PTF); (d) dissolving the filter (DF).

The first method is a dry deposition technique which guides aerosol-synthesized CNTs in an electric field directly to the substrate by means of electrostatic precipitation (ESP). An ESP is a highly efficient collection method widely used in aerosol sampling, which we have applied for collecting CNTs for the first time (Publications I and II). The novelty of this technique is the improved efficiency of CNTN deposition directly from the synthesis reactor, by means of an electric field. The collection is performed at room temperature, allowing the use of heat-sensitive substrates. As-grown CNTs are carried downstream of the furnace by a CO flow, where they are collected using the ESP technique. This collection process is possible due to the spontaneous charging phenomenon of CNTs during their bundling in the gas-phase (92–99% are charged with up to 5 elementary electrical charges), which was discovered at the outlet of the floating catalyst (aerosol) reactor [152, 153]. Figure 11 (a) schematically illustrates the ESP-based deposition method. An electrostatic precipitator is a cylindrical chamber with an inner horizontally-positioned metal electrode, where the substrate is placed [154]. Application of a constant negative electric field between this electrode, surrounded by an electrical shielding, and the cover of the precipitator, allows guidance of positively charged CNT bundles towards the substrate surface. In the same way, a positive electric field can be used to guide negatively charged bundles. Without application of an electric field, CNTs in a gas flow tend to go around the substrate, leaving very few nanotubes on the surface, as seen in Figure 12.

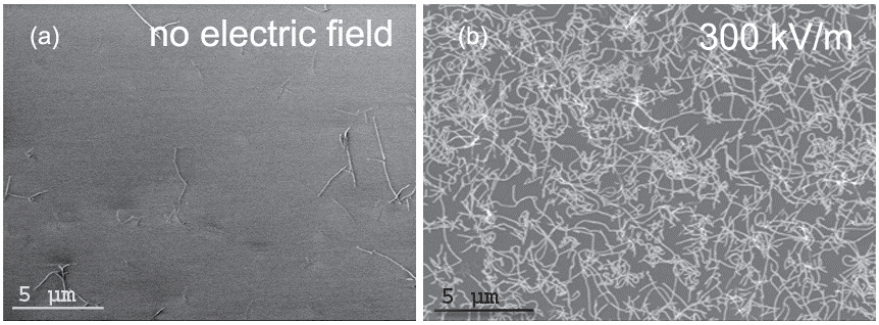


Figure 12 SEM images of CNTNs deposited using an ESP technique, (a) without application of an electric field, and (b) with an applied field of 300 kVm^{-1}.

The CNTN density can be controlled by varying the electric field strength and collection time. The average density of the CNTN was estimated by means of a CPC (TSI Model 3775 or 3022) connected to the ESP. On the basis of the measurements of CNT bundle concentration before and after application of an electric field of a certain polarity, and considering the ratio between the positively- and negatively-charged CNTs at certain synthesis temperatures (1/6 at 850°C and 1/2 at 1050°C, as shown in [153]), the CNTN density was roughly estimated according to the following formula:

$$\rho_{calc} = \frac{t \cdot \Delta C \cdot Q}{S},$$

where t is the collection time, ΔC is the CNT concentration change in the electrostatic precipitator, taking into account CNT polarity, Q is the particle flow rate, and S is the substrate area. The estimated average CNTN density approximately corresponds to the direct CNT density measurements made with using scanning electron microscopy (SEM). Therefore, this method allows calibration of CNTN density during the collection process, by simply adjusting the collection time.

Our second CNT deposition technique requires a thermal precipitator, previously only used for nanoparticle collection [155]. Our work is the first to demonstrate that a thermal precipitation (TP) can be successfully applied for direct dry CNT deposition onto any substrate. Figure 11 (b) shows the TP-based deposition method in more detail. The basis for the TP technique is thermophoresis, i.e., the diffusion of aerosol particles in a temperature gradient, from high- to low-temperature zones of the gas [156]. The TP method uses an electrically heated top plate (T=393 K), and a water-cooled bottom plate (T=283 K) onto which the substrate for CNT collection is placed. This is an effective technique for dry deposition of CNTs directly downstream from the synthesis reactor, which also enables the use of flexible temperature-sensitive substrate materials.

The other two CNTN deposition methods are based on capturing CNTs directly from the gas-phase by flow filtration, and subsequently transferring the CNTN

onto the substrate of interest. We use nitrocellulose membrane filters as a collection media for CNTNs. The networks are transferred to a substrate at room temperature, either by simple press transfer from the filter (PTF), or by dissolving the filter (DF) in acetone. Both of these deposition techniques are schematically shown in Figures 11 (c) and (d), respectively. In the former method, the CNTN is simply pressed (pressure on the order of 10^3 Pa), and can be transferred to practically any material due to poor CNTN adhesion to the nitrocellulose filter [157]. In the latter method, we place the filter onto the substrate, and transfer the CNTN by dissolving the filter on the substrate surface with an acetone bath (Publication III). Both methods are simple, versatile, and economical means of CNTN preparation on various substrates, requiring no dispersion or purification steps prior to the transfer, or additional post-processing after the transfer is complete.

4.3 Fabrication of carbon nanotube thin film transistors

TFT structures generally differ by the order of stacking of the gate, semiconductor material, and source/drain electrodes. We have mainly used bottom-gate CNT TFT structures in this work, however, top-gate structures have also been employed in certain cases for flexible devices. Transistor fabrication, when lithographic techniques were employed, was performed in the class 10-1000 clean room.

Bottom-gate TFTs were fabricated on a highly doped p-silicon substrate, coated on both sides with a thermally grown SiO_2 layer (100 nm) acting as a gate dielectric. A bottom-gate electrode (typically Al: 200 nm or Ti/Au: 10/100 nm) was deposited on the back side of the wafer, after removing the SiO_2 layer using wet etchants (hydrofluoric acid (HF) buffered by the addition of ammonium fluoride (NH_4F)) or reactive ion etching (RIE). Source and drain electrodes (Ti/Au in different proportions, i.e., 3–10 nm of Ti and 50–100 nm of Au) were patterned by standard photolithography, electron-beam evaporation, and lift-off processes. CNTNs were deposited from the floating catalyst CVD reactor using one the above described techniques (ESP, TP, PTF or DF), either before the fabrication of source/drain electrodes, or on top of the patterned electrodes. CNTNs outside of the channel area were removed by oxygen plasma after protecting the transistor channel with photoresist. We have also employed a technique to deposit CNTNs onto the substrate with photolithographically opened areas that define transistor channels, and subsequently remove the photoresist in acetone, so that only CNTs in the transistor channel area adhered to the silicon dioxide surface remain (Publications I and II). In this case, for the precise alignment of the subsequent lithography steps for the source/drain formation, thin Al alignment marks were prepared on the front side of the substrate prior to the CNTN deposition. Finally,

as an additional step for certain cases, an aluminum oxide (Al_2O_3) passivation layer was deposited on top of the device by the atomic layer deposition (ALD) technique to protect the channel layer from external damage, and to suppress hysteresis (Publication II). Al_2O_3 layers have been grown using trimethyl aluminum (TMA) and deionized water as precursors for aluminum and for oxidation, respectively. The deposition was conducted at 190–200°C when using SiO_2/Si substrates, with a deposition rate of 1.1 Å per cycle, and the pressure in the reactor was maintained at around 5 mbar. This processing temperature of ALD was chosen in order to perform thermal treatment of devices to remove possible water residue, which might be present on the device surface after the lift-off and subsequent rinsing processing steps. Nitrogen was used as both a carrier and a purging gas. The ALD growth process is described in more detail elsewhere [158].

When fabricating CNT TFTs on flexible and transparent polyethylene naphthalate (PEN) substrates (Teijin DuPont Films, 125 µm in thickness), the process temperature was maintained below 145°C throughout device fabrication (Publication III). After forming gate electrodes individual for each transistor (Ti/Au: 10/100 nm), a 40 nm Al_2O_3 insulator layer was deposited by ALD at 145°C. Windows for contacting the gate electrodes were then opened by photolithography and RIE. This local-gated device structure allows control of every transistor, important for the fabrication of integrated circuits. Similar processes for source and drain formation, as well as CNT network deposition, were carried out as described above for the devices on a Si substrate. Schematic illustration of typical bottom-gate transistor layouts is shown in Figure 13.

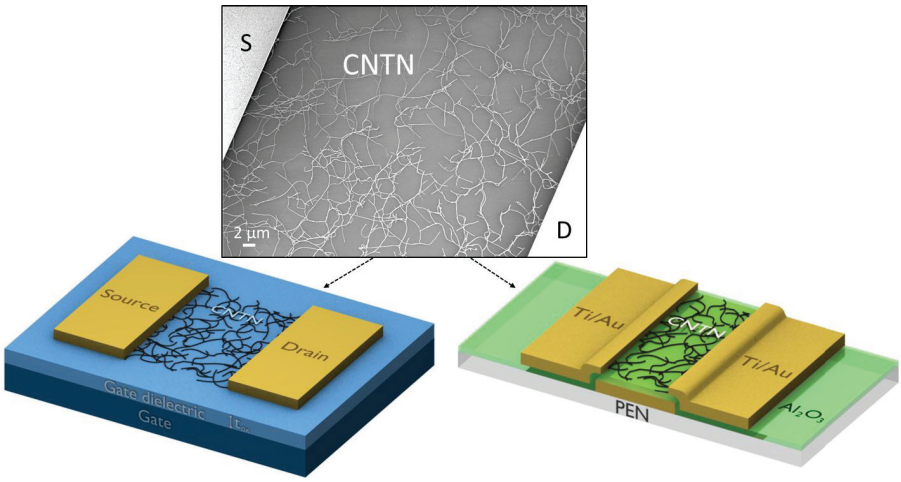


Figure 13 Schematic illustration of the bottom-gate transistor layouts on silicon and plastic substrates, incorporating random CNTNs as a channel material. SEM image of a CNTN is shown in the inset.

Top-gate device structures were fabricated on flexible (Kapton 200 HN, 50.8 µm, or polyethylene terephthalate (PET), 200 µm) substrates (Publications II, IV).

CNTNs were deposited onto the polymer substrate, and the source and drain electrodes (Ti/Au: 20/50 nm) were patterned by standard photolithography, electron-beam evaporation, and lift-off. For the gate dielectric, 100 nm of Al_2O_3 was deposited by ALD on top of the structures. This step also provided effective device passivation. A standard temperature of the ALD growth process was 200°C, but lower temperatures (80°C) were used in the case of heat-sensitive polymer substrates. Finally, the top-gate electrode (50 nm Au or Al, deposited by an electron-beam evaporator) was defined via another step of photolithography and lift-off (Figure 14). Note that no photolithography was used for electrodes formation in Publication IV as described in the next chapter.

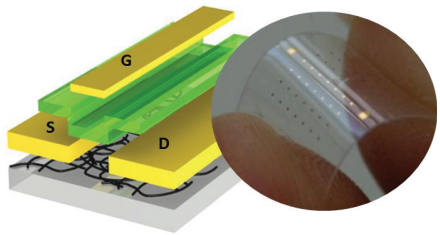


Figure 14 Schematics of a top-gate CNT TFT structure and a photograph of an array of CNT TFTs on a flexible substrate.

4.4 Characterization techniques

As-synthesized CNTs comprising the CNTN were characterized using various microscopy techniques, i.e., SEM, atomic force microscopy (AFM), and transmission electron microscopy (TEM), as well as optical absorption and Raman spectroscopies. SEM was the most frequently used tool for the visualization of the nanotube networks deposited directly from the floating catalyst CVD reactor onto the substrate (Publications I–V). SEM tools Leo Gemini 982, Jeol JSM-7500F, and Zeiss LEO 1560 were typically used for observing the CNTNs, estimating the nanotube bundle length, and analyzing the network morphology. In certain cases, SEM was complemented with AFM imaging of CNTs on SiO_2/Si substrates, which was particularly useful for estimating the average nanotube bundle diameter (Publications III, V). For TEM observations CNTs were collected directly onto TEM grids by an ESP. TEM was carried out for an additional observation of the as-produced CNTs, using Philips CM200 FEG operated at 200 kV (Publications I, II, and V). For absorption analysis, CNT thin films, collected onto a membrane filter, were transferred via the PTF technique to an optically transparent quartz substrate. The absorption spectra were measured by a double beam PerkinElmer Lambda 900 UV-vis-NIR spectrometer, equipped with two excitation sources, a deuterium lamp and a halogen lamp, which together cover the working wavelength range from 175 to 3300 nm. An empty substrate was used in the reference beam to exclude the effect of the substrate for the measurement. Optical absorption

spectrometry was shown to be an effective tool to evaluate the mean diameter of the nanotube samples, since all types of nanotubes are active in the UV-vis-NIR region [159, 160]. Raman spectroscopy (JY-Horiba LabRAM HR 800) of as-grown CNTs, using 633 nm and 488 nm laser excitations, confirmed that the nanotubes produced by the floating catalyst CVD are single-walled, and the sample quality was assessed by analyzing the ratio of the G and D band intensities (Publications I and II).

Three terminal electrical measurements of CNT TFTs were performed using an ambient probe station coupled to an HP 4155A or Agilent 4156C semiconductor parameter analyzers or the Agilent B1500A semiconductor device analyzer. In addition, the Keithley 2612A dual source-measurement unit was used for pulsed characterization. All the measurements were typically carried out at room temperature in air.

5. Results and discussion

5.1 Aerosol methods remove manufacturing bottlenecks

5.1.1 Direct dry or transfer printing

CNTs continuously synthesized using a floating catalyst (aerosol) CVD method provide a significant advantage over other widely used techniques by allowing direct deposition of the CNTN onto the substrate at room temperature. Deposition of CNTs instantaneously following their growth offers a simple and quick method to form random CNTNs on any substrate material. The aerosol-based CVD synthesis of CNTs has been widely explored since the 1990s, but the applicability of as-grown material directly deposited onto the substrate for CNT TFTs was not yet elaborated. With the goal of direct integration of aerosol-synthesized CNTNs into active electronic devices, we have developed four different techniques for the CNT collection onto the substrate, i.e. by applying either electrophoretic or thermophoretic forces or filtering CNTs and subsequently transferring them to the substrate, as described in detail in the experimental section 4.2. By avoiding time-consuming, resource-draining, and potentially detrimental liquid purification and dispersion steps, aerosol technology provides an opportunity to capitalize on the superb properties of pristine CNTs, and reduce the processing costs. Figure 15 shows the process flow schematics for the CNTN formation, demonstrating that aerosol technology allows minimization of the intermediate steps between the CNT synthesis and application, in contrast to a typical solution-processed CNTN deposition, widely explored for flexible applications. Moreover, the aerosol technology is conducive to the fabrication of CNT TFTs on flexible and transparent heat-sensitive substrates, since the deposition is performed at room temperature, unlike substrate-supported CVD growth methods. Aerosol technology can be further scaled-up by increasing the widths of the CNT deposition nozzle and collection filters, and, combined with roll-to-roll printing techniques, pave the way to the realization of large-scale, low-cost, and flexible electronics.

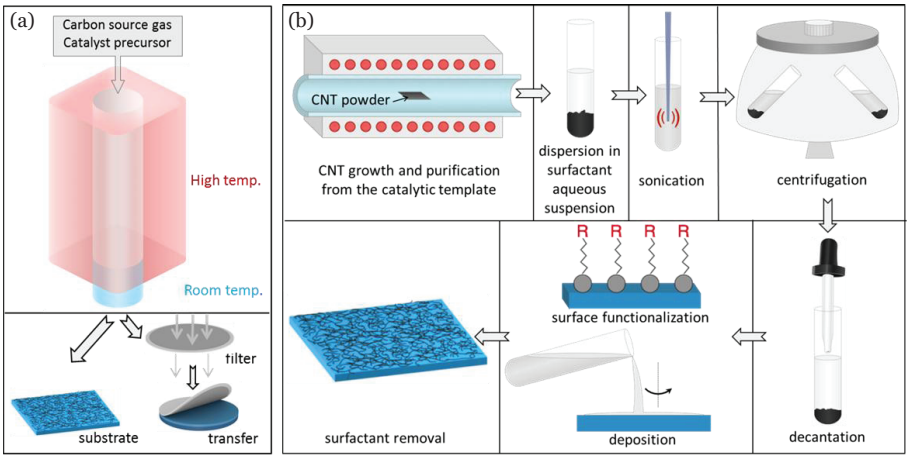


Figure 15 Schematic illustration comparing (a) the direct dry or transfer of CNTNs using aerosol technology and (b) typical solution-based CNTN formation process flows. After the growth of CNTs and their purification from the catalyst and support, a typical solution deposition process involves dispersion of the CNT powder in surfactant aqueous suspension, sonication, further centrifugation to remove big bundles, and decantation to separate the supernatant CNTs. Repeated rounds of centrifugation and decantation, to improve the purification process, may be necessary. Finally, CNTN is deposited onto a substrate typically functionalized with amino groups to improve adhesion, and must be followed by cleaning the residual surfactant. Aerosol technology allows shortening of the process chain, in terms of both time and resource consumption.

5.1.2 Material synthesis optimization

Earlier experiments have demonstrated that by altering the nanotube synthesis conditions in the floating catalyst reactor, the average length of CNTs and their mean diameter can be controlled [149, 150]. *In-situ* nanotube sampling experiments at different locations in the reactor, and subsequent examination by TEM, allowed us to conclude that the length of CNTs is determined by the residence time in the temperature window available for the growth of CNTs in the heated zone of the reactor, before its termination (with the inhibition of the CO-disproportionation reaction at temperatures higher than 945°C) [149]. At low temperature profile the CNT growth window is larger which yields longer nanotubes on average [148, 149]. In this study, the synthesis conditions were optimized with respect to the CNT length. The temperature of around 880°C was determined to be optimal for the synthesis of longer CNTs. The average bundle length was estimated to be around 5.4 µm (standard deviation 4.1 µm). In comparison, CNTs grown at the temperature of 1025°C had the average CNT bundle length of 1.4 µm (standard deviation 0.8 µm). The bundle length was estimated from SEM images of nanotubes collected on SiO_2/Si substrate.

TEM observations and Raman measurements detected high-quality of as-grown CNTs. Figure 16 (a) displays a TEM micrograph of CNT bundles grown at 880°C. Raman spectroscopy measurements using 633 nm and 488 nm laser excitations

confirmed that the nanotubes are single-walled, showing the strong G band (with peak at 1590 cm^{-1}), and characteristic of a CNT radial breathing mode (RBM) in the low-frequency region (100–200 cm^{-1}), as for example shown in Figure 16 (b). A notable characteristics of the collected spectrum is a weak D-band (around 1300 cm^{-1}), which corresponds to the presence of defects on the nanotube walls, or amorphous carbon material in the sample. The high quality of as-synthesized CNTs is finally accessed by estimating the intensity ratio of G and D bands, which appeared to be very low (for the example in Figure 16 (b), I_G/I_D=15 at an excitation energy of 1.96 eV). A separate TEM study has shown that the as-grown CNT sample from the floating catalyst (aerosol) CVD synthesis reactor contains no significant chirality selectivity, producing approximately 1/3 metallic and 2/3 semiconducting CNTs [161].

Optical absorption spectra of the typical CNT sample collected at the temperature of 880°C, as implemented in the high-performance TFTs, is shown in Figure 16 (c). It allows to evaluate the nanotube mean diameter of around 1.1 nm. We have observed that most of the nanotubes grown under these synthesis conditions have a narrow diameter distribution in the range of 0.8–1.4 nm [150]. In contrast, increasing the reactor temperature leads to an increase of the nanotube diameter with the most abundant diameter fractions in the range of 1.6–2.0 nm and the mean diameter of 1.7 nm for the sample grown at 1025°C [150]. We should note that as-deposited CNTNs typically contain individual CNTs and small bundles.

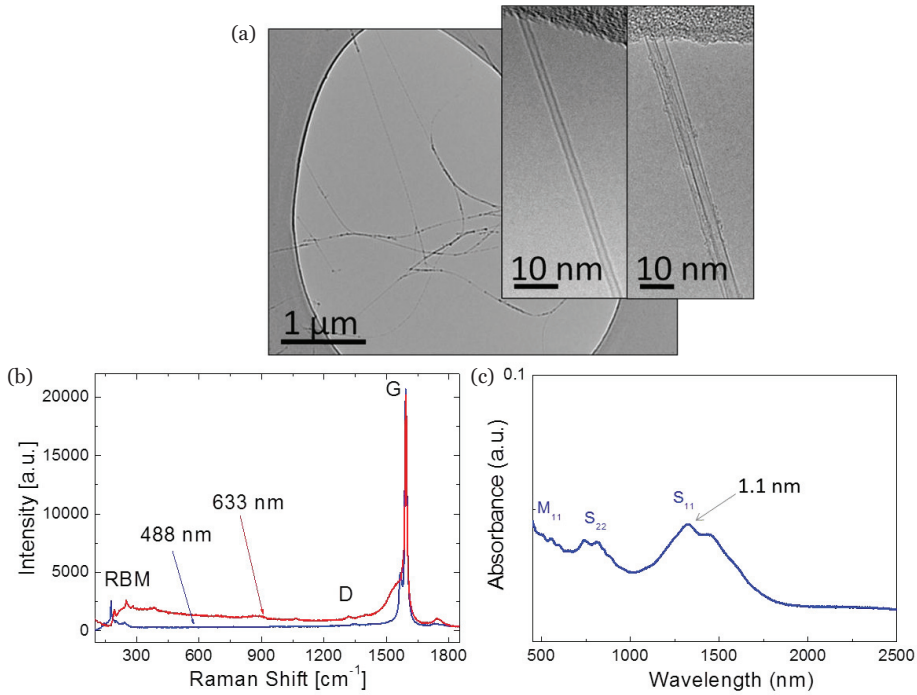


Figure 16 (a) TEM image of as-synthesized CNTs and bundles grown by the floating catalyst CVD method. (b) Raman spectra of CNTs using 633 nm (red) and 488 nm (blue) laser excitations. (c) UV-Vis-NIR absorption spectra of the CNTN. CNTs are synthesized at 880°C.

5.1.3 Nanotube network patterned assembly

Successful implementation of CNTNs in devices requires the ability to pattern the networks into various features at desired locations on the substrate. A number of patterning techniques have been developed, which can be grouped into pre-growth and post-growth methods. Pre-growth patterning refers to the selective growth of nanotubes on a pre-patterned catalyst film by the CVD process. Post-growth patterning includes the techniques developed for the controlled assembly of CNTs onto the substrates after their growth and purification processes from the liquid suspensions, using, for example, inkjet printing, electrophoresis deposition, or chemically anchored deposition [102, 162-164]. Standard photolithography and subsequent oxygen plasma etching is currently the most widely used method to pattern CNTNs in order to electrically separate individual devices from each other, and eliminate parasitic leakage paths. As described in the previous chapter, we have also used this technique to remove undesired CNTNs outside the device area (Publications III and V). In our earlier work, we also exploited photolithographic techniques to open areas for TFT channels prior to direct dry CNTN deposition, followed by photoresist lift-off together with unwanted nanotubes from outside the transistor area (Publications I, II). This patterning technique is applicable with dry deposition of CNTs, and allows simple post-growth patterning of CNTNs without the need for additional surface treatments, since the adhesion between the dry-deposited carbon nanotubes and the silicon dioxide surface was found to be sufficient for successful photoresist lift-off in acetone. However, precise density control with such a patterning technique can become a challenge.

We have also proposed a new CNTN patterning method enabled by aerosol-based dry deposition technology, which does not require photolithographic or etching processes and is performed at room temperature, allowing the use of heat sensitive substrate materials (Publication IV). The key feature of the technique is the utilization of a shadow mask for controllable positioning of CNTs at desired areas, simultaneously with their deposition from the synthesis reactor. The shadow mask can be positioned either directly on the substrate surface where CNTs are deposited, or under the filter paper, the latter producing patterned CNTNs that can be further transferred onto the substrate (see Figure 17).

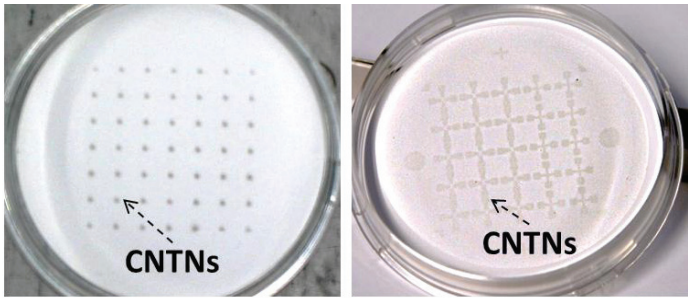


Figure 17 Photographs of patterned CNTNs on a membrane filter formed by placing different shadow masks directly under the filter during the CNT filtration from the gas-phase.

Using a shadow mask for CNTN patterning, positioned on the substrate inside the electrostatic precipitator, also allowed observation of the electrodynamic focusing effect of CNTs during their deposition in the gas-phase. This phenomenon of focused self-assembly of CNTs can be described and explained as follows. Small CNT bundles, formed during the synthesis process, are spontaneously charged as described in detail elsewhere [153]. Charge is accumulated on the shadow mask surface simultaneously with the CNT deposition directly from the floating catalyst (aerosol) synthesis reactor, which modifies the applied electric field in the ESP system, and produces electrostatic lenses around the mask openings. Further, charged CNTs approaching the mask are repelled by the charge of the same polarity accumulated on the mask surface, and are efficiently focused through the mask opening onto the collecting substrate. This provides an opportunity to overcome mask resolution limits, allowing feature sizes smaller than the mask openings to be obtained (see Figure 18). Shadow mask application for CNTN patterning during deposition from the floating catalyst (aerosol) synthesis reactor can further be scaled up and implemented for low-cost, flexible electronic components.

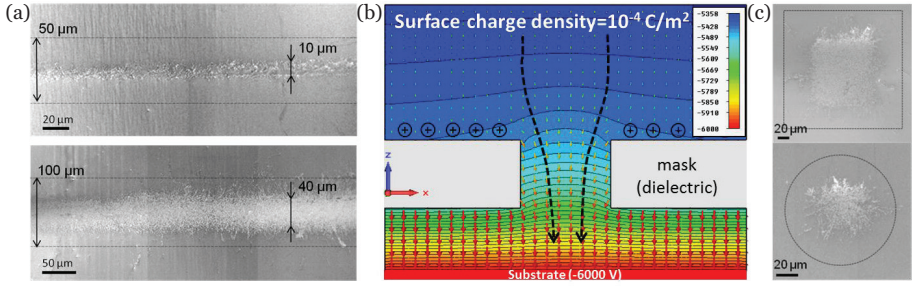


Figure 18 (a) SEM images showing electrodynamic focusing of charged CNTs on a SiO_2/Si surface (the actual shadow mask openings are shown by a dashed line). Polymer mask openings 50 µm and 100 µm wide result in CNTN patterns focused to a width of around 10 µm and 40 µm, respectively. (b) Electric field and potential simulations for a –6 kV voltage applied to the substrate surface, and a charge of 10^{-4} Cm^{-2} accumulated on the mask surface, reveal focusing of CNTs into the 100 µm mask opening. The gap between the mask and the substrate is 70 µm. (c) SEM images showing focused deposition of CNT bundles through a square opening in the mask of size 200×200 $µm^2$ (CNTN pattern is 100×100 $µm^2$) and circular opening with 100 µm diameter (CNTN pattern has a diameter of about 40 µm).

5.1.4 Lithography-free device fabrication

The shadow mask, when placed at a certain distance from the substrate surface, can subsequently be used to define metal electrodes and insulators on top of the CNTN for the fabrication of either back-gate or top-gate TFT geometries on both rigid and flexible substrates. Figure 19 shows a schematic of the step-by-step process of CNTN patterned self-assembly, and precise alignment of all transistor layers by changing only the deposition angle of the metal, keeping the same shadow mask in place.

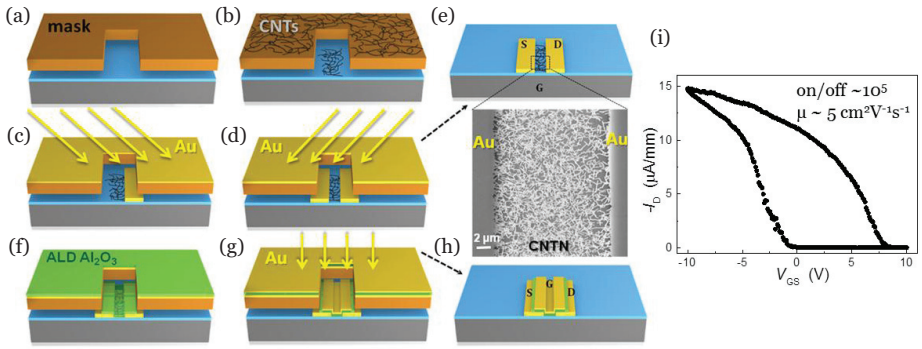


Figure 19 Schematic of a step-by-step, lithography-free fabrication process of a CNT TFT based on the application of a single shadow mask, for both (a, b) the deposition of CNTs directly after the synthesis reactor, and (c, d) defining source and drain electrodes by adjusting the metal deposition angle. (e) Schematic of as-fabricated bottom-gate CNT TFT without a mask. Inset shows SEM image of the CNTN channel between source and drain electrodes. Fabrication of a top-gate thin film transistor by: (f) depositing a dielectric layer of Al_2O_3 using an ALD technique, (g) straight metal evaporation and (h) mask removal. (i) Transfer characteristics of a typical bottom-gate CNT TFT fabricated using a polymer shadow mask with opening size 50×100 μm². V_{DS}=−1 V. The TFT channel length is 55 μm, and channel width is approximately 10 μm (the substrate is tilted on the axis perpendicular to the CNT channel during metal evaporation).

We have demonstrated proof-of-concept of this single mask lithography-free approach by fabricating CNT TFTs on both rigid (SiO_2/Si) and flexible PET substrates (Publication IV). Figure 19 (i) shows an example of the bottom-gate CNT TFT performance fabricated using a lithography-free technique. This novel CNT TFT fabrication method, utilizing only one mask for the deposition of all transistor layers in a self-aligned manner, could offer significant simplification of device fabrication by avoiding standard lithographic processing, and allow lower manufacturing costs due to the reduction of process steps. However, it should be noted that CNTN uniformity and density with focused deposition needs careful control for TFT applications based on heterogeneous CNTs, if trying to obtain smaller device length scales.

5.2 Optimization of device performance

5.2.1 Carbon nanotube network density

When assembling as-synthesized CNTs into a random network configuration, the ability to accurately control the density of nanotubes within the network during the deposition is important for CNT TFT applications. Measuring the gate response of I_D allows to determine whether the networks exhibit semiconducting or metallic behavior, depending on the nanotube density (Publication I). By adjusting the deposition time of CNTs from the floating catalyst (aerosol) reactor, we are able to control the density of CNTNs. SEM images in Figure 20 display the increase of

CNTN density with duration of deposition, knowledge of which allows estimation of the optimal deposition conditions to achieve high device on/off ratio. It is important to note here that the CNTN collection time optimization for TFT application depends on the synthesis conditions and the method of deposition used (Publication V). Figure 20 (d) shows an example of how TFT transfer characteristics may vary depending on the CNTN density.

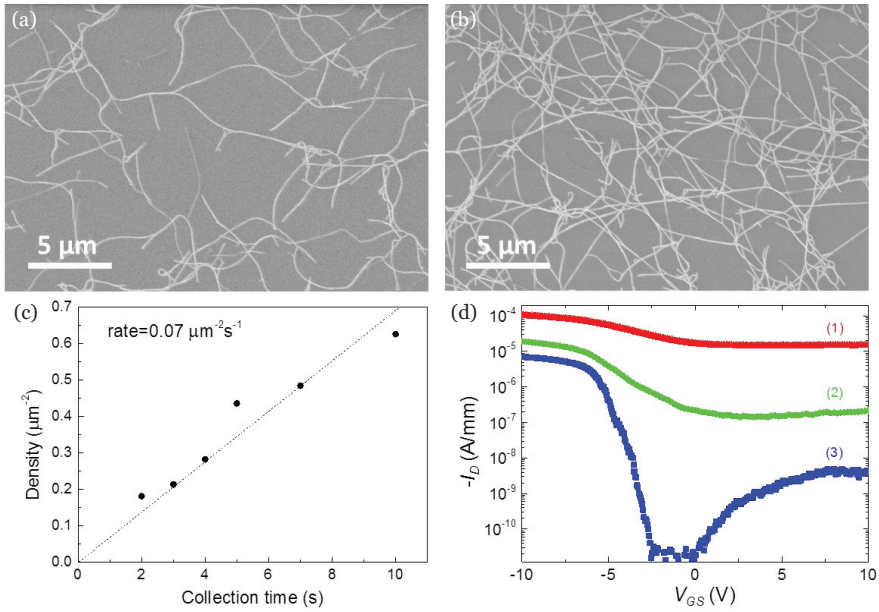


Figure 20 SEM images showing CNTNs with different collection times: (a) 2 s, and (b) 10 s. (c) CNTN density dependence on collection time. Density is estimated from SEM images. (d) Transfer (I_D–V_{GS}) characteristics of the three devices (L_{ch}=W_{ch}=100 µm) with different CNTN densities varying from a denser network collected for 10 s (curve (1)) with weak gate response, to a more rarefied one collected for 2 s (curve (3)) with semicond1ucting behavior. Curve (1) corresponds to CNT TFT with an on/off ratio of approx. 10; curve (2), on/off ratio of approx. 10^2, and curve (3), on/off ratio of $>10^5$. V_{DS}=−0.5 V. In this example CNTN was collected onto a membrane filter by flow filtration and transferred to the SiO_2/Si substrate by the DF method.

Standard silicon substrate covered with a thin silicon oxide layer was first employed in order to evaluate the potential of as-grown CNTNs as a semiconducting material for a TFT channel. In this case, the highly doped silicon substrate served as a common back gate. Figure 21 presents the transfer (I_D–V_{GS}) and output (I_D–V_{DS}) characteristics of a CNT TFT device with an optimized density of nanotubes. The devices typically exhibit predominantly p-type conduction in ambient environment when the gate voltage is swept from –10 V to +10 V. CNT TFTs show linear behavior at low V_{DS} suggesting the formation of ohmic contacts between the nanotubes and electrodes.

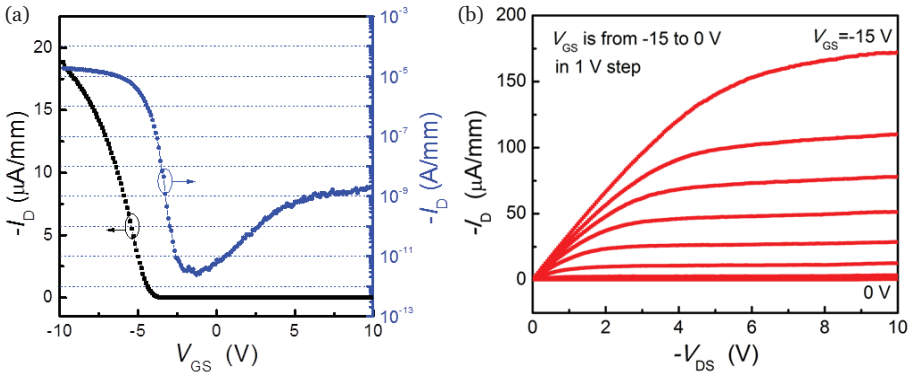


Figure 21 (a) Transfer (I_D–V_{GS}) characteristics of a typical CNT TFT with optimized density on a silicon substrate. (b) Output (I_D–V_{DS}) characteristics of the same device exhibiting saturation behavior. L_{ch}=W_{ch}=100 μm. V_{DS}=−0.5 V. CNTN was deposited by DF method.

5.2.2 On/off ratio scaling with channel length

One of the most important performance parameters of a TFT is the current on/off ratio, which demonstrates the efficiency of the current modulation with the gate bias. When integrating many transistors into a digital circuit, the presence of current at the transistor off-state would result in large power consumption, and therefore such a circuit would be impractical. We have examined the variation of the device on-current (I_{ON}), off-current (I_{OFF}), and on/off ration (I_{ON}/I_{OFF}) with respect to the channel length in CNT TFTs, as shown in Figure 22 (Publication III). In this study we used CNTN material synthesized using optimized conditions (long CNTs with up to 10 μm in length) and deposited by the DF method.

Observing the performance of on-state and off-state currents with respect to the device channel length, we are able to determine when the device is operating near the percolation region. In our case, CNTN collected onto a filter for 10 s showed a classical 2D conductor behavior, where $I_D \sim L_{ch}^{-1}$, and both m_{on} and m_{off} are close to unity. For a rarified network with a collection time of 2 s, a network-like behavior governed by percolation is observed. In this case, I_{ON} exhibits nearly inverse proportional dependence on L_{ch}, while I_{OFF}, which is determined by metallic and/or large-diameter nanotubes, rapidly decreases in the range of L_{ch} values from 20 to 50 μm, and, accordingly, a large on/off ratio is obtained for L_{ch} values larger than 40 μm (see Figure 22 (a)). Figure 22 (b) shows the statistics of on/off ratio distribution with L_{ch} varying from 5 to 100 μm. For L_{ch}=100 μm, 91% of the TFTs have on/off ratios higher than 1×10^5 (77% of the TFTs have on/off ratio higher than 1×10^6); the median value in this case is 4×10^6. The bimodal distribution of the on/off ratio, which can be seen for L_{ch} from 30 to 50 μm, indicates the presence of separate groups of devices with and without metallic paths (shown by blue and green lines, respectively). Such a mode transition occurs at values of L_{ch} which are several times longer than L_{CNT}. That is explained by the reduced probability of metallic CNTs shorting out the device.

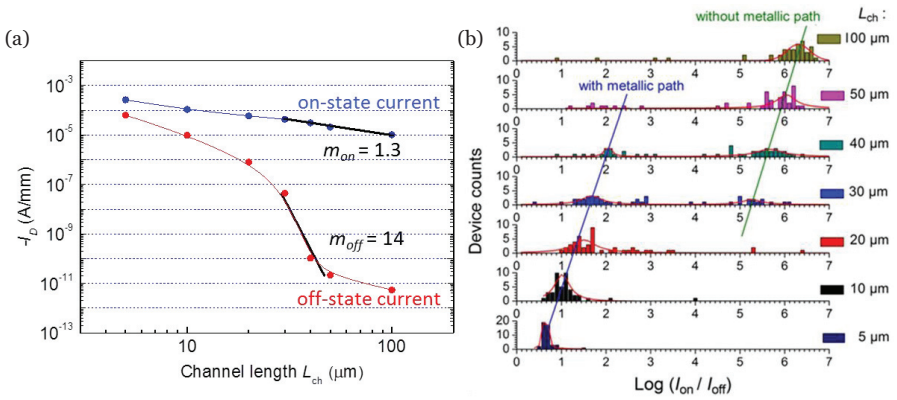


Figure 22 (a) On- and off-state currents as a function of channel length for a CNTN collected for 2 s and deposited by DF method. Data represents the median values for twenty CNT TFTs measured for each L_{ch}. (b) Histograms of the distribution of the on/off ratio for L_{ch} values ranging from 5 to 100 μm. Forty-six TFTs were considered for each value of L_{ch} in the statistical analysis. Red curves are Gaussian fits. Blue and green lines indicate the separate groups of devices with and without metallic paths, respectively. V_{DS}=−0.5 V. V_{GS} is swept from −10 to +10 V.

5.2.3 Mobility evaluation

Carrier mobility (μ) of a random network of CNTs is another important parameter to evaluate the TFT performance. It can be calculated from the linear region of direct current characteristics by the standard formula:

$$\mu = \frac{dI_D}{dV_{GS}} \frac{L_{ch}}{W_{ch}} \frac{1}{V_{DS}} \frac{1}{C_g},$$

where L_{ch} and W_{ch} are the device channel length and width, V_{DS} the bias voltage, V_{GS} the gate voltage, I_D the drain current and C_g the gate capacitance per area. As discussed in Chapter 3, two models are used to estimate the gate capacitance: the parallel plate model, and a rigorous analytical model. The parallel plate model, in which a CNTN is assumed to be a homogeneous sheet, overestimates the gate capacitance, and correspondingly underestimates the average mobility of a CNTN. However, this model is typically used in the literature to evaluate the mobility as a performance index of common TFTs based on silicon, organic, and other thin film materials. Therefore, using the parallel plate gate capacitance estimation allows for direct comparison of our devices with others reported in the literature.

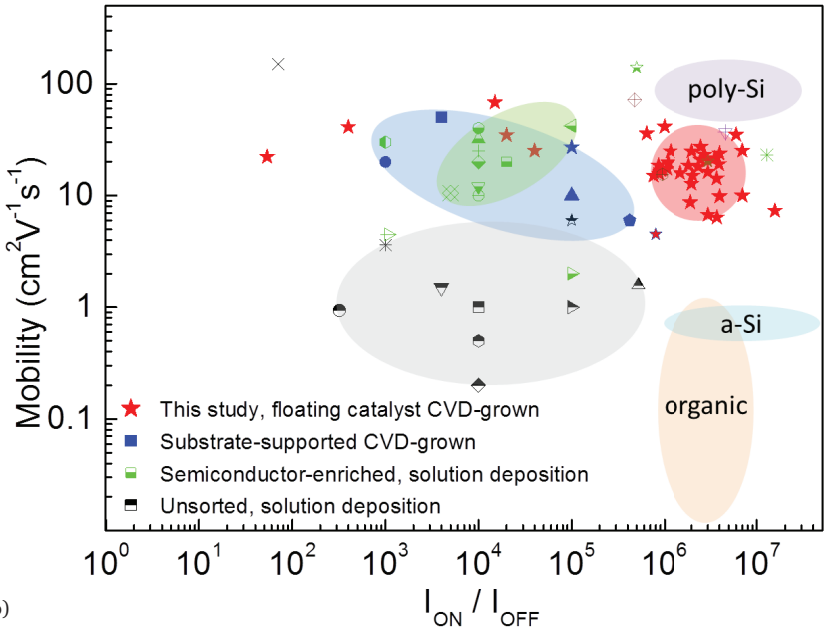
Our optimized TFTs, in terms of material quality, network density, and device geometry, were able to demonstrate a mobility of 35 $cm^2V^{-1}s^{-1}$ and I_{ON}/I_{OFF} ratio of 6×10^6, simultaneously. Mobility was estimated using a parallel plate model for the capacitance and the CNTN was deposited by the DF method in this case. Figure 23 compares the mobility and the on/off ratio of 36 such CNT TFTs (L_{ch}=100 μm) on mechanically rigid substrates, with those of other TFTs based on amorphous silicon (a-Si), polycrystalline silicon (poly-Si), ZnO-based semiconductors, organic materials, and other representative best-performing TFTs based on CNTNs reported in the literature. The typical mobility and I_{ON}/I_{OFF} ratio of our devices are

approximately 20 $cm^2V^{-1}s^{-1}$ and 1×10^6, and the corresponding maximum values are 68.3 $cm^2V^{-1}s^{-1}$ (with an I_{ON}/I_{OFF} ratio of 1.5×10^4), and 1.6×10^7 (with a mobility of 7.3 $cm^2V^{-1}s^{-1}$), respectively. Figure 23 also includes data demonstrating the best-performing CNT TFTs fabricated using the TP deposition method with optimized network density demonstrating the carrier mobility of 20 $cm^2V^{-1}s^{-1}$ and $I_{ON}/I_{OFF} = 3\times10^6$ simultaneously (Publication V), and the ESP deposition method with the mobility of 4.5 $cm^2V^{-1}s^{-1}$ and $I_{ON}/I_{OFF} = 8\times10^5$ (Publication II). The TP technique was found to be a promising approach for the preparation of CNTNs that are dry-deposited directly onto the substrate after their synthesis, without the use of membrane filters for initial CNT collection. Further studies of this technology and device performance optimization are encouraged. The peculiarities of the CNTN morphology characteristic for different deposition methods was found to significantly influence the device performance as discussed in the next section. Comparison of our CNT TFTs with those in recent representative reports reveals that floating catalyst (aerosol) CVD-grown CNTNs are capable to show outstanding performance in terms of concurrent mobility and on/off current ratio, being inferior to only a few recent reports based on semiconductor-enriched CNTNs. While significantly outperforming TFTs based on a-Si and typical soluble organic materials, our TFTs approach performance comparable with low-temperature poly-Si and amorphous In-Ga-Zn-O TFTs, which typically require conventional vacuum processes for deposition on a substrate.

The effective coverage of such rarified CNTNs, used for TFTs, is quite low. For the above mentioned high-performance CNT TFTs, the linear density of CNTs (Λ_o) was estimated to be about 0.54 tubes/μm. Therefore, we used a more rigorous analytical model to estimate the gate capacitance, which takes into account the realistic electrostatic coupling between sparse CNTs and the gate electrode [141] (see Chapter 3). Hence, the gate capacitance ($C_{g,r}$) becomes lower than that estimated by the parallel plate model ($C_{g,p}$), as $C_{g,r}/C_{g,p}$~1/18. Based on the rigorous model, the device mobility is evaluated to be 634 $cm^2V^{-1}s^{-1}$ for the device with I_{ON}/I_{OFF} ratio of 6×10^6. The highest carrier mobility evaluated by a rigorous model reached 1236 $cm^2V^{-1}s^{-1}$ with concurrent I_{ON}/I_{OFF} ratio of 1.5×10^4.

High-performance of our CNT TFTs is attributed to a number of important factors, i.e., carefully controlled density and unique morphology of as-deposited CNTNs, comprised of long and straight nanotubes with a narrow diameter distribution. Deposition directly following the gas-phase growth yields clean and high-quality nanotube material which plays a significant role. By avoiding solution processing to prepare CNT suspensions, we avoid possible contamination of CNTs with surfactants, which are known to degrade the electrical performance of CNT TFTs by increasing the resistance between CNTs and CNT/electrodes, or causing charge traps around the nanotube itself, frustrating the gate modulation [111, 165, 166].

(a)



(b)

Substrate-supported CVD-grown CNTNs	**Solution deposited, semiconducting CNTNs**
▲ Snow *et al.*, Appl. Phys. Lett., 2003 [45]	▬ Arnold *et al.*, Nat. Nanotechnol., 2006 [83]
★ Cao *et al.*, Nature, 2008 [79]	▲ Zhang *et al.*, Nano Lett., 2011 [98]
■ Sangwan *et al.*, Appl. Phys. Lett., 2010 [123]	◆ Takahashi *et al.*, Nano Lett., 2011 [111]
⬟ Mizutani *et al.*, Appl. Phys. Expr., 2010 [167]	★ Miyata *et al.*, Nano Res., 2011 [80]
● Kim *et al.*, ACS Nano, 2010 [73]	◒ Rouhi *et al.*, Adv. Funct. Mater., 2011 [99]
Solution deposited, unsorted CNTNs	⊖ Engel *et al.*, ACS Nano, 2008 [51]
★ LeMieux *et al.*, Science 2008 [50]	◀ Sangwan *et al.*, ACS Nano, 2012 [168]
▲ Okimoto *et al.*, Adv. Mater., 2010 [89]	▶ Izard *et al.*, Appl. Phys. Lett., 2008 [169]
◓ Nobusa *et al.*, Appl. Phys. Lett., 2011 [102]	◐ Ha *et al.*, ACS Nano, 2010 [90]
◆ Noh *et al.*, IEEE Electr. Device Lett., 2011 [92]	✳ Chen *et al.*, Nano Lett., 2011 [91]
▼ Zhao *et al.*, J. Mater. Chem., 2012 [104]	+ Lee *et al.*, Small, 2012 [105]
⬒ Schindler *et al.*, Physica E, 2007 [95]	⊠ Lee *et al.*, Adv. Mater., 2010 [170]
◓ Takenobu *et al.*, Appl. Phys. Lett., 2006 [172]	▷ Zhang *et al.*, ACS Nano, 2012 [171]
▷ Asada *et al.*, J. Phys. Chem. C, 2011 [81]	▼ Wang *et al.*, Nano Lett., 2009 [71]
× Snow *et al.*, Appl. Phys. Lett., 2005 [97]	**Examples of other materials**
✳ Numata *et al.*, Appl. Phys. Expr., 2012 [103]	⊕ ZnO, rf magnetron sputtering [173]
	⊕ amorphous In-Ga-Zn-O, rf sputtering [174]
	⊕ organic single crystal, PVD [175]
This work, floating catalyst (aerosol) CVD-grown CNTNs	
★ CNTN deposited by DF ★ CNTN deposited by TP ★ CNTN deposited by ESP	

Figure 23 (a) Mobility vs. on/off ratio plot, comparing our 38 CNT TFTs based on CNTNs deposited by various methods with other representative best-performing TFTs based on CNTNs, amorphous silicon [44], polycrystalline silicon [176], ZnO-based semiconductors [173, 174], and organic materials [177]. The comparison excludes all-nanocarbon TFTs. All mobility values are evaluated using a parallel plate model. (b) Legend for representative CNT TFTs from earlier reports, and examples of other alternative materials.

5.2.4 Carbon nanotube network morphology

The properties of electronic devices based on CNTNs are found to depend on the CNT deposition method used, which can yield a range of network morphologies. Here, we define morphology to include CNT density, arrangement of CNTs within the network or network layout (e.g., curliness/alignment), and CNT-CNT junction density, all of which are expected to affect transport in the CNTN. We have investigated the morphology of CNTNs deposited at room temperature onto SiO_2/Si substrates by four different techniques: electrostatic or thermal precipitation, and filtration followed by press transfer or dissolving the filter (Publication V). The deposition methods are described in more detail in Chapter 4. The CNTNs were collected on the same synthesis day, using the same CNT synthesis conditions. This approach ensures the consistency of individual CNT structural properties. We have used the same CNT deposition time (10 s), resulting in comparable CNTN densities amongst all the collection methods, as verified later from SEM images using image analysis software (Publication V). No additional CNT processing, CNTN modification, or wafer treatment prior to nanotube deposition was employed. Despite the same synthesis conditions, the resulting CNTNs possess very different morphology after subsequent deposition onto the substrate using one of the four methods. Figure 24 shows SEM images of CNTNs as transistor channels which clearly possess different arrangement of CNTs and CNT bundles within the network, corresponding to the deposition techniques used.

In order to understand how CNTN morphology affects the electrical properties of CNTN devices, we fabricated bottom-gate TFTs with the same device geometry based on CNTNs deposited by four different deposition techniques. Figure 25 compares the performance of such devices in terms of their device mobility and on/off ratio. The device mobility was calculated from the forward sweep DC transfer characteristics (solid symbols and top error bars in Figure 25). We note that due to the presence of hysteresis in CNT devices the forward sweep DC measurement somewhat overestimates mobility compared to the reverse sweep and pulsed measurements (bottom error bar and open symbols in Figure 25). Nevertheless, using the forward sweep DC transfer curve and the parallel plate model for gate capacitance estimation allow direct comparison of our devices with other representative reports in the literature, as shown in the previous section. Our results demonstrate that the electrical properties of CNT TFTs vary significantly with the CNTN deposition method used. Devices fabricated from CNTNs deposited by ESP exhibit the best performance in terms of I_{ON}/I_{OFF} (up to $>10^5$) in comparison with other TFTs with this network density, but typically have lower device mobility, $\mu \approx 2–14$ $cm^2V^{-1}s^{-1}$. CNT TFTs fabricated using the PTF deposition method typically have higher mobility, $\mu \approx 3–30$ $cm^2V^{-1}s^{-1}$, and lower $I_{ON}/I_{OFF} \approx 6–20$, in comparison with ESP devices. The DF deposition method results in CNT TFTs with low $I_{ON}/I_{OFF} \approx 2–8$, but high $\mu \approx 50–60$ $cm^2V^{-1}s^{-1}$. We note that low device

on/off ratio is due to the higher CNTN density of such devices in comparison with the optimized devices presented in the previous section. CNT TFTs based on CNTNs deposited by TP show good potential for further development with high $\mu \approx 30–60$ cm^{2}V^{-1}s^{-1}, comparable to DF-deposited devices, and higher I_{ON}/I_{OFF} ratio ≈20–1100 (for optimized densities at lower deposition time $I_{ON}/I_{OFF} \approx 10^5–10^6$ and $\mu \approx 15–20$ cm^{2}V^{-1}s^{-1}, concurrently, as demonstrated in the example of Figure 23).

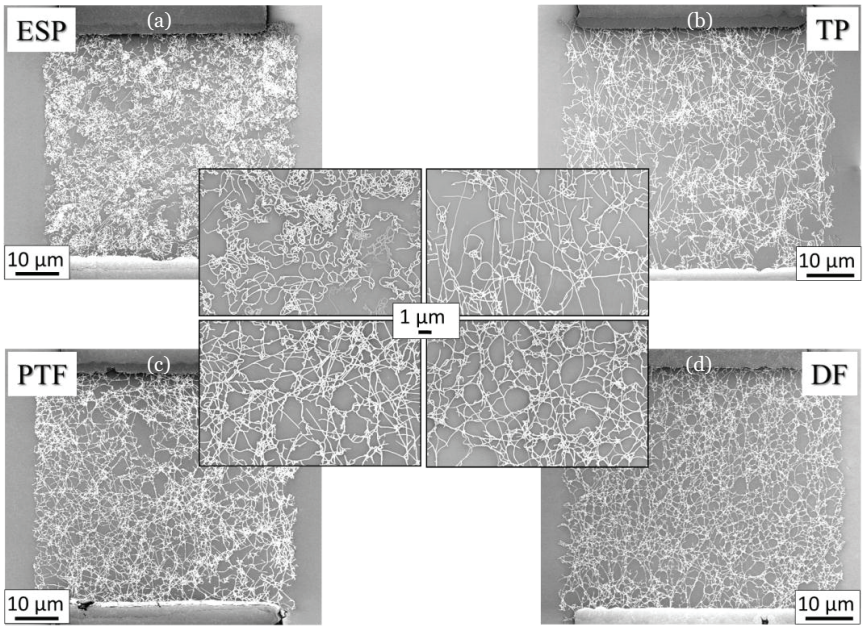


Figure 24 SEM images showing the morphology of CNTNs in a transistor channel (L_{ch}=W_{ch}=50 µm) formed on SiO_2/Si substrate by four different CNTN deposition techniques: (a) CNTN deposited by electrostatic precipitation (ESP); (b) CNTN deposited by thermal precipitation (TP); (c) CNTN deposited by press transferring from a filter (PTF); (d) CNTN deposited after dissolving the filter (DF). Insets in the center show higher magnification SEM images for each deposition technique.

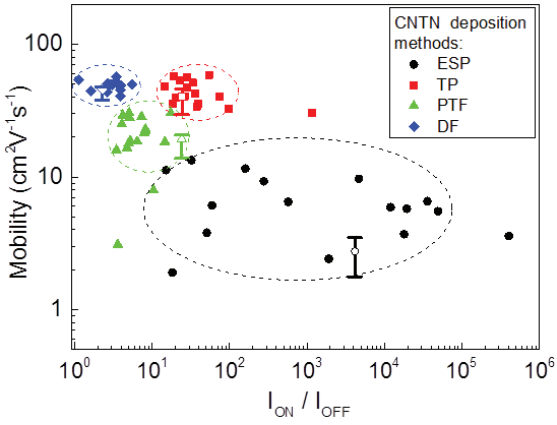


Figure 25 Comparison of mobility and on/off ratio of CNT TFT devices, where the transistor channel is comprised of a random CNTN grown under the same CNT synthesis conditions and deposited by the four methods directly after synthesis. L_{ch}=W_{ch}=50 µm. V_{DS}=−1 V. Error bars highlight the effect of hysteresis on mobility calculations (top - forward sweep, bottom - reverse sweep). Open symbols represent pulsed measurement results.

We analyzed the CNTN morphology using SEM, AFM and image analysis software to investigate the difference in device performance (Publication V). SEM images acquired are shown in Figure 24. We find that CNTs and CNT bundles deposited directly onto the substrate by ESP under the influence of an applied electrical potential tend to exhibit rings, loops and curled morphology, which can be attributed to electrically driven bending instability and/or a mechanical buckling effect [178, 179]. Such unique morphology of ESP-deposited CNTNs with high tube-to-tube junction density could result in enhanced electron scattering processes in comparison with the other methods, and renders more diffusive transport. The rings, which are mostly made of CNT bundles, are bridging straight and curled CNTs, therefore introducing more Schottky barriers in the path of the current flow. This could explain the lower mobilities of ESP-deposited CNTNs than those of the other three deposition methods. The peculiar orientation of the ESP-deposited CNTs also causes higher device-to-device variation, corroborated by the wide distribution of on/off ratio in such devices (approximately $20–5\times10^5$).

In contrast, TP-deposited CNTs result in a higher degree of alignment in the direction of aerosol flow compared with other deposition techniques. Greater CNT alignment in the TFT channel and fewer junctions along the current flow paths, improve the performance of TP-deposited CNT TFTs, relative to those deposited with other methods. Furthermore, decreased bundle diameter as observed from AFM images can also contribute to the improved device performance in terms of on/off current ratio. These results suggest that, when optimized, the TP method could be a promising technique for direct and dry CNTN deposition for TFT applications.

Both the PTF and DF techniques employ a membrane filter for the deposition of CNTNs, which are then transferred to the receiving substrate. CNTNs deposited by the PTF method preserve the morphology of as-deposited random films formed by flow filtration directly after gas-phase synthesis. This deposition method, however, could be less efficient when transferring very sparse CNTNs. Networks deposited by the DF method exhibit a unique morphology due to curvature induced by liquid droplet meniscus evaporation. This leads to an increased tube-to-tube contact area [180, 181]. The lack of curvature in the CNT links between junctions, as compared to the ESP method, leads to increased network conductivity. The morphology of DF-deposited CNTs is especially interesting due to the predominant Y-type tube-to-tube junctions rather than X-type, as shown in Figure 26 (a). Because there is strong coupling of carrier wavefunctions at tube-to-tube contacts that have a large area, the Y-type junctions (which have a large junction area) are expected to have lower junction resistance than the X-type junctions (which have a small junction area, and therefore a high contact resistance), as schematically shown in Figure 26 (b). This agrees with the recent c-AFM experimental results, which show that the inter-nanotube contact resistance of Y-type junctions (R_j=58±9 kΩ) is significantly

lower than that of X-type junctions (R_j=180±20 kΩ) [131]. The high-performance of CNT TFTs reported in Publication III was mainly attributed to this unique CNT arrangement within the network, together with the use of long CNTs and small bundles.

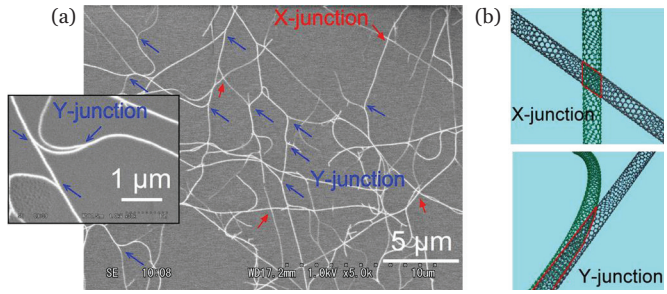


Figure 26 (a) SEM image of a sparse CNTN deposited onto a SiO_2/Si substrate by DF method. Inset: magnified view of Y-junctions. The red and blue arrows indicate X- and Y-junctions. (b) Schematics of X- and Y-junctions.

We find that there is a close relationship between the morphology of CNTNs and the electrical performance of TFTs based on these networks. Each deposition technique requires accurate optimization of the deposition time to control the density of heterogeneous CNTs for maximized CNT TFT performance. Our results emphasize the important role of CNTN morphological parameters, especially nanotube alignment and junction density, for the practical applications of CNTNs integrated into devices directly after the gas-phase synthesis.

5.2.5 Hysteresis suppression

Gate-induced hysteresis is typically observed in the transfer characteristics of our devices in an ambient environment. The presence of such hysteresis is a common and significant challenge of CNT TFTs, the understanding and elimination of which is important for repeatable and robust operation of logic circuits. This phenomenon in CNT TFTs has been attributed to defects or charge traps either at the CNT/dielectric interface or within the gate dielectric itself [182]. Interface trapped charges between the gate electrode and dielectric due to structural defects and impurities have also been shown to be a source of hysteresis in CNT TFTs [78]. Investigation of the electrical behavior of CNT transistors under different environments led to the conclusion that water molecules surrounding the nanotube and the dielectric surface are the most significant contributors to hysteresis in non-passivated CNT transistors [183]. For experimental purposes, storing our CNT TFT devices under vacuum resulted in hysteresis reduction by eliminating water molecules weakly adsorbed to the CNT surface, but could not fully eliminate hysteresis even after 7 days storage, due to the presence of SiO_2 surface-bound water, and additional heating in a dry environment was required (Publication II). Different strategies have been implemented to encapsulate CNT

transistors and reduce hysteresis associated with interface defects. For example, it was shown that coating nanotube devices with a silicon nitride (SiN_x) film [184] or PMMA polymer after heating [183] can significantly reduce hysteresis. It was, however, reported that SiN_x film deposition by electron cyclotron resonance sputtering or thermal CVD induces surface damage in the CNT channel, leading to current degradation [184], while the PMMA protection of the CNT channel from the humidity of the ambient atmosphere is not sufficiently effective [185]. ALD, on the other hand, has been shown to be an attractive technique for non-destructive passivation of CNTs, with the possibility to grow thin films at lower processing temperatures [186, 187]. Coating of our CNT TFTs with the ALD Al_2O_3 almost fully eliminated the device hysteresis, which is attributed to the reduction of interface trap density around the CNTs when the devices are baked at 200°C in vacuum during the ALD process, as can be seen in Figure 27 (a, b) (Publication II). Figure 27 (c) demonstrates an example of the conformal coverage of a CNT bundle with ALD Al_2O_3, deposited using TMA and H_2O precursors.

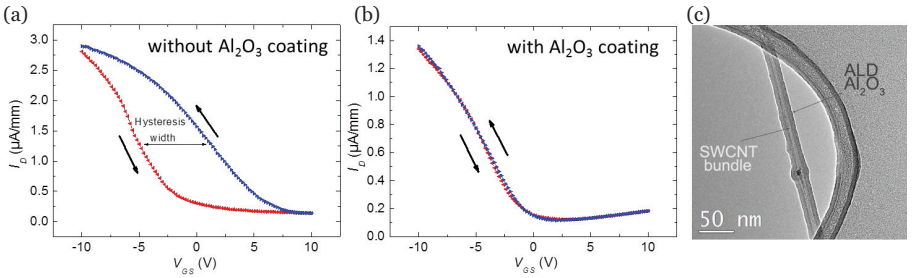


Figure 27 Transfer characteristics (I_D–V_{GS}) of a CNT TFT (a) before ALD Al_2O_3 passivation and (b) after coating with a 32 nm thick Al_2O_3 layer. L_{ch}=50 µm, W_{ch}=100 µm. (c) TEM image of a CNT bundle coated with a 5 nm ALD Al_2O_3 layer. For this experiment CNTs were grown at 1025°C and collected onto a TEM grid using ESP.

It should be pointed out that the passivation of CNT-based devices with ALD-grown layers at certain conditions was shown to change the device polarity from p-type to predominantly n-type, which is likely caused by the interface fixed charges doping effect [188]. Air-stable conversion of CNT TFTs from p-type to n-type using HfO_2 ALD passivation layer grown at high temperature was recently investigated and explained by desorption of oxygen and accumulation of positive fixed charge in the high-*k* oxide layer [189]. Therefore, accurate control over the conditions and temperature of ALD growth and the post-annealing procedure are important for controlled device passivation [190].

It is worth noting here that the presence of hysteresis between the forward and reverse gate voltage sweeps adds uncertainty in calculating the mobility from the electrical characteristics of CNT TFTs. The pulsed measurement technique has recently been applied to measure transistors based on individual CNTs [191] and networks [192]. When hysteresis cannot be eliminated during fabrication, the

pulsed measurement technique enables effective hysteresis suppression and a more accurate evaluation of the mobility values (as was shown in Figure 25 with open symbols). We used a pulsed sweep method with gate pulses of alternating polarities (AP) by applying a negative V_{GS} pulse after each positive pulse with the same duration and amplitude (as shown in the inset of Figure 28), instead of a monotonic sweeping of V_{GS} between incrementing (forward) and decrementing (backward) values (Publication V). In our experiment, the pulse duration (t_{ON}) was 20 ms and the off time (t_{OFF}) was set to zero, since it was shown that in AP mode hysteresis elimination is independent of the duty cycle ($t_{ON}/(t_{ON}+t_{OFF})$) [192]. This is due to the immediate discharging of the charge traps by the gate pulse of the opposite polarity [192]. Figure 28 presents our experimental results comparing the transfer characteristics of a typical CNT TFT using DC gate voltage measurements at ambient conditions, and the same device measured by AP method, with the latter exhibiting a largely reduced hysteresis effect.

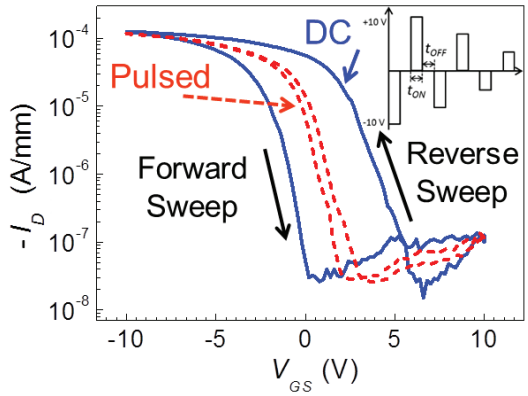


Figure 28 Transfer characteristics (I_D–V_{GS}) of a CNT TFT using DC and pulsed characterization under ambient conditions. CNTN is deposited using ESP. L_{ch} = W_{ch} =50 µm at V_{DS}=−1 V.

5.3 Towards flexible electronics

Taking advantage of the developed room temperature CNTN deposition techniques and knowledge of as-deposited CNTN properties, we have fabricated CNT TFTs on flexible plastic substrates. In this case, CNT TFTs were fabricated on a PEN substrate with a 40-nm thick Al_2O_3 gate dielectric layer deposited by an ALD technique at 145°C. Figure 29 shows a schematic of a flexible CNT TFT and transfer characteristics of an optimized device with a similar performance to that of a CNT TFT on a silicon substrate.

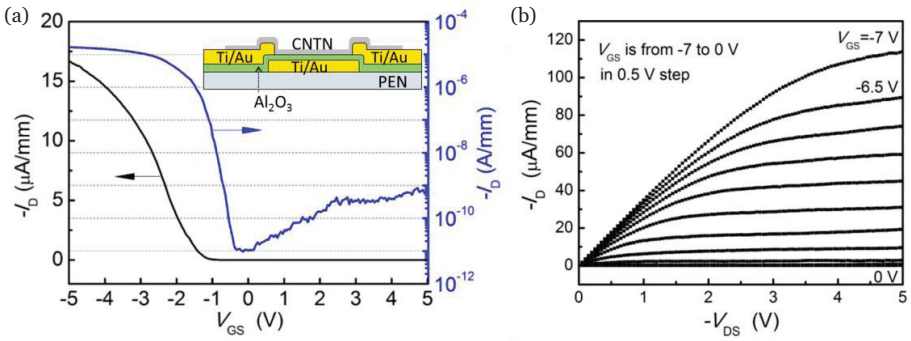


Figure 29 (a) Transfer characteristics (I_D–V_{GS}) and (b) output (I_D–V_{DS}) characteristics of a typical bottom-gate CNT TFT on a PEN substrate with L_{ch}=W_{ch}=100 μm at V_{DS}=−0.5 V. Inset in (a) shows device schematics.

Further, we deviate from single CNT TFT optimization to larger-scale integration of devices, fabricating flexible digital circuits. The circuits include inverters, ring oscillators of 3, 11 and 21 stages, NOR and NAND gates. Performance uniformity of CNT TFTs is especially important for their integration into digital circuits. Figure 30 shows a photograph of integrated circuits on a flexible and transparent PEN substrate.

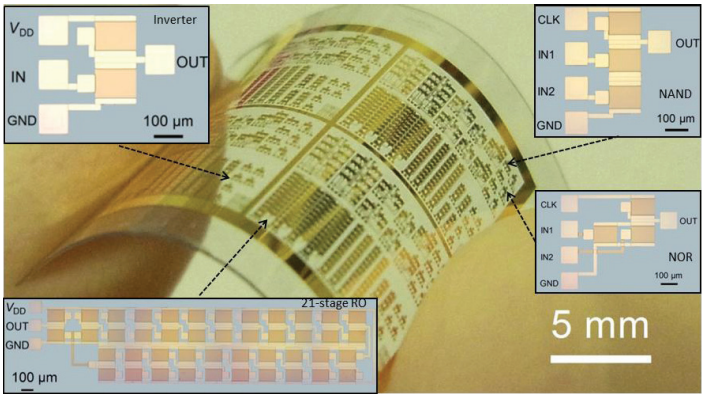


Figure 30 Photograph of devices fabricated on a flexible and transparent PEN substrate. Inset: optical micrograph of an inverter, 21-stage ring oscillator, NAND and NOR logic gates built out of CNT TFTs.

Fabrication of an inverter and a ring oscillator is a basic requirement for a semiconductor technology, to be able to construct a complete range of logic circuits. We fabricated an inverter based on two identical CNT TFTs (driver and load), which successfully performed the simplest logic function - inversion. The load was a gate-source-shorted CNT TFT, lightly doped with F_4TCNQ (tetrafluorotetracyano-*p*-quinodimethane) to adjust the logic threshold voltage [193]. Figure 31 (a) shows the input-output characteristics of an inverter with a voltage gain of 16 at a supply voltage (V_{DD}) of −5 V. The large area of the eye pattern in the folded transfer curve implies a large noise margin for logic

operation, and allows us to construct logic integrated circuits. However, it is important to note that the noise margin, in fact, is decreased due to the presence of hysteresis in CNT TFTs, which should be eliminated using appropriate surface treatments as discussed in the previous section.

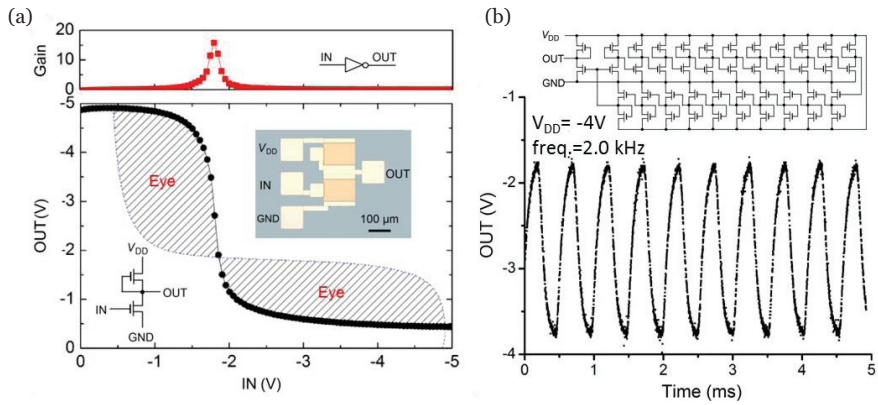


Figure 31 (a) Input-output and gain characteristics of an inverter. Inset: optical micrograph, circuit diagram and symbol of an inverter. (b) Output characteristics of the ring oscillator with an oscillation frequency of 2.0 kHz at V_{DD}=−4V.

A ring oscillator is typically built out of an odd number of inverters or delay cells with the output of the last stage fed back to the input of the first, forming a closed-loop chain [194]. A multi-stage ring oscillator allows evaluation of the compatibility of present CNT TFTs with conventional circuit architectures and device uniformity, as proper operation of each TFT used in the ring oscillator is necessary to realize oscillation [167]. Figure 31 (b) shows output characteristics and a circuit diagram for a 21-stage ring oscillator with an output buffer, in which 44 CNT TFTs are integrated on a PEN substrate. An oscillation of the output voltage begins spontaneously as soon as the supply voltage V_{DD} reaches a threshold value of approximately –2 V. The oscillation frequency reaches 2.0 kHz at a V_{DD} of –4 V. This circuit demonstrates good uniformity of the present CNT TFTs. The oscillation frequency of a ring oscillator depends on the delay time of each inverting stage, τ_d, and the number of stages used in the ring oscillator, N, through the relationship:

$$f_{osc} = \frac{1}{2N\tau_d} .$$

In order to evaluate the operation speed, we calculate the delay time (switching speed) of each inverter in our 21-stage ring oscillator, τ_d=12 μs (83 kHz). This value shows a significant improvement over recent reports in the literature [90]. Achieving almost 100 kHz class operation, with device geometries that are compatible with scalable printing techniques (L_{ch}=100 μm), demonstrates the potential applicability of aerosol-synthesized CNTNs in low-cost printed electronics. Output characteristics of the 21-stage ring oscillator exhibited the same

performance one year after fabrication, which demonstrates the stability of our integrated circuits over time.

NOR and NAND logic gates are ‘universal’ building blocks of present digital circuits. They can be constructed by replacing the driving TFT of an inverter with a parallel (NOR) or series (NAND) connection of transistors. Figure 32 presents these basic logic gates based on our CNT TFTs. NOR (Figure 32 (a)) and NAND (Figure 32 (b)) gates operated by a clock (CLK) signal at 100 Hz show clear logic outputs with large voltage swings, which contribute to the robust operation of the integrated circuits.

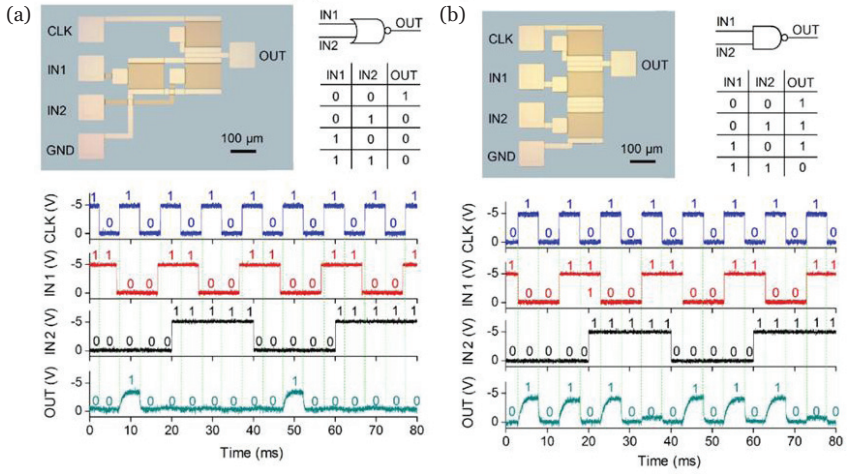


Figure 32 Optical micrograph, circuit symbol, truth table and input-output characteristics of (a) NOR and (b) NAND logic gates.

These results demonstrate the first step towards larger-scale integration of CNT TFTs, and their potential applicability for flexible integrated circuits.

5.4 Prospects and challenges

CNTN electronic material is starting to impact on the commercial world, holding a still greater promise for the future of macroelectronics with its possibilities for enabling cost-sensitive, flexible, and transparent devices. The demonstrated fabrication technology and performance levels achievable with networks of CNTs make them attractive for academic laboratories and industrial level research and development alike. However, several nanotube material and processing issues still need to be addressed in order that the future work fully exploits this material in realistic applications.

Firstly, increasing the semiconductor CNT fraction in nanotube networks is desirable. As-synthesized CNTs are typically a mixture of metallic and semiconducting tubes at a ratio of 1:2. Even though there are twice as many semiconducting tubes, the presence of metallic CNTs with density above the

percolation threshold can become a challenge for proper CNT TFT operation. Multiple approaches have been employed to minimize the effect of metallic CNTs within the as-grown network, including electrical breakdown of metallic CNTs by Joule heating [54], selective chemical modification [55, 195-199], plasma treatment [200-202], light/e-beam irradiation [203-205], or engineering the layout of CNTNs by lithographic patterning and etching [206]. However, most of these additional procedures for the removal of metallic CNTs on a substrate may have the possible drawback of device performance degradation and scalability limitations. Another common strategy adopted in this thesis is fine-tuning the density of CNTNs with metallic CNT density below the percolation threshold. In this case, control over the density of CNTNs (typically <1 CNT μm^{-2}), proper device geometry (typically channel lengths >40 μm), and network morphology (straight long tubes with Y-type tube-to-tube junctions) is critical for the optimized device performance. Electronically pure nanotubes (~99% semiconducting) could enable higher CNTN densities, which, together with their aligned assembly, provide improved drive currents for each transistor, as was recently demonstrated by the IBM research group [100]. One should note, that the purity of semiconductor-enriched samples and control over their aligned assembly are key issues for obtaining larger on-current values in such TFTs [207]. A number of innovative post-synthesis separation techniques for obtaining semiconductor-enriched samples using solution deposition methods have been proposed [83, 208]. The capability of obtaining predominantly semiconducting CNT samples, and its commercial availability, have resulted in a wide range of recent lab-scale demonstrations of TFTs based on semiconducting CNTNs, including digital integrated circuits [146], mechanically deformable and stretchable active-matrix backplanes for the development of tactile sensor arrays [111], and displays [98]. However, it goes without saying that solution techniques are time- and resource-consuming, requiring tedious processing steps that may result in contamination and structural damage, as discussed in Chapter 3.3 of the dissertation. Therefore, the main challenge for the current research work on nanotube synthesis lies in the *selective growth* of CNTs, with specified electronic type, diameter, and, ultimately, chirality. Developing a method for such preferential nanotube synthesis using a floating catalyst (aerosol) technique, with the advantage of continuous production of high quality CNTs and low temperature deposition, is a breakthrough future research topic. We have made the first steps toward this goal, by tailoring the length and diameter of as-grown CNTs via controlling the temperature and gas content within a floating catalyst reactor [149, 209]. However, significant research efforts are still required to understand the CNT growth process with defined electronic properties.

Sorting CNTs by *length* is another important material issue to be taken into account. Experimental results of our work presented in this dissertation

demonstrate the high performance of CNT TFTs based on a few micrometer-long CNTs and small bundles. Recently, a solution process for chemical purification and separation of micrometer-long semiconducting CNTs was demonstrated, and their application in TFTs showed outstanding performance in comparison with typical solution-processed networks based on shortened CNTs [210]. The researchers applied an additional gel filtration step to filter longer CNTs, however, this reduces the yield of the purification process. Increased average length of nanotubes constituting the network provides a smaller average number of nanotube junctions per transport pathway, and therefore higher device performance can be achieved. In addition, individual CNTs or small bundles are preferred for TFT applications to reduce the gate screening effect by adjacent nanotubes within a bundle.

It is also critical to address the device-level issues of CNT TFTs. Even though ensemble properties of many CNTs in a random network allow device reproducibility by eliminating variations of electronic properties between individual CNTs, device-to-device variability in CNT TFTs still demands improvements for practical industrial applications. Therefore, control over the *uniformity* of film formation over large areas plays a critical role. Using high-purity homogeneous semiconducting arrays would allow full coverage for the transistor channel, addressing the issue of uniformity control and allowing smaller channel lengths for a higher degree of device integration in the future. Proper surface passivation and process control is critical for eliminating the environmental effects and reducing interface traps for increased device consistency.

Further, let us consider the application of CNT TFTs as complementary logic gates. CNT TFTs usually show predominantly p-type behavior under ambient conditions, and PMOS configuration of integrated circuits is currently widely adopted. However, CMOS operation is desirable due to lower power consumption and larger noise margin. Therefore, *control of carriers* in CNT TFTs is a topic of active research, providing a wide range of approaches to achieve n-type doping, as recently reviewed [25, 211]. Ability to construct both p- and n-type high performing and stable CNT TFTs will allow the fabrication of more complex CNTN-based logic circuits under ambient conditions.

The next important issue is the development of *large-scale device fabrication technology* integrating CNTNs with high yield at reasonable throughput and cost. Printing techniques offer cost-effective and high-volume roll-to-roll type of processing for flexible and inexpensive electronic components with the main advances in processing and tools coming from the display and photovoltaic industries. The future of flexible, printed electronics seems to be very promising with its market share rising from $16.04 billion in 2013 to $76.79 billion by the year 2023, according to a recent report from the consulting company IDTechEx [212]. This growing demand demonstrates the need for large-area electronics

solutions. Combining CNTN material as a high performance semiconductor with existing printing methods over large areas offers significant business potential, providing new direction beyond the currently existing technologies, including flexible, and transparent electronics. Thus far, the majority of research on flexible CNT TFTs still employs lithographic techniques to fabricate high-performance devices, which requires costly materials and expensive equipment. *Lithography-free fabrication* at ambient temperature and pressure is the most attractive route for low-cost, fast fabrication of flexible devices. Improvements in device characteristics using printing processes still require significant attention for performance-demanding applications. An important advantage of the floating catalyst (aerosol) CNT technology is the potential compatibility with roll-to-roll printing of large-area flexible substrates. This opens wide horizons for the future application of this technology for high-throughput, industrial-scale, flexible and low-cost device fabrication, appropriate for e.g., signage, displays or sensing applications.

Finally, printing other device components such as *gate dielectrics* also requires separate research attention from the materials perspective. Typically, thin and high capacitance gate insulators are desirable, to enable low voltage and possibly hysteresis-free TFT operation. The currently often used ALD or sputtering techniques for the formation of gate insulators, which involve high-cost vacuum technology, should be replaced by scalable and low-cost processing methods compatible with flexible substrates. A number of reports on CNT TFTs have demonstrated the successful integration of high-*k* printed ionic gel dielectrics, to achieve flexible CNT TFTs [90, 91], which, however, pose limitations on the operating speed of transistors. A new class of ultra-thin, self-assembled nanodielectrics has also been studied for high-performance CNT TFT applications [168, 213]. Further studies on this topic deserve future research attention.

Success in the development of highly flexible and transparent CNT TFTs recently encouraged researchers to further realize stretchable devices using carbon nanomaterials for novel non-planar electronic applications. Attempts to achieve deformable and, at the same time, transparent devices include successful realization of all-carbon nanomaterial transistors, integrating CNTN channel and either CNT thin film [64-66, 214] or graphene [78, 215] material as electrodes (source, drain and gate), combined with plastic polymers as the substrate and dielectric layer. Very recently, the group led by Prof. Lee demonstrated impressive results on the realization of highly stretchable and transparent TFTs, using CNTN as the active-channel and graphene as electrodes [216]. This *new class of electronics*, capable of not only bending, but also stretching, moulding, twisting, folding, and conformally wrapping onto arbitrarily curved surfaces without significant performance degradation, is an emerging research direction which is poised to revolutionize many aspects of our daily lives, paving the way to novel

electronic devices, and incorporating electronic functionality into various stretchable media, like human skin, rubber, and plastic products. It is worth noting that, in the course of the development of highly stretchable electronics, a detailed study of strain-induced device performance under mechanical deformation is important.

To conclude, macroelectronics has the potential to open doors for emerging fields in electronics, addressing new products and new markets. Owing to the recent progress in materials and processing, the opportunity for a major breakthrough is now within sight. Application of random CNTN material for low-end electronics, characterized by large-area, larger feature size, compatibility with a continuous printing process rather than batch lithographic fabrication, and new functionality, is feasible in the near future. With further improvement of material uniformity, purity (in terms of electronic type, length, and possibly chirality), and certain processing issues, more demanding high-performance applications are possible. The success of the technology, taking CNTN material from the academic laboratory into society, depends on how quickly and effectively these challenges can be addressed. Close collaboration between different industries, with materials, printing, plastics, paper, and electronics expertise, would foster the co-development of various aspects of device production to achieve the desired level of functionality. We believe that a CNTN electronic material has a promising future for the research and development of a wide range of real-world applications.

6. Conclusions

The primary objective of this dissertation work was to demonstrate the applicability of the CNTN material, synthesized using a floating catalyst (aerosol) CVD technique, in thin film devices. In particular, we wanted to explore the potential of sub-monolayer, random CNTNs as an alternative channel material to fabricate TFTs. The ultimate goal was to demonstrate CNT TFTs and integrated circuits on flexible and transparent substrates.

The research was motivated by the knowledge of exceptional electrical, mechanical, and optical properties of individual CNTs, and the promising potential of a continuous ambient-pressure floating catalyst (aerosol) CVD synthesis system. A network of CNTs, composed of a random nanotube ensemble, is attractive for realistic technology applications, as it leverages many unique properties of its nanoscale constituents, while providing large-scale fabrication possibilities. With that in mind, we have developed a number of potentially scalable room-temperature CNTN deposition techniques, which allow positioning of CNTs in a random network configuration, directly after their gas-phase synthesis with a vertical flow aerosol reactor, onto any substrate of interest, or onto the filter paper for subsequent simple transfer. This direct dry or transfer printing of CNTNs based on aerosol methods is an alternative approach to commonly used techniques, which either rely on the local substrate-supported CVD growth of CNTs, or deposition of CNTs from solutions. Four different CNTN deposition techniques were developed: electrostatic or thermal precipitation, and filtration followed by press transfer or dissolving the filter. Aerosol methods were proposed as a solution to existing CNTN fabrication bottlenecks, offering simple, direct deposition of high-quality pristine CNTs at room temperature onto any substrate material, with controlled density. The possibility of CNTN patterned assembly by applying shadow masks during the nanotube collection via filtration or electrostatic precipitation was shown. The concept of lithography-free fabrication of CNT TFTs with a single shadow mask, placed on the substrate during the CNT deposition and subsequent electrode formation, was also demonstrated.

Taking advantage of the aerosol technology to deposit as-synthesized electronically heterogeneous (1/3 metallic and 2/3 semiconducting) CNTs, we have fabricated TFTs integrating a CNTN channel. The synthesis conditions for the CNT growth were optimized with respect to the average nanotube bundle dimensions. CNTNs comprised of individual CNTs or small bundles of around 5.4 μm up to 10 μm in length, and narrow diameter distribution with a mean value of around 1.1

nm, were found to exhibit superior performance in TFTs. The network density was controlled by adjusting the CNT deposition time so that the density of metallic CNTs was below the percolation threshold. Network density optimization for each deposition method was found to be important. We have studied the network morphology, obtained by four different aerosol-based deposition techniques, and highlighted the importance of morphological parameter control, especially nanotube alignment and junction density, for improved device performance.

TFTs based on a CNTN, optimized with respect to the network morphology and device geometry, showed high performance in terms of concurrent mobility and on/off current ratio. The transistors with nanotube networks formed by flow filtration and subsequent transfer by dissolving the filter simultaneously demonstrated an on/off ratio of 6×10^6 and mobility of 35 $cm^2V^{-1}s^{-1}$ based on the parallel plate model for the gate capacitance estimation. For sparse CNTNs as used in our case this model is known to underestimate the device mobility. Using a rigorous analytical model, the highest carrier mobility reached 1236 $cm^2V^{-1}s^{-1}$ with concurrent on/off ratio of 1.5×10^4. The impressive performance of as-deposited CNTNs was explained by the unique morphology of the network, which consisted of long (few micrometers) nanotubes with well-controlled density and predominantly Y-type of nanotube junctions, providing a larger junction area and hence lower resistance in comparison with X-junctions. In contrast, the results showing somewhat inferior performance of TFTs based on CNTNs deposited by means of electrostatic precipitation were explained by the abundance of CNT loops and curled morphology of such networks with higher junction density. We note that direct dry printing of CNTNs onto the substrate of interest, without the need to dissolve the filter, is desirable for the future compatibility of the gas-phase technique with large-scale roll-to-roll printing processes. In this sense, thermal precipitation was shown to be a new promising direct deposition method, which yields a relatively higher degree of CNT alignment within the network along the direction of the carrier gas flow in comparison with other methods. Further research on the optimization of this technique for CNT TFT fabrication is expected to yield significant results. Overall, the demonstrated successful operation of CNT TFTs show promise for the use of random CNTNs, prepared by the gas-phase synthesis method, for post-silicon technologies.

Leveraging a room temperature CNTN formation with the aerosol technology, CNT TFTs were also fabricated on flexible and transparent substrates. Integrating several CNT TFTs, flexible digital circuits were realized, including, for example, inverters, ring oscillators, NOR and NAND gates. These results demonstrate the potential of medium-scale CNT TFT integration for flexible digital circuits. It should be noted that the typical CNT TFT feature size (50-100 μm channel lengths) is compatible with established low-cost printing techniques, which, however, should be scaled down for higher density transistor integration.

The work of this dissertation demonstrates the first results on the successful application of a random network of CNTs, synthesized and deposited using gas-phase techniques, for next generation inexpensive, flexible electronics.

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The field of flexible and large-area electronics with such emerging applications as foldable displays, artificial skins and smart textiles is rapidly growing. A network of carbon nanotubes represents a new class of material with superior properties for various flexible electronic applications. This thesis focuses on exploring the applicability of carbon nanotube networks, produced using an ambient pressure floating catalyst (aerosol) technique, as an active layer for thin film transistors, the basic building blocks for large-area electronics. The methods of vacuum-free nanomaterial formation and patterning at room temperature, developed in this work, allow the use of plastic heat-sensitive substrates with minimized process steps. High-performance operation of transistors and integrated circuits, based on networks with optimized morphology, on flexible and transparent substrates is shown. The results of this work reveal the promising potential of carbon nanotube networks, prepared by gas-phase techniques, for next generation inexpensive, flexible electronics.

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