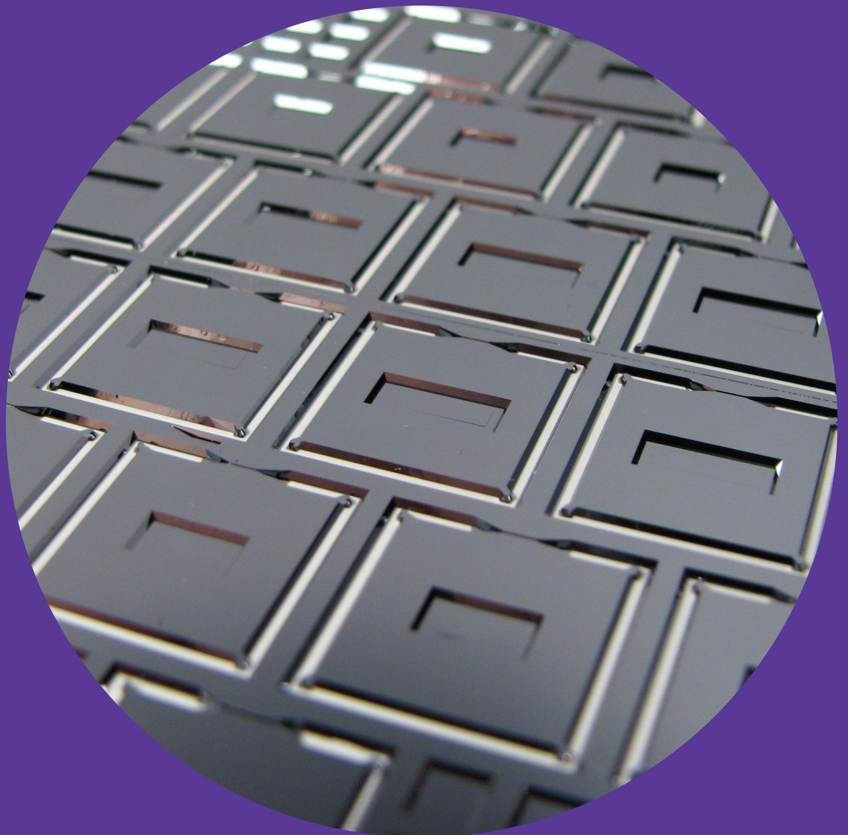
Department of Micro and Nanosciences

Microfabrication technologies for single-crystal silicon sensors

Päivi Sievilä



A!

DOCTORAL DISSERTATIONS

Aalto University publication series
DOCTORAL DISSERTATIONS 193/2013

Microfabrication technologies for single-crystal silicon sensors

Päivi Sievilä

A doctoral dissertation completed for the degree of Doctor of Science (Technology) to be defended, with the permission of the Aalto University School of Electrical Engineering, at a public examination held at the lecture hall TU1 of the school on 13 December 2013 at 12.

Aalto University
School of Electrical Engineering
Department of Micro and Nanosciences
Micro and Quantum Systems Group

Supervising professor
Professor Ilkka Tittonen

Preliminary examiners
Professor Heli Jantunen, University of Oulu, Finland
Professor Klas Hjort, University of Uppsala, Sweden

Opponent
Professor Silvan Schmid, Technical University of Denmark

Aalto University publication series
DOCTORAL DISSERTATIONS 193/2013

© Päivi Sievilä

ISBN 978-952-60-5450-6
ISBN 978-952-60-5451-3 (pdf)
ISSN-L 1799-4934
ISSN 1799-4934 (printed)
ISSN 1799-4942 (pdf)
http://urn.fi/URN:ISBN:978-952-60-5451-3

Unigrafia Oy
Helsinki 2013

Finland

A? Aalto University

Aalto University, P.O. Box 11000, FI-00076 Aalto www.aalto.fi

Abstract

Author
Päivi Sievilä

Name of the doctoral dissertation
Microfabrication technologies for single-crystal silicon sensors

Publisher School of Electrical Engineering

Unit Department of Micro and Nanosciences

Series Aalto University publication series DOCTORAL DISSERTATIONS 193/2013

Field of research Electrophysics

Manuscript submitted 12 August 2013 **Date of the defence** 13 December 2013

Permission to publish granted (date) 10 October 2013 **Language** English

☐ **Monograph** ☒ **Article dissertation (summary + original articles)**

Abstract

For decades, silicon as a high quality solid material has been playing a major role in developing state-of-the-art micromechanical sensors. In this work, the performance of silicon etching processes is evaluated, and utilized in creating devices for high precision sensing of mechanical forces. Emerging methods such as atomic layer deposition (ALD) and focused ion beam (FIB) processing are combined with established technologies in order to achieve extended functionalities.

The thesis is focused on the fabrication of components from single crystal silicon. In the developed processes, anisotropic tetramethylammonium hydroxide (TMAH) wet etching has a central role. The material behavior related to substrate specifications, doping level, and the effects inherent to thin films, is studied both during the fabrication stage and in the final structures. Furthermore, the intrinsic residual stress generation in mechanical devices is investigated.

The results were applied in successful production of mechanical sensors with superior accuracy in acoustic wave detection. The specific features of silicon-on-insulator (SOI) technology were utilized in the fabrication of released, membrane-type cantilevers that serve as highly sensitive microphones in photoacoustic spectroscopy. Moreover, ALD thin film coatings were shown to be advantageous in manipulating the functional properties of resonant silicon sensors. A step towards further device miniaturization was taken by using FIB implantation as a wet etching mask to realize 3D nanoscale structures.

Some of the developed cantilever sensors have already been implemented in commercial photoacoustic gas analyzers. In a broader perspective, the achievements related to stress control in mechanical silicon structures are of great importance in reliable production of various micro- and nanomechanical systems. All the methods employed in this work are compatible with integrated circuit (IC) processing, which enables combining the developed processes with electronic chips and the adaptation to industrial manufacturing.

Keywords silicon, silicon-on-insulator SOI, micromechanical devices, sensors, microfabrication, wet etching, focused ion beam, doping

ISBN (printed) 978-952-60-5450-6 **ISBN (pdf)** 978-952-60-5451-3

ISSN-L 1799-4934 **ISSN (printed)** 1799-4934 **ISSN (pdf)** 1799-4942

Location of publisher Helsinki **Location of printing** Helsinki **Year** 2013

Pages 114 **urn** http://urn.fi/URN:ISBN:978-952-60-5451-3

Aalto-yliopisto

Aalto-yliopisto, PL 11000, 00076 Aalto www.aalto.fi

Tiivistelmä

Tekijä
Päivi Sievilä

Väitöskirjan nimi
Yksikiteiseen piihin pohjautuvien antureiden mikrovalmistustekniikoita

Julkaisija Sähkötekniikan korkeakoulu

Yksikkö Mikro- ja nanotekniikan laitos

Sarja Aalto University publication series DOCTORAL DISSERTATIONS 193/2013

Tutkimusala Sähköfysiikka

Käsikirjoituksen pvm 12.08.2013 **Väitöspäivä** 13.12.2013

Julkaisuluvan myöntämispäivä 10.10.2013 **Kieli** Englanti

☐ **Monografia** ☒ **Yhdistelmäväitöskirja (yhteenveto-osa + erillisartikkelit)**

Tiivistelmä

Korkealaatuisten materiaaliominaisuuksiensa vuoksi piillä on viimeisten vuosikymmenten ajan ollut keskeinen asema mikromekaniikan kehityksen kärjessä. Tässä työssä arvioidaan piin syövytysmenetelmien ominaispiirteitä ja niitä hyödyntämällä valmistetaan antureita, jotka ovat äärimmäisen herkkiä mekaanisten voimien havainnoinnissa. Vakiintuneempiin tekniikoihin yhdistellään esimerkiksi atomikerroskasvatusta (ALD) ja kohdistetun ionisuihkun (FIB) avulla tapahtuvaa työstämistä uudenlaisten toiminnallisten ominaisuuksien saavuttamiseksi.

Väitöskirjassa keskitytään valmistamaan komponentteja yksikiteisestä piistä. Kehitetyt prosessit perustuvat olennaisilta osin anisotrooppiseen tetrametyyliammoniumhydroksidi (TMAH) –märkäsyövytykseen. Työssä tutkitaan materiaalien käyttäytymistä ottamalla huomioon lähtösubstraatteihin, seostukseen ja ohutkalvoihin liittyvät ominaisuudet sekä valmistuksen aikana että lopullisissa rakenteissa. Lisäksi selvitetään sisäisten jäännösjännitysten syntymekanismia mikromekaanisissa laitteissa.

Saavutettuja tuloksia hyödyntämällä valmistettiin menestyksekkäästi mekaanisia antureita, joiden avulla voidaan havaita akustisia aaltoja suurella tarkkuudella. Silicon-on-insulator (SOI) –teknologian erityispiirteitä hyväksikäyttäen toteutettiin vapautettuja, kalvomaisia palkkirakenteita, jotka toimivat erittäin herkkinä mikrofoneina fotoakustisessa spektroskopiassa. Lisäksi ALD-ohutkalvopinnoituksesta todettiin olevan etua värähtelevien piiantureiden toiminnallisten ominaisuuksien muokkaamisessa. Koska yleisenä suuntauksena on tuottaa jatkuvasti yhä pienempikokoisia antureita, kehitettiin myös menetelmä joka perustuu FIB-ioni-istutuksen käyttöön märkäsyövytysmaskina kolmiulotteisten nanorakenteiden valmistuksessa.

Osa työssä valmistetuista fotoakustisista antureista on käytössä kaupallisissa kaasuanalysattoreissa. Laajemmasta näkökulmasta katsottuna erityisen merkittäviä ovat jännitysten hallintaan liittyvät tulokset, sillä niiden avulla pystytään parantamaan monenlaisten mikro- ja nanomekaanisten laitteiden tuotannon luotettavuutta. Kaikki työssä käytetyt menetelmät ovat yhteensopivia integroitujen piirien (IC) valmistuksen kanssa, mikä mahdollistaa kehitettyjen prosessien yhdistelemisen elektroniikkakomponentteihin sekä siirtämisen teolliseen tuotantoon.

Avainsanat pii, SOI, mikromekaaniset laitteet, anturit, mikrovalmistustekniikat, märkäsyövytys, kohdistettu ionisuihku, seostus

ISBN (painettu) 978-952-60-5450-6 **ISBN (pdf)** 978-952-60-5451-3

ISSN-L 1799-4934 **ISSN (painettu)** 1799-4934 **ISSN (pdf)** 1799-4942

Julkaisupaikka Helsinki **Painopaikka** Helsinki **Vuosi** 2013

Sivumäärä 114 **urn** http://urn.fi/URN:ISBN:978-952-60-5451-3

Preface

The research reported in this dissertation has been carried out at the Department of Micro- and Nanosciences at Aalto University School of Electrical Engineering (formerly Helsinki University of Technology). To me this means a period of nine years during which Micronova center for micro- and nanofabrication has been a place for opportunities, moments of despair, cosiness and academic freedom. Most of all I will remember the unique atmosphere inside the cleanroom that I found so fascinating right from the beginning.

I would like to express my sincere thanks to Professor Ilkka Tittonen for his effort in supervising this thesis, for the continuous patience and endorsement, and for accepting even the most stubborn individual choices that I have made during all these years. Professor Jyrki Kauppinen is thanked for his innovations and collaboration related to the development of photoacoustic cantilevers. It has also been a great honor to perform SOI research together with Markku Tilli and Jari Mäkinen. Furthermore, the support of Okmetic Oyj has been invaluable in the realization of the devices and structures fabricated within this work.

I wish to thank Nikolai Chekurov for persistent pursuing towards the goals of common projects, and for teaching me that growing and learning is not possible without sometimes breaking something. Thank you also Ossi Hahtela, Ville-Pekka Rytkönen, Jussi Raittila and staff at Gasera Ltd, without your effort and the results we gained together, this thesis would not have finished. I am grateful to Veli-Matti Airaksinen for believing in me and pushing me forward on my career when I have been doubtful about myself. Ossi Kimmelma, Mika Koskenvuori, Thomas Lindvall, Osmo Vänskä, Mikhail Erdmanis, Ville Pale, Mikko Ruoho, Zhengjun Liu, Kari Iltanen, Paula Heikkilä, Sami Franssila, and the rest of the present and former staff at Micronova; thank you for collaboration and encour-

agement, not forgetting all the long and winding conversations we have had.

I would like to express my gratitude for the great financial support provided by Graduate School in Electronics, Telecommunications and Automation GETA in Finland, Finnish Foundation for Technology Promotion (TES), Nokia Foundation, Jenny and Antti Wihuri Foundation, and Walter Ahlström Foundation.

I am grateful to my family and friends; you have been there for me, accepting me as I am in greatest joys, deepest sorrows and everything in between. Tuomo, thank you for standing by me ever since the day we met when I for the very first time entered the Department of Electrical and Communications Engineering as a first year student. And finally, the warmest, grateful thoughts to my dearest kids Eero and Iiris, you have taught me such things about life that not even the best university could ever provide.

Espoo, November 6, 2013,

Päivi Sievilä

Contents

Preface i

Contents iii

List of Publications v

Author's Contribution vii

1. Introduction 1

1.1 Background . . . 1

1.2 Objectives and scope . . . 3

2. Silicon processing 5

2.1 Materials . . . 5

2.1.1 Silicon as a substrate material . . . 5

2.1.2 Thin-films . . . 8

2.2 Microfabrication . . . 12

2.2.1 Optical lithography . . . 13

2.2.2 Towards nanoscale . . . 14

2.2.3 Etching . . . 16

3. Fabricated sensors and structures 23

3.1 Mechanical silicon oscillators . . . 23

3.2 Acousto-optical SOI cantilevers . . . 25

3.2.1 Photoacoustic application and cantilever design . . . 25

3.2.2 Fabrication . . . 28

3.2.3 Functionality . . . 32

3.3 Dopant-induced stress in mechanical silicon structures . . . 34

3.3.1 Experiments . . . 34

3.3.2 Theoretical analysis . . . 36

3.3.3 Stress control 38
3.4 Nanoscale silicon structures 39
3.4.1 FIB-TMAH process 39
3.4.2 Fabricated structures 40

4. Conclusions **43**

Bibliography **45**

Publications **55**

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I O. Hahtela, P. Sievilä, N. Chekurov, and I. Tittonen. Atomic layer deposited alumina (Al_2O_3) thin films on a high-Q mechanical silicon oscillator. *Journal of Micromechanics and Microengineering*, vol. 17, pp. 737-742, March 2007.

II P. Sievilä, V.-P. Rytkönen, O. Hahtela, N. Chekurov, J. Kauppinen, and I. Tittonen. Fabrication and characterization of an ultrasensitive acousto-optical cantilever for pressure sensing. *Journal of Micromechanics and Microengineering*, vol. 17, pp. 852-859, March 2007.

III P. Sievilä, N. Chekurov, and I. Tittonen. The fabrication of silicon nanostructures by focused ion beam implantation and TMAH wet etching. *Nanotechnology*, vol. 21, 145301, March 2010.

IV P. Sievilä, N. Chekurov, J. Raittila, and I. Tittonen. Sensitivity-improved silicon cantilever microphone for acousto-optical detection. *Sensors and Actuators A: Physical*, vol. 190, pp. 90-95, January 2013.

V P. Sievilä, J. Mäkinen, M. Tilli, and I. Tittonen. Dopant-induced stress in microfabricated silicon devices. *Journal of Applied Physics*, vol. 114, 043512, July 2013.

Author's Contribution

Publication I: "Atomic layer deposited alumina (Al_2O_3) thin films on a high-Q mechanical silicon oscillator"

The author fabricated the silicon oscillators and participated in carrying out the ALD alumina coating experiments. The measurements were performed by the co-authors.

Publication II: "Fabrication and characterization of an ultrasensitive acousto-optical cantilever for pressure sensing"

The author participated in process development, fabricated the components, contributed in characterization, and prepared the manuscript.

Publication III: "The fabrication of silicon nanostructures by focused ion beam implantation and TMAH wet etching"

The planning and carrying out the experiments as well as the result analysis were performed by the author together with N. Chekurov. The author prepared the manuscript.

Publication IV: "Sensitivity-improved silicon cantilever microphone for acousto-optical detection"

The author fabricated the components and had the main responsibility of the process development. The photoacoustic measurements were performed in collaboration with J. Raittila. The author prepared the manuscript.

Publication V: "Dopant-induced stress in microfabricated silicon devices"

The author performed the experiments and the simulations and prepared the manuscript.

Other related publications, conferences, and conference proceedings to which the author has contributed:

O. M. Hahtela, A. F. Satrapinski, P. Sievilä, and N. Chekurov. Atomic layer deposited alumina (Al_2O_3) coating on thin film cryoresistors. *IEEE Transactions on Instrumentation & Measurement*, vol. 58, no. 4, pp. 1183-1187, April 2009.

A. Secchi, A. M. Fiorello, M. Dispenza, S. D'Auria, A. Varriale, A. Ulrici, R. Seeber, J. Uotila, V. Venditto, P. Ciambelli, J. C. Antolin, F. Colao, T. Kuusela, I. Tittonen, P. Sievilä, G. Maisons. Drugs and precursor sensing by complementing low cost multiple techniques: Overview of the European FP7 project CUSTOM. *Proceedings of SPIE 8545, Optical Materials and Biomaterials in Security and Defence Systems Technology IX*, vol. 8545, pp. 85450G1-6, November 2012.

P. Sievilä, N. Chekurov, and I. Tittonen. Silicon nanostructure fabrication by FIB writing and TMAH wet chemical etching. *Nanotech Conference & Expo 2010*, Anaheim, CA, USA, 21-25 June, 2010.

P. Sievilä, J. Fonsen, O. Hahtela, N. Chekurov, J. Kauppinen and I. Tittonen. Optically detected, framed silicon cantilever for high precision acoustic sensing. *Transducers'07 & Eurosensors XXI*, Lyon, France, 10-14 June, 2007.

Abbreviations

Al	Aluminum
ALD	Atomic layer deposition
Al_2O_3	Aluminum oxide, alumina
AR	Anti-reflective
Ar	Argon
B	Boron
BHF	Buffered hydrofluoric acid
BOX	Buried oxide
BSOI	Bonded silicon-on-insulator
CF_4	Carbon tetrafluoride
CH_4	Methane
CH_3COOH	Acetic acid
CHF_3	Trifluoromethane
CMOS	Complementary metal oxide semiconductor
CO	Carbon monoxide
CO_2	Carbon dioxide
c-Si	Crystalline silicon
DRIE	Deep reactive ion etching
DSP	Double-side polished
EBL	Electron beam lithography
EDP	Ethylenediamine pyrocatechol
FEM	Finite element modelling
FIB	Focused ion beam
FT-IR	Fourier transform infrared
FWHM	Full width at half maximum
Ga	Gallium
H_2	Hydrogen
HF	Hydrofluoric acid
HNO_3	Nitric acid

H_2O	Water
IC	Integrated circuit
IPA	Isopropanol
IR	Infrared
K	Potassium
KOH	Potassium hydroxide
LMIS	Liquid metal ion source
MEMS	Microelectromechanical systems
NEMS	Nanoelectromechanical systems
NIL	Nanoimprint lithography
NNEA	Normalized noise equivalent absorption
N_2O	Nitrous oxide
O_2	Oxygen
OH^-	Hydroxide ion
P	Phosphorus
PAS	Photoacoustic spectroscopy
PECVD	Plasma enhanced chemical vapour deposition
RF	Radio frequency
RIE	Reactive ion etching
rms	Root mean square
Sb	Antimony
sccm	Standard cubic centimeters per minute
SEM	Scanning electron microscope
SF_6	Sulfur hexafluoride
Si	Silicon
SiH_4	Silane
SiN_x	Silicon nitride, non-stoichiometric
SIMS	Secondary ion mass spectrometry
SiO_2	Silicon dioxide
SiO_xF_y	Silicon oxyfluoride
SNR	Signal-to-noise ratio
SOI	Silicon-on-insulator
SSP	Single-side polished
TEM	Transmission electron microscope
TMA	Trimethyl aluminum, $Al(CH_3)_3$
TMAH	Tetramethylammonium hydroxide, $(CH_3)_4NOH$
UV	Ultraviolet

Symbols

A_c	Area of the cantilever
C	Concentration
d	Thickness
d_b	Thickness of a beam
d_f	Thickness of a film
E	Young's modulus
k_0	Cantilever spring constant
k_{gas}	Gas spring constant
l	Length
$n_{Al_2O_3}$	Refractive index of alumina
n_{Si}	Refractive index of silicon
P	Power
p	Pressure
Q	Quality factor
R	Radius of curvature
R_{AR}	Reflectivity with an antireflection coating
R_{calc}	Calculated radius
R_{meas}	Measured radius
R_{Si}	Reflectivity of a silicon surface
V_{eff}	Effective volume
w	Width
β	Lattice expansion coefficient
γ	Ratio of specific heat capacities
$\Delta\epsilon$	Misfit strain
Δh	Deflection
κ	Curvature
ν	Poisson's ratio
σ	Stress

1. Introduction

1.1 Background

Silicon, having a traditional role as a semiconductor material, is an unbeatable choice for various applications due to its electric, mechanical, optical and thermal properties. With the help of dopant atoms, the electrical behaviour can be tailored from high resistivity to high conductivity. Silicon has excellent stress-strain behaviour and linear elasticity that enable highly repeatable and long-term stable operation in mechanical applications. The advantages include also the capability to manufacture and process material with perfect crystal orientation, and the possibility to polish the surface to almost atomic smoothness (rms roughness ~0.1 nm). Silicon is transparent to microwaves and infrared light that makes possible the combination of devices with fiber optic systems operating at telecommunication wavelengths. Moreover, the thermal properties of silicon are suitable for thermo-mechanical actuation.

Most of the existing microfabrication infrastructure - cleanrooms, wafer technologies and processing equipment - has originally been developed for filling the ever-growing needs of integrated circuit (IC) industry. In addition, it provides a superior platform for evolving micro- and nanoelectromechanical systems (MEMS/NEMS) [1, 2], photonic and optoelectronic devices [3, 4], and solar power systems [5].

The potential of silicon in micromechanics was first reviewed by K. E. Petersen in the beginning of 1980's [6]. Nowadays its role has been established in commercial fabrication of many mechanical components such as switches, filters, oscillators, fluidistic devices, medical- and biochips, microphones, accelerometers, gyroscopes, flow detectors, micromirrors, and cantilever sensors [7–12].

The typical detection or generation of the mechanical signal is based on utilizing piezo- or thermoelectric, resistive, capacitive, magnetic, optic, or resonant characteristics. To ensure reliable and reproducible device performance, attention must also often be paid on the strict control of critical dimensions, surface quality, and stresses already at the designing phase [13, 14].

In addition to the requirements set by the final application, the fabrication techniques to be applied set their own limitations that need to be considered. One important aspect is the need for high level of cleanliness. Hence, the control of particles and traces of organic impurities is crucial in the processing of any kinds of structures involving micro- or nanoscale dimensions. Besides, MEMS and CMOS components are often handled in the same laboratories or even integrated together in the final devices. Thus, potential sources of metallic impurities must often be taken into account throughout the whole microfabrication chain [15, 16].

A proper MEMS device design starts by a considered selection of the substrate material. The classical, and in many cases the most cost-effective approaches are based on surface or bulk micromachining, whereas the growing demands of advanced sensor production are often filled by selecting more specialized substrates such as silicon-on insulator (SOI) wafers [17–19]. As important as the substrate are the applied thin-film materials that are needed both during the fabrication and for building up structural parts [20]. Furthermore, components in various mechanical, electrical and optical applications benefit from thin-film coatings that are utilized, *e.g.* for functional or protective purposes [21].

Likewise in IC-production, the trend in developing mechanical devices is towards scaling down their dimensions [22,23]. The miniaturization alters the physical properties of sensor structures, which breaks new ground for advanced detection schemes. As an example, silicon nanowires can be used as sensors in medical applications due to their high surface-to-volume ratio and dimensions close to the species to be detected [24]. The nanoscale size sets challenges to microfabrication processing, especially because the character of mechanical components, in contrast to electronics, often relies on 3D structures with remarkable height differences.

The overall motivation behind this work is related to the continuous drive to build up new processes, devices, and applications on the underlaying infrastructure by using commercial equipment, microfabrication compatible materials, and established processing techniques in new con-

texts or in a non-standard way. As a result, novel component designs, as well as fabrication and prototyping methods that are easy to adapt to industrial usage are achieved.

1.2 Objectives and scope

The aim of this thesis is to develop mechanical, crystalline silicon based micro and nanodevices. The understanding of the special characteristics of materials, microfabrication, and final devices alike is of great importance in producing functional, state-of-the-art components. In this work, a special attention is paid to wet etching as a fabrication method, and devices with released structural parts. The scope of the work and the interconnections between the themes discussed are visualized in Fig. 1.1.

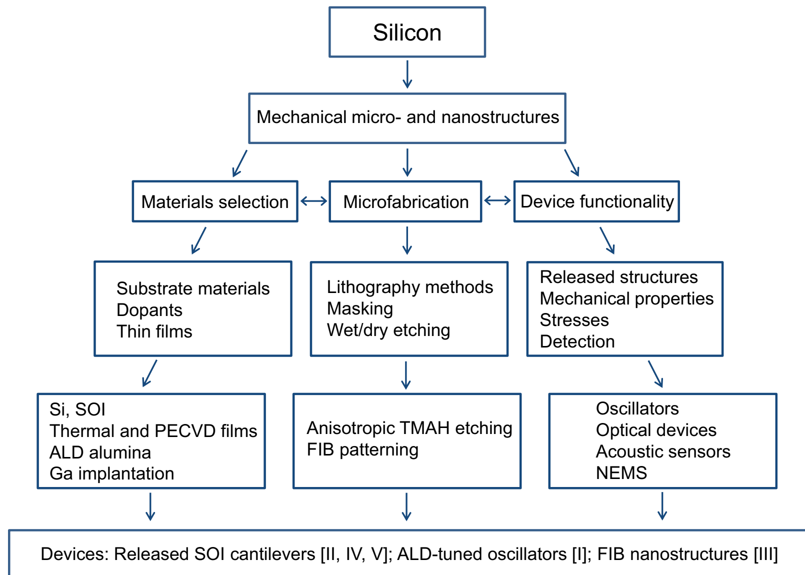


Figure 1.1. Scope of the thesis. The pyramidal structure shows how the results of the publications I-V (at the lowest level) are related to a more general context.

The compiling part of the dissertation summarizes the results presented in five journal articles, each providing a partial contribution to the research field of interest. In Publication I, high-Q optomechanical silicon oscillators for high-precision sensing applications are fabricated. The potential to use atomic layer deposited (ALD) coatings in fine tuning the mechanical properties of resonant structures and utilize them as protec-

tive or functional thin-films is studied. Publication II and Publication IV concentrate on the process development, microfabrication and characterization of optically detected acoustic SOI cantilevers. This novel type of microphone is designed to meet the demands of ultimate sensitivity in photoacoustic spectroscopy. Because the operation of these components as well as many other MEMS devices relies on thin, released parts, adequate stress control is an important aspect. This is discussed in Publication V, describing particularly the effects of doping and thin-film materials selection on residual stress in silicon. Publication III concentrates on focused ion beam (FIB) patterned nanoscale structures. The motivation is related to the fabrication of 3D devices having applications in MEMS/NEMS, fluidistics, and optics.

The structure of this compilation is as follows: Chapter 2 reviews the materials and fabrication methods commonly used in microsystems technology, emphasizing the features utilized in the experiments of this thesis. Chapter 3 concentrates on the achieved results, discussing the investigated fabrication processes and the resulting structures and devices. Finally, the conclusions are presented in Chapter 4.

2. Silicon processing

This chapter reviews the basic concepts related to microfabrication, with an emphasis placed on silicon processing. The properties of the starting material - bulk silicon and SOI wafers - are discussed, as well as several thin-film deposition techniques needed for adding materials during the fabrication. The desired patterns are typically transferred to the substrate by the means of lithography, defining the areas where the material can be removed by etching. This is performed by using either liquid or gaseous chemicals. The processing of most of the structures presented in this work is based on wet etching that is therefore covered here in more detail. Methods for fabricating nanoscale structures by focused-ion-beam (FIB) -based processes are also introduced.

2.1 Materials

2.1.1 Silicon as a substrate material

The microfabrication processing usually starts by wafer selection. The final devices are built in and on the top of this base material. Crystalline silicon (c-Si) substrates are extensively employed in commercial semiconductor applications. They serve also as a starting material for all the structures fabricated within this work. Thus the focus is on describing the properties of single crystalline silicon, in contrast to amorphous silicon in which the atomic order is random, or polycrystalline silicon consisting of multiple, small, regularly ordered crystals. The discussion of other types of semiconductors and insulators as substrates is excluded, even though they are widely used in certain fields of microsystems technology.

Crystal structure

In single crystalline silicon the atoms are organized regularly into a cubic diamond lattice throughout the crystal, Fig. 2.1 (a). Each Si atom has four neighbouring atoms in a tetrahedral arrangement, and the lattice constant is 5.431 Å. Viewing the crystal from different directions reveals atoms arranged in several planes. This crystallographic orientation is described by *Miller indices* (hkl). The most important crystal planes of silicon are (100), (110), and (111), as illustrated in Fig. 2.1 (b) [25].

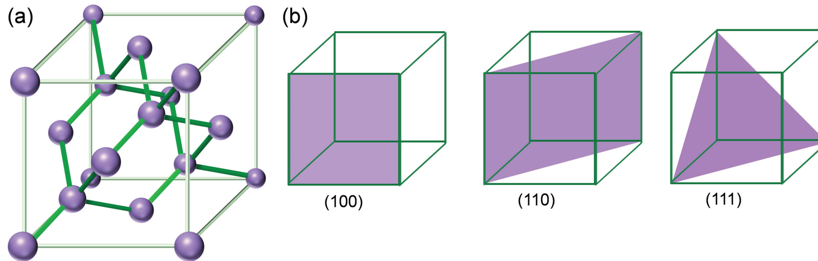


Figure 2.1. (a) Cubic diamond lattice of silicon. (b) The most important silicon crystal planes.

Especially from the mechanical engineering point of view, the crystal orientation is a critical aspect since it has an effect on the material parameters such as *Young's modulus* (E) describing the stiffness of a material [26]. As a material, silicon is strong and brittle; it deforms fully elastically until it breaks. The brittleness is exploited in wafer dicing, in which the cleavage propagates along the crystal planes enabling an easy way to divide a larger sample into small chips. The crystal orientation has also remarkable effects on the microfabrication properties of silicon, as will be shown later in this chapter.

Bulk silicon wafers are widely available in various sizes for a moderate price. The typical diameters are 100/150/200/300 mm, and the thickness varies from $\sim$ 300 to 800 μm. The wafer is cut along a desired crystal plane, <100> being the most commonly used orientation of the surface. Depending on the purpose of use, either one or both surfaces of the wafer are polished with a root mean square (rms) roughness of approximately 0.1 nm [27]. Whereas single-side polishing (SSP) is enough in many IC applications, double-side polishing (DSP) is often necessary in MEMS processing, in which double-sided patterning or wafer bonding takes place.

Doping

The introduction of dopant atoms into silicon crystal lattice is a fundamental process used to modify the electrical characteristics of the substrate. In addition to integrated circuits, doping plays a central role in many MEMS applications enabling the function of various conductors and contacts, electrostatic devices, resistors, and piezoresistive elements. The doping type, p or n, refers to the character of silicon as a semiconductor material. P-type dopants such as boron, aluminum, and gallium act as *acceptors* providing holes as free charge carriers in the crystal, whereas n-type dopants like phosphorus, antimony, and arsenic are *donors* supplying excess electrons. The concentration of dopants defines the silicon resistivity, with densities of approximately 10^{14} - 10^{16} cm^{-3} considered light doping and 10^{18} - 10^{19} cm^{-3} high doping. The doping of bulk material takes place during the silicon crystal growth. Dopants can also be added locally to only certain areas of a wafer during device processing by means of ion implantation or diffusion.

Besides electrical properties, the presence of dopants leads also to mechanical effects such as silicon lattice contraction (B, P) or expansion (Sb) proportional to the dopant concentration [28–30]. If there is gradient in the dopant distribution in vertical direction, the lattice volume change may induce significant stress and deformation of mechanical silicon devices as was shown in Publication V.

Doping can also be utilized as a part of the microfabrication process because it behaves as an *etch stop*: the highly doped areas of silicon are not dissolved in specific wet etchants [31, 32]. Especially boron doping exceeding 10^{19} cm^{-3} is commonly used for etch stop purposes. In nanoscale structuring, focused ion beam implanted gallium shows similar type of resistance towards both wet and dry etching [33–36], [Publication III].

Silicon-on-insulator substrates

SOI wafers are customized substrates for specific end applications. The structure is made up of a bulk silicon wafer (handle), a topmost, thin silicon (device) layer, and a silicon dioxide (SiO_2) (buried oxide, BOX) film between them, Fig. 2.2. The properties like dopant type, resistivity, thickness and crystal orientation can be selected separately for both silicon wafers. The most typical reasons for working with SOI in mechanical applications are related to its potential for accurate and simple fabrication of devices with less processing steps. The advantages are related to the

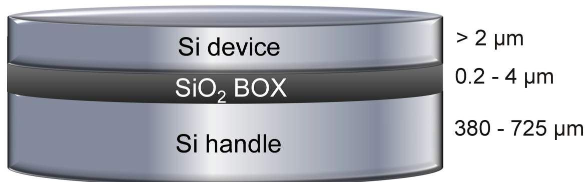


Figure 2.2. Silicon-on-insulator wafer structure. The dimensions are typical for bonded SOI wafers used in MEMS applications [27].

buried oxide that can serve, for example, as an electrical insulator, an etch stop layer for both dry and wet etching of silicon, or a sacrificial layer for released structures.

In CMOS devices, thin-film SOI, manufactured in most cases by the Smart Cut method, is widely employed. The typical film thicknesses in these applications range from tens to a few hundreds of nm. In MEMS, instead, the films are thicker: the common device layer thickness varies from 2 to 100 μm and the buried oxide thickness from hundreds of nanometers to a few microns [27, 37]. The fabrication of such wafers is in most cases based on bonded SOI technique (BSOI), in which an oxidized bulk wafer is joined to a plain wafer and annealed at high temperature near 1 000 °C for bond strengthening, followed by thinning and polishing one of the wafers to a desired device layer thickness [27]. BSOI substrates serve as a basis for the structures fabricated in Publication II, Publication IV and Publication V.

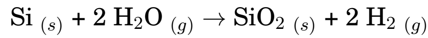
2.1.2 Thin-films

The possibility to grow high quality thin-films is a central feature in microfabrication. A short introduction is given about selected techniques for the growth of thin-films that play an essential role in the fabrication processes developed in this thesis. The focus is on dielectric materials, and hence metals, that are typically deposited by sputtering or evaporation, are not discussed in more detail.

Thermal oxidation

Silicon dioxide is probably the most common thin-film material in microtechnology. Besides being an integral part of the SOI substrate construction as discussed above, it is typically applied as a dielectric or insulating material in final devices, and as a diffusion barrier or a hard etching mask during silicon processing [38].

In thermal oxidation, atoms at the surface of the silicon substrate react with oxygen at high temperatures (from 800 to 1 200 °C). Very thin films (< 100 nm) may be deposited by *dry oxidation* employing pure oxygen gas, but for thicker films *wet oxidation* is used. In this case the reaction takes place in steam:



$$Si_{(s)} + 2\,H_2O_{(g)} \rightarrow SiO_{2\,(s)} + 2\,H_{2\,(g)}$$

The oxidation rate is dependent on the temperature and the oxidant partial pressure, and is typically a few hundreds of nm/h. When the film thickness increases, the rate slows down as the oxidizing species must diffuse through the oxide to the silicon-oxide interface. The growing oxide is amorphous, and its molar volume is over the double of that of silicon. Thus the amount of silicon consumed during oxidation is approximately 45 % of the thickness of the SiO_2 film. There is also a difference in thermal expansion coefficients: expansion of silicon is approximately five times higher than that of SiO_2, leading to a stronger contraction of the substrate at the cooling phase after oxidation. As a consequence of these factors, the oxide film takes a larger volume compared to silicon and is under compressive stress as seen in Fig 2.3.

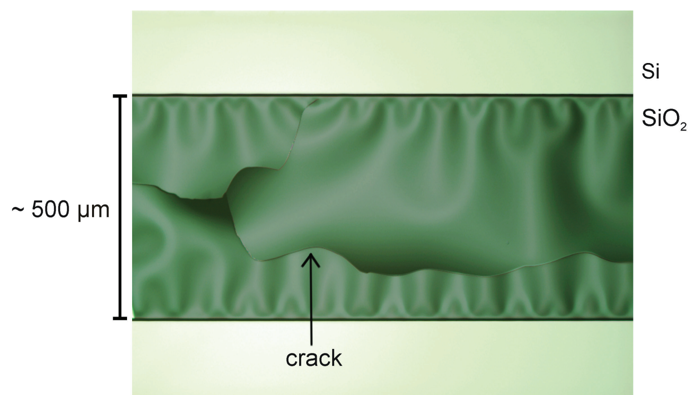


Figure 2.3. Optical microscope view shows a volume difference induced crack in a 1 μm thick, released thermal SiO_2 film .

Due to the growth mechanism, the dopant elements in silicon crystal also participate in the oxidation process. The difference of the chemical potentials in oxide and silicon induces *segregation* of the dopant atoms near the interface. As a result, some elements, *e.g.* phosphorus, accumu-

late on the silicon side, whereas others, such as boron, escape into the oxide [39].

PECVD

In plasma-enhanced chemical vapour deposition (PECVD), the growth of thin-films is based on chemical reactions of plasma-activated source gases. The method is not considered as an actual high temperature process since the temperature is only around 300 °C, which is beneficial in many applications [40]. The deposition is relatively fast and the rate, typically tens of nm/min, is linear and independent of the film thickness.

Silicon oxides and nitrides are common films produced by PECVD. The growth of SiO_2 differs from thermal oxidation because silicon at the wafer surface is not participating in the reaction. Instead, the film deposition takes place by letting the source gases, *e.g.* silane SiH_4 and nitrous oxide N_2O, react on the substrate. Unfortunately, the quality of PECVD films is not comparable to the films obtained by high temperature processing; they suffer from pinholes, stresses, and poor etch resistance [41]. Film densification and quality improvement are nevertheless achievable by post deposition annealing [42]. This property was exploited in the fabrication processes investigated in Publication IV and Publication V.

ALD

Atomic layer deposition (ALD) technique is a self-limiting method based on sequential surface reactions of precursor gas molecules. Because the thin-film growth is linear and depends directly on the number of growing cycles, it is possible to control the thickness of the film at the atomic level [43, 44]. The typical temperature for ALD processing is 200 - 300 °C. The ALD process cycle is illustrated in Fig. 2.4.

Compared with other thin-film deposition techniques such as evaporation, sputtering, or PECVD, ALD has an advantage of high conformality: even a complex surface topography with steps, shaded areas and deep trenches is covered with a uniformly thick film. This ability is beneficial especially in miniaturizing semiconductor devices, but also in the processing of MEMS components since they typically contain three-dimensional structures [45, 46].

ALD has a capability of producing a wide range of both conducting and insulating layers. Multilayered structures are achievable with a single processing step, because several types of films can be deposited consecutively. In the processes discussed within this thesis, ALD alumina Al_2O_3

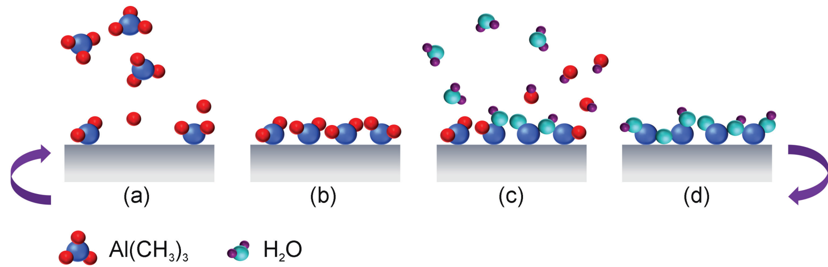


Figure 2.4. ALD process cycle for Al_2O_3 growth. The first precursor is pulsed to the chamber and it reacts with the substrate surface (a). The excess vapor and by-products are purged away with a carrier gas (b) before the second precursor that reacts with the first precursor is brought in (c). After another purging step, a new cycle is ready to begin (d).

is applied [47]. It is a beneficial material in MEMS fabrication especially due to its exceptional property to serve as an ultra-thin, high selectivity mask in cryogenic silicon dry etching [48]. In Publication I its effects as coatings on mechanical oscillators are studied.

Stress

Thin-film related stress is a challenge in many applications. The operation of many micromechanical devices like micromirrors, various kinds of membrane- and cantilever-type sensors and RF-MEMS components is based on thin, released structures. Thus attention must be paid especially to residual stresses left in these devices after fabrication processing, as they may induce deformation, affect the mechanical properties and even prevent their functionality [49]. Stresses can be controlled by a careful selection of materials and processing methods, and sometimes by depositing additional compensating layers.

The stress can be *extrinsic*, *i.e.* caused by the mismatch of thermal expansion coefficients, or *intrinsic*, meaning that it originates from the thin-film material structure and the growth process [50]. Depending on the materials, the stress leads to either tensile or compressive effects, Fig. 2.5.

A common way to determine the stress is to measure the curvature of the thin-film coated structure [51]. Stoney's formula relates the radius of curvature R to stress σ [52]. For cantilever shaped structures that are in the focus of this thesis, the curvature is often practically determined by measuring the deflection of the free end Δh. The difference of stresses between the upper and lower surfaces is given as:

$$\Delta\sigma = \frac{Ed^2}{6R(1-\nu)} = \frac{\Delta h E}{3(1-\nu)}\left(\frac{d}{l}\right)^2, \quad (2.1)$$

where d is the thickness of the cantilever, E is the Young's modulus, and ν is the Poisson's ratio. The latter form follows from the assumption that the deflection is small compared with the cantilever length l, and thus $R = l^2/2\Delta h$ based on geometry. The use of Stoney's equation in the presented form is limited to the situations in which the film is much thinner compared with the substrate thickness. As an example, when the film thickness is 3.5 % of that of the substrate, and the elasticity is assumed to be homogeneuos throughout the structure, the error in the curvature is 10 % [53]. The thin film assumption is not valid for the structures of Publication V, but more accurate approximations are applied, as will be discussed later in Section 3.3.2.

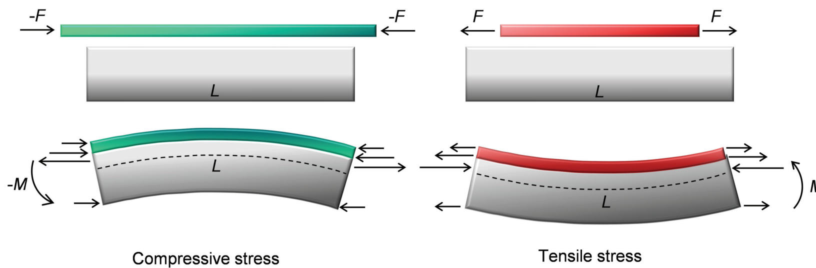


Figure 2.5. Thin-film induced stresses. A larger film is compressed, whereas a film with a smaller volume experiences tensile stress. The dashed line shows a neutral axis that remains unstressed when the structure bends.

2.2 Microfabrication

In microfabrication, patterns are usually transferred onto substrates by means of lithographic patterning and subsequent etching. Photolithography is the traditional and dominating patterning method in semiconductor device production. For nanoscale structuring, more advanced - and unfortunately often also more time consuming - patterning techniques based on, *e.g.* direct writing by electron or ion beams are needed [54]. Besides patterning, also etching plays a critical role in defining the shape and dimensions of the final structures.

2.2.1 Optical lithography

The principle of conventional photolithography is presented in Fig. 2.6: A photomask (glass plate with a chromium pattern) is aligned with a wafer having a layer of spincoated photosensitive polymer resist on it. The exposure by UV light (approximately 1 s) changes the solubility of the illuminated areas of the resist in a developer. The generated pattern can then be used, *e.g.* for etching the underlaying material away. As a replicating technique, the throughput of optical lithography in serial production is hundreds of wafers per hour.

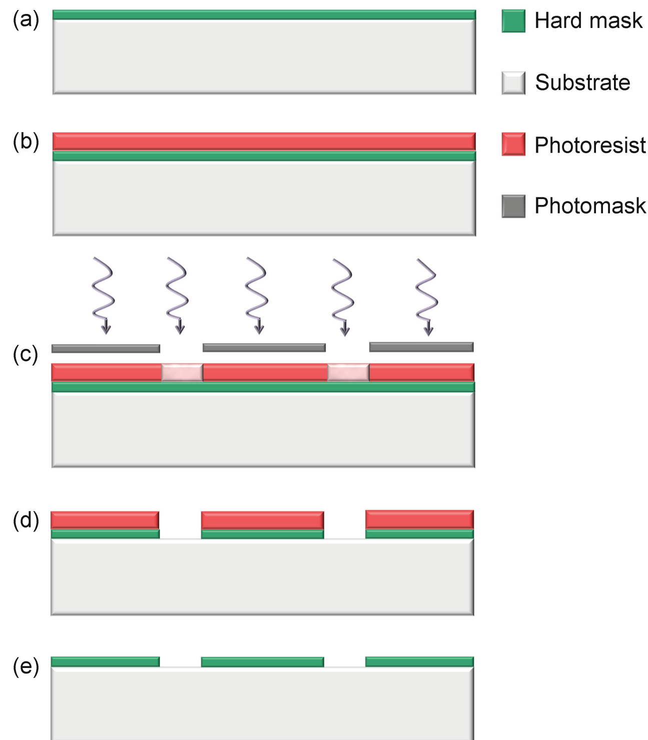


Figure 2.6. Principle of thin-film patterning by photolithography. (a) Thin-film deposition; (b) photoresist spinning; (c) exposure through a photomask (positive process); (d) resist development and thin-film etching; (e) resist removal.

Often the main concern related to patterning is the *resolution*. In contact and proximity approaches, in which the mask is brought to an intimate contact with the wafer, or to a distance of some microns to avoid mask damage, the resolution is limited by light diffraction. Also the photomask pattern size has its own contribution, where sub-micron features are increasing substantially the price. The flatness of the surface is often

a resolution-limiting factor especially in mechanical applications, as the surface to be patterned may cover vertical dimensions of several microns. In conclusion, in MEMS an accuracy of ~ 1 μm is achievable in optimized circumstances, but more often in practice a few microns is a more realistic goal.

Improvement of resolution is achievable by using projection optics: after the photomask the light passes through a lens system providing on a wafer an image with a reduced magnification. Projection optics is typically used in stepper lithography utilized in IC fabrication for chipwise exposure. By using deep UV light having shorter resolution-limiting wavelengths, and an advanced reduction optics, the minimum resolvable linewidth (a half-pitch) is in the order of tens of nm [55, 56].

In addition to resolution, the accuracy of the lateral positioning, *i.e.* the *alignment* is crucial in processes with multiple lithographic steps. Particularly in MEMS applications, double-sided processing is often required, which involves aligning the pre-existing structures on one side of the wafer to the pattern to be exposed on the other side. In contact lithography, the positioning with an accuracy in the order of a few microns is achieved by using alignment marks on the photomasks and with the help of the exposure tool that enables to move the substrate and the mask mechanically with high precision. Double-sided patterning and careful alignment along crystal directions are key features in the processes developed in Publications I, II, IV, and IV.

2.2.2 Towards nanoscale

For nanopatterning, beams with shorter wavelengths are required. In electron beam lithography (EBL) no photomask is used but the pattern is written pixel by pixel on a resist coated substrate. Features less than 10 nm in width are achievable but at the cost of low throughput and challenging patterning of larger areas [57]. The same restrictions are related to focused ion beam (FIB) patterning, which is discussed more in detail below. An applicable low-cost method for mass production is nanoimprint lithography (NIL), in which a hard stamp with a nanostructured surface mechanically deforms the resist material replicating the original pattern [58].

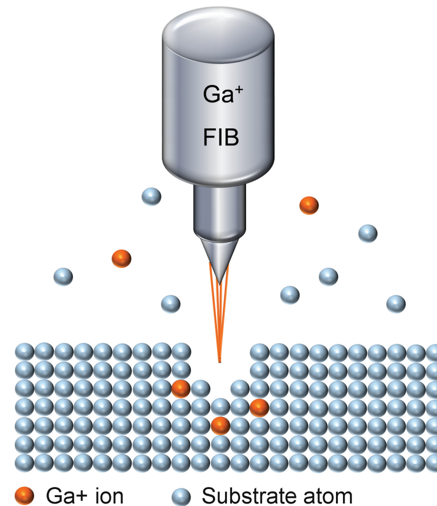


Figure 2.7. Focused ion beam milling. In parallel to the sputtering of the substrate atoms, a certain amount of primary Ga^+ ions is implanted into the sample.

Focused ion beam patterning

In FIB processing, a well focused beam of ions is scanned over the substrate. The technique can be used for multiple functions involving physical milling, imaging, material deposition, ion-assisted etching, and implantation [59]. The conventional way to use FIB is milling: the energetic ions induce sputtering of the surface atoms, and the desired freeform pattern can be directly written on the substrate without using any resist and subsequent etching, Fig. 2.7. The applications of FIB include photomask and circuit repair, transmission electron microscopy (TEM) sample preparation, and nanostructure fabrication especially on prototyping level [60, 61]. One advantage is the capability to pattern on irregular surfaces with slopes or other 3D structuring that are excluded with methods requiring resist coating.

Most FIB tools are based on gallium ions extracted from a liquid metal ion source (LMIS) [62]. The acceleration voltage of the ions affects the accuracy and efficiency, and thus in most cases the use of the highest possible value (30 kV in the experiments of this work) is advisable. The ion dose delivered to the sample is defined as the number of ions passing through a unit area. Milling requires a higher dose (> 10^{18} ions/cm^2 for silicon), whereas the use of lower doses results in gallium implantation. The beam size and thus also the spatial resolution are affected by the beam current. As a consequence, high resolution patterning increases the processing time. With small currents (1-10 pA), a spot size of approx-

imately 10 nm is achievable (full width at half maximum FWHM for a Gaussian shaped beam).

The use of local gallium implantation as an etching mask opens up new opportunities for developing nanofabrication processes. In silicon processing, the implanted areas become protected but the material around them can be removed by means of plasma or wet chemical etching at rates that are very fast compared with direct FIB milling. The method has been utilized for realizing various types of configurations including MEMS devices [63], nanosensors [35], and layer-by-layer manufactured 3D structures [64]. In addition to silicon, the corresponding masking effect has been reported in certain thin-film materials. Ga^{+} -implanted PECVD nitride (SiNx) is resistant to CF_4 reactive ion etching, whereas aluminum oxide (Al_2O_3) shows an opposite behaviour as the implanted areas are etched with a higher rate in phosphoric acid etchant, enabling a negative patterning scheme [65, 66]. Combined with silicon patterning, the use of thin-films as an intermediate layer helps to protect the bulk material from undesired lattice damage and dopant contamination [67].

2.2.3 Etching

The patterning of the substrate is frequently followed by etching. Material from these areas, that are not protected by an etch resistant mask, is chemically removed. *Isotropic* etching means that the reaction proceeds at an equal rate in all directions, Fig. 2.8 (a). Silicon dioxide etching in buffered hydrofluoric acid (BHF) is a typical example of an isotropic process. If the rate is direction-dependent, the process is *anisotropic*, Fig. 2.8 (b) and (c). *Selectivity* describes the ratio between the etch rates of two materials or crystal directions. When liquid-phase chemicals are used, the process is called wet etching, whereas dry etching takes place typically in gas and plasma.

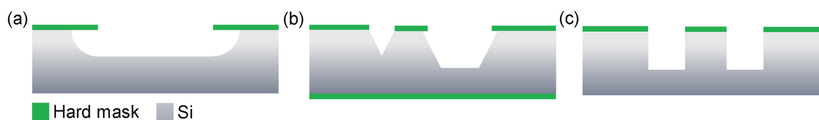


Figure 2.8. Etching profiles resulting from (a) isotropic etching; (b) anisotropic wet etching of <100> Si; (c) anisotropic dry DRIE etching.

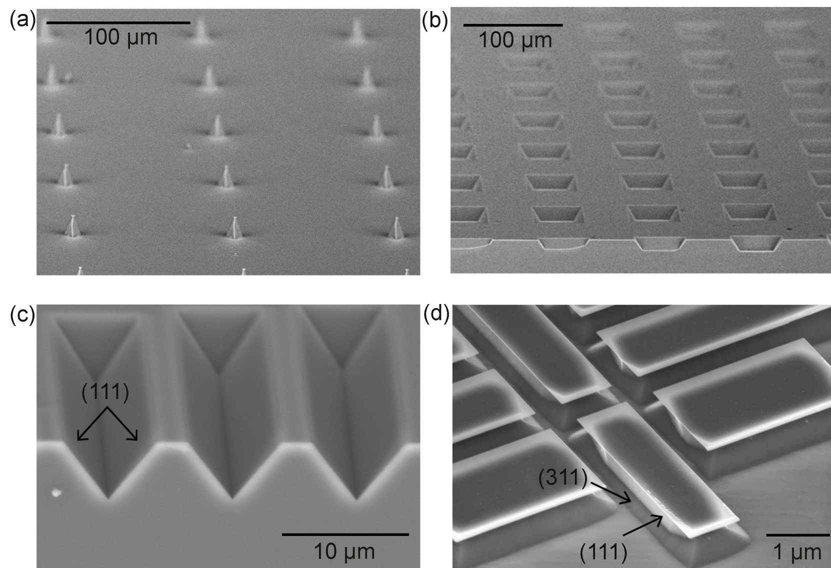


Figure 2.9. Anisotropically wet etched c-Si structures: (a) tips; (b) wells; (c) (111)-plane-limited v-grooves; all on a <100> oriented substrate. (d) Patterns etched with a rectangular mask (shown on the top) on a <110> substrate. The sidewalls are vertical and determined by the (111) planes. Self-limiting slow etching planes (311) are seen to appear at the bottom.

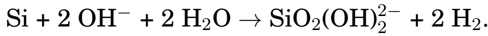
Wet etching of silicon

Wet etching is a widely used mass production method in silicon processing. Common structures include grooves, membranes, cantilever sensors, resonators, sample wells, tips, and microfluidic channels. Scanning electron microscope (SEM) images in Fig. 2.9 show examples of characteristic wet etched structures. For isotropic etching, a mixture of nitric acid (HNO_3), hydrofluoric acid (HF), and acetic acid (CH_3COOH) is the most common choice. Here the focus is, however, on anisotropic, crystal orientation-dependent wet etching.

In certain hot alkaline solutions the etch rate of silicon depends strongly on the crystal plane exposed to the etchant [68]. Thus the dimensions of the final structures are determined by the orientation of the chosen substrate in addition to the mask patterns. Aqueous solutions of potassium hydroxide (KOH), ethylenediamine pyrocatechol (EDP), and tetramethylammonium hydroxide (TMAH) are the most common anisotropic silicon wet etchants [69–71]. Potassium is an impurity to be avoided in a cleanroom environment because it may introduce unwanted mobile K^+ ions. EDP, instead, is poisonous and carcinogenic. Therefore, the use of TMAH

($(CH_3)_4NOH$) is advisable in laboratories with both IC and MEMS processing, and when the CMOS-compatibility of the sample is an important aspect.

The chemical reaction of alkaline silicon etching is given as [72]:



$$Si + 2\,OH^- + 2\,H_2O \rightarrow SiO_2(OH)_2^{2-} + 2\,H_2.$$

Etching is mainly an electrochemical process. When the hydroxide ions catch the free bonds at the silicon surface, their stronger electronegativity diminishes the strength of the bonds to the other atoms in the lattice, and silicon is dissolved. A clear visual indicator of the reaction is hydrogen release, seen as bubbles forming on the substrate surface.

Examples of mask pattern alignment and the corresponding profiles of the structures after anisotropic wet etching are shown in Fig. 2.10. The

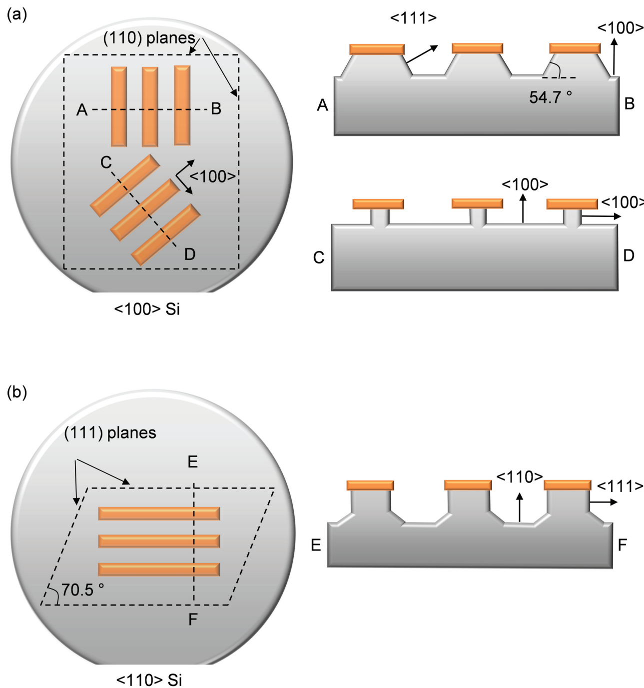


Figure 2.10. Pattern alignment and crystal plane dependency of anisotropic silicon wet etching. (a) The patterns with a cross-cut A-B show the typical alignment on a <100> substrate, leading to the formation of characteristic V-grooves between the lines when the etching proceeds. Instead, as a result of the pattern alignment 45° off the <110> directed main axes on the substrate, the (100) planes appear in parallel to the direction of the lines, and perfectly vertical fast etching sidewalls are obtained, C-D. (b) For a <110> oriented substrate, the self-limiting shape is a U-groove, E-F.

atoms in silicon crystal are the most tightly packed in the <111> direction, that correspondingly shows the slowest etch rate. In addition, the Si atoms have only one free bond to catch the OH^- ions instead of the two bonds of the faster etching (100) plane. In <100> silicon etching, the 54.7° angle between the (100) and (111) planes is a characteristic feature. When the (111) planes meet, the etching terminates.

Due to the anisotropy, care must be taken when rectangular shapes are etched because at convex corners fast etching (311) planes are revealed. In many designs, sharp corners are desired, and thus a *corner compensation* can be added to the mask pattern, Fig. 2.11. As the etching proceeds, this additional structure is etched and a rectangular corner is achieved. The size of the mask pattern often limits the space available for the compensation, that cannot therefore be made perfect.

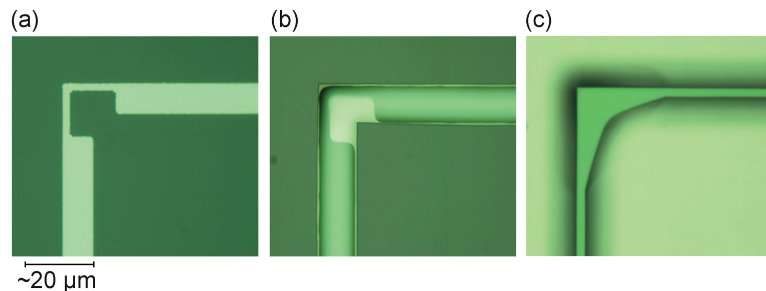


Figure 2.11. Optical microscope images of convex corner etching on <100> Si (mag 50×). (a) Patterned hard mask with a corner compensation; (b) Successful timing leads to a rectangular corner after silicon etching; (c) Further etching results as undercutting revealing fast etching crystal planes.

Photoresist itself is not durable enough as a masking material in silicon wet etching, but it can be used for patterning a *hard mask* such as Si_3N_4 or SiO_2 thin-film. As discussed above, also the dopant induced etch stop is a commonly exploited technique. In recent years, the supply of spincoatable polymers that have been developed to be used directly as a mask or a protective layer, has opened up new alternatives in wet processing. One example is commercially marketed as ProTEK (Brewer Science Inc.), a coating material resistant towards both bases and acids. It is capable for protecting topographies with steps of several microns in through wafer alkaline wet etching, which was utilized in Publication V.

TMAH was applied as a silicon wet etchant in all the processes developed within this thesis. The typical parameters and etching conditions are listed in Table 2.1. The most critical parameters to be controlled are tem-

Table 2.1. Typical TMAH etching conditions.

Concentration [wt-%]	25
Temperature °C	85
Etch rate, (100) [μm/min]	0.6
Etch rate, (110) [μm/min]	1.4
Selectivity, SiO_2:Si	> 3000:1
Selectivity, (100):(111)	30:1
Selectivity, Ga^+ doping (>10^{16} cm^{-2})	2000:1

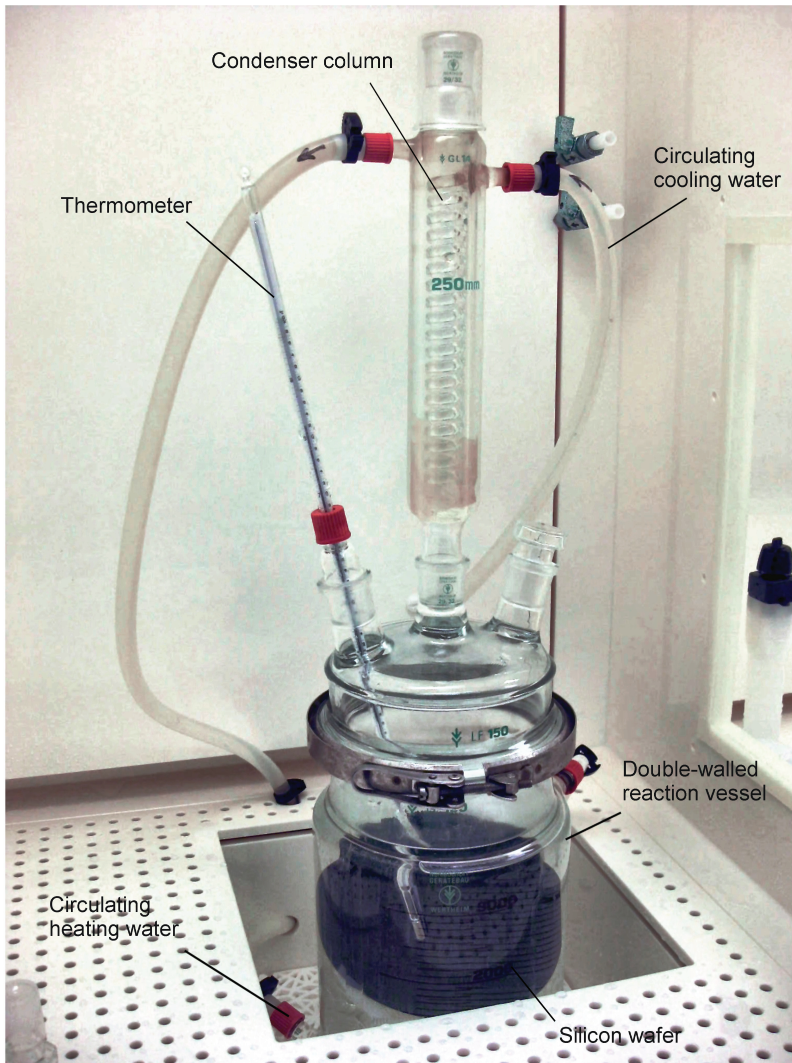


Figure 2.12. TMAH wet etching setup used in the experiments.

perature and TMAH concentration. The typical etching takes place close to 80-90 °C, because the elevated temperature has a direct impact on the reaction rate. Also the decrease of TMAH concentration increases the etch rate, because the amount of water molecules is higher [73]. The maximum is reached close to 4 wt-% [74]. However, this type of speeding up is often not advisable, mainly due to the effects on the surface quality and crystal plane selectivity [75]. In long etching processes, the evaporation of water and the resulting concentration of the solution need to be controlled. In critical applications, fresh solutions are required because the dissolved silicon decreases the concentration of active OH^- ions. A photograph of the etching setup used in the experiments is seen in Fig. 2.12.

The TMAH etching results in smooth silicon surfaces when solutions containing over 22 wt-% are used. At concentrations close to 15 wt-%, (111) planes start to form pyramid-like *hillocks*, as the (110) planes etch slower than (100) planes [76]. Some applications take an advantage of this type of pyramidal texturization, *e.g.* in solar cells the light trapping capability can be improved [77, 78]. In recent years there has been a lot of activity in studying the influence of additive surfactants, such as isopropanol (IPA) and Triton-X, in TMAH solution [79–81]. As a result, the crystal plane selectivity can be manipulated, and extremely smooth surfaces can be achieved [82, 83].

Dry etching

Dry etching means the removing of material typically with help of *reactive ion etching* (RIE); based on the action of both chemically active radicals and physical ion bombardment. The etching gases are brought into a vacuum chamber, and ionized by an RF-field to form plasma that reacts with the sample surface. Depending on the feed gases, several types of materials (*e.g.* Si, SiO_2, Si_3N_4) can be etched with the same equipment. The typical etch rates are in the order of tens or hundreds of nm/min. In many cases the etching time is relatively short, and photoresist is sufficient as a masking material.

In silicon processing, dry etching provides certain benefits compared with wet etching; the most important being the capability of high anisotropy that is independent on the crystal directions but produces practically vertical sidewall profiles. Silicon dry etching is typically performed by fluorine based chemistry [84].

Deep reactive ion etching (DRIE) is an extension to the basic mechanism of RIE. It enables fast (several μm/min) etching of structures with very deep and narrow profiles [85]. In the experiments of this work, cryogenic DRIE was used for silicon dry etching. The temperature in the etching chamber is decreased to less than - 100 °C, and the etching is performed in SF_6/O_2 plasma. The gases form a SiO_xF_y passivation layer on silicon that is sputtered away from horizontal surfaces by directional ion bombardment [86]. The resulting sidewall profile can be tuned by changing the SF_6 and O_2 mixture, the lack of O_2 leading to isotropic etching. SiO_2, and especially Al_2O_3 and Al are thin-film materials durable enough to be used as hard masks in silicon DRIE.

3. Fabricated sensors and structures

The main results of this thesis are presented in this chapter. The emphasis is on the fabrication process development of the realized mechanical devices. Attention is also paid to the application-specific features affecting behind the design of each structure.

3.1 Mechanical silicon oscillators

The topic of Publication I is related to the necessity of functional, protective, or optical coatings on sensitive MEMS devices. The coatings may be used, for example, as active layers, with classical examples being mass or gas sensors, or for preventing chemical and mechanical wear or failure inducing phenomena such as stiction [87, 88]. In optical devices, sequential growth of different materials enables multilayer high- and anti-reflection stacks [89].

The particular approach of the study was to report the effect of double sided ALD alumina coating on the dynamical, thermo-mechanical and optical properties of a mechanical silicon oscillator, Fig. 3.1. The design of the coated non-tilting out-of-plane vibrational mode oscillators with a high quality factor ($Q = 100\ 000$ at $p < 10^{-2}$ mbar) for mechanical resonance has been presented in Ref. [90]. The structures are proposed to be used in high precision sensing applications, short range detection of weak forces and in interferometric systems as moving mirrors with a capability to detect femtometer-level displacements [91].

The components were fabricated from double-side polished 380 μm thick <100> oriented silicon, Fig. 3.2. A bulk silicon wafer was thermally oxidized with a 95 nm thick SiO_2 film. The oscillator structure was aligned and patterned on both sides of the wafer, and etched in 85 °C TMAH, using oxide as a hard mask. The resulting structures have a well-defined

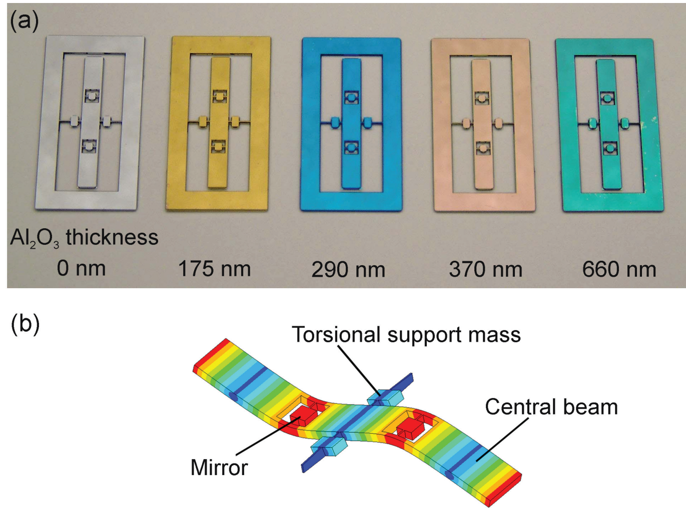


Figure 3.1. (a) ALD alumina coated mechanical silicon oscillators. The dimensions of the central beam, being mainly responsible for the resonance frequency of the whole structure, are 1.5 mm $\times$ 14 mm $\times$ 380 μm (Picture courtesy of Ossi Hahtela.) (b) FEM-simulated mode pattern of a vibrating oscillator (outer frame not shown). The aim of the design is to keep the non-tilting mirror vanes parallel to the original component plane during all the phases of vibration [92].

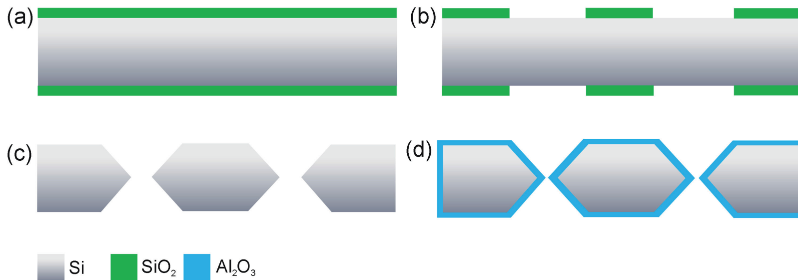


Figure 3.2. Fabrication process of alumina coated silicon oscillators. (a) thermal oxidation; (b) double-sided pattern alignment and hard mask oxide etching; (c) anisotropic silicon etching and oxide removal; (d) ALD coating.

symmetry and high surface quality, which are essential for balanced operation and minimized energy dissipation. The dimensions were optimized by using finite element modelling (FEM) [90]. In ALD alumina coating, trimethyl aluminum TMA ($Al(CH_3)_3$) and water were used as precursors. The films were deposited at 220 °C, 2.3 mbar, and the thicknesses, measured by ellipsometry, varied from 5 to 662 nm.

As a result of the coating, the resonance frequency of the oscillators was found to slightly increase because the added films effectively stiffening the structures. Film thicknesses up to 100 nm were deposited without any significant influence on the intrinsic high mechanical quality. It was also shown that the sensitivity of the resonance frequency to ambient temperature decreased when the film thickness was increased. For the thickest Al_2O_3-coating (660 nm), the temperature-induced drift in the resonance frequency was measured to be 31 % less than that of an uncoated oscillator.

Besides the mechanical behaviour, a deposited alumina film was demonstrated to act as an optical anti-reflection coating whenever the thickness is a multiple of a quarter of the reflecting wavelength. The reduction of the reflectivity from $R_{Si} = 0.35$ to $R_{AR} = 0.035$ was obtained because the refractive index of alumina ($n_{Al_2O_3} = 1.64$ at 633 nm) is lower than that of the silicon substrate ($n_{Si} = 3.92$).

3.2 Acousto-optical SOI cantilevers

Publication II and Publication IV discuss the design, fabrication and characterization of acousto-optical cantilever microphones. The components are primarily developed to be used in photoacoustic spectroscopy (PAS), having applications in various fields of research and industry. These include *e.g.* sample analysis in biology, medicine, and industrial process control, as well as ambient air, pollutant, and toxic gas monitoring [93–95]. The cantilever pressure sensors reported in this thesis have been developed to optimize the sensitivity of the measurement, which is a multifaceted challenge related not only to the acoustic sensor, but to the characteristics of the whole surrounding photoacoustic system.

3.2.1 Photoacoustic application and cantilever design

To understand the requirements set for the microphone properties and design, the fundamentals of photoacoustic detection are briefly described. The principle of cantilever-enhanced PAS measurement is shown in Fig. 3.3. Infrared (IR) light is guided through a window to a sample sealed in a closed chamber and absorbed at wavelengths characteristic to it. The excitation and non-radiative relaxation of gas molecules increase the gas temperature and pressure. The periodic modulation of the incoming light

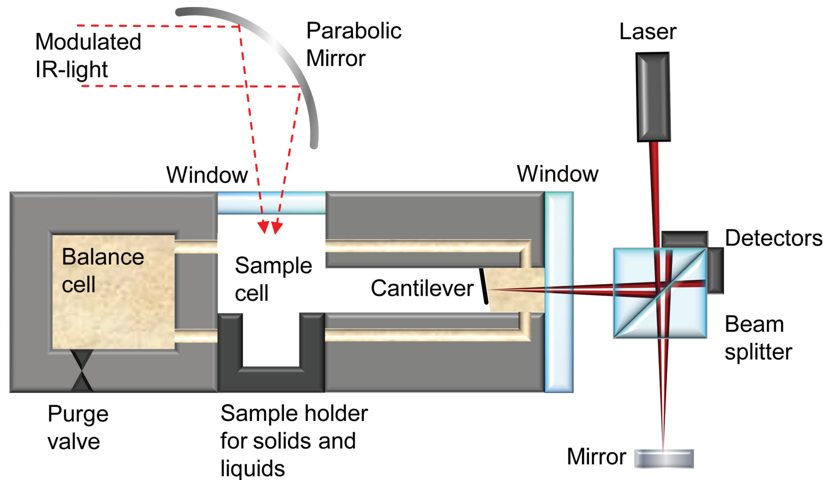


Figure 3.3. Principle of photoacoustic detection [Publication IV]. Gaseous samples act themselves as a medium that couples the acoustic signal to the cantilever microphone, whereas with solids and liquids the heat is transferred from the sample to a coupling gas. The gas can be changed via the valves connected to the balance cell, from where it is guided to the sample cell through the gap around the cantilever. The centers of masses of both balance and sample cells are located on the same side of the cantilever to extinguish the acceleration noise caused by the movement of the setup.

generates an acoustic wave with an amplitude proportional to the concentration of the absorbing gas, which in turn is detected with a microphone.

The sensitivity of the photoacoustic method is strongly dependent on the acoustic sensor. The limitations of conventional membrane type microphones are related to the capacitive measurement principle and the nonlinear pressure response. Major improvements are thus achieved by using a silicon cantilever microphone with a non-contact interferometric readout as visualized in Fig. 3.3. The reason is that under pressure variations the cantilever only bends with a wide dynamical range but does not stretch, and the optical measurement technique does not induce damping. This allows the measurement of pressure variations that are a hundred times lower than those detected by condenser microphones, Fig. 3.4 [96–98].

Because the cantilever has a major role in the total photoacoustic system signal response, a flexible crystalline silicon based design with dimensions aiming to minimize the spring constant is selected, Fig. 3.5. The cantilever can be considered as a harmonic oscillator with a spring constant k_0. In addition, its bending induces a change on the photoacoustic sample cell volume acting as a "gas spring" with a constant k_{gas}. Thus

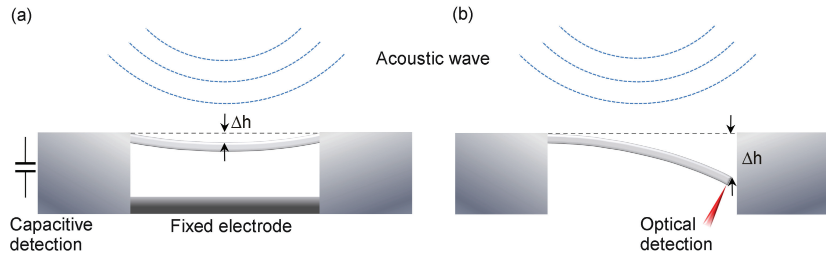


Figure 3.4. Comparison of a conventional condenser microphone (a) and a cantilever microphone (b). The movement of the cantilever's free end can be even two orders of magnitude greater than the movement of the middle point of a deformed membrane under the same pressure variation.

the total effective spring constant can be described as [99]:

$$k = k_0 + k_{gas} = \frac{2}{3}Ew\left(\frac{d}{l}\right)^3 + \gamma\frac{A_C^2 p}{2.5V_{eff}}. \tag{3.1}$$

In the equation above, E is the Young's modulus of silicon (169 GPa), w, d, l and A_c are the width, the thickness, the length and the area of the cantilever, respectively, p is the pressure inside the sample cell, V_{eff} the effective cell volume ($\sim$ 0.1 cm^3), and γ the ratio of the specific heat capacities of the gas inside the cell (1.4 for air).

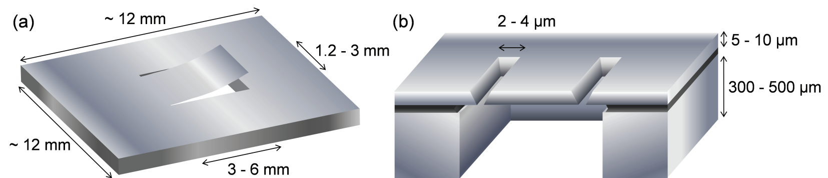


Figure 3.5. The design and typical dimensions of an acoustic cantilever sensor.

Besides the cantilever, there are also other factors affecting the signal in the photoacoustic cell as visualized in Fig. 3.6. The gas leakage through the air gap surrounding the cantilever acts as a high pass filter attenuating the signal at low frequencies. Thus the gap area should be as small as possible. On the other hand, the limited rate of heat transfer and the non-radiative relaxation of excited molecules show a low pass filter type behavior. As a result of the total system response, the operation range is typically below the fundamental resonance frequency of the cantilever.

The sensitivity of the PAS detection is limited by noise. Thus the optimization of the cantilever aims to maximize not only the signal response

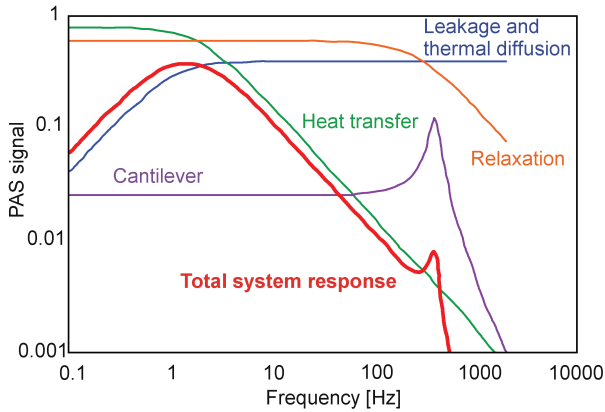


Figure 3.6. Components affecting the photoacoustic system response. The illustration is reproduced after [100].

but the signal-to-noise ratio (SNR) of the measurement. The noise components affecting the detection characteristics of the system include acceleration, acoustic, and electrical noise as well as Brownian noise that becomes the dominant factor of the noise spectrum when external sources are suppressed. It is originating from thermal fluctuations inducing collisions of gas molecules with the cantilever. The noise behaviour is frequency dependent, and affected by the dimensions of the cantilever and the surrounding air gap [99, 101].

3.2.2 Fabrication

In order to realize cantilever microphones, a few alternative fabrication processes were implemented, Fig. 3.7. All variations were based on double-sided etching of <100> oriented silicon patterned by optical lithography.

The first one (Fig. 3.7 (a)) was a simple bulk process based on timed TMAH wet etching (25 % solution, 85 °C). A double-side-polished wafer was thermally oxidized (step 1), and the (111)-plane-limited trenches that determine the cantilever thickness were etched (step 2). The oxide layers were removed in BHF, and the wafer was re-oxidized to protect the top surface and to release the cantilevers from the other side (step 3). The challenges with the process are related to the control of the etching time, thickness variations over the wafer, non-idealities of TMAH etching, and worst of all, the stress caused by the oxide protecting the top surface that can tear the structure open during the release. As a result, the reproducibility was poor and the achievable width of the gap surrounding the

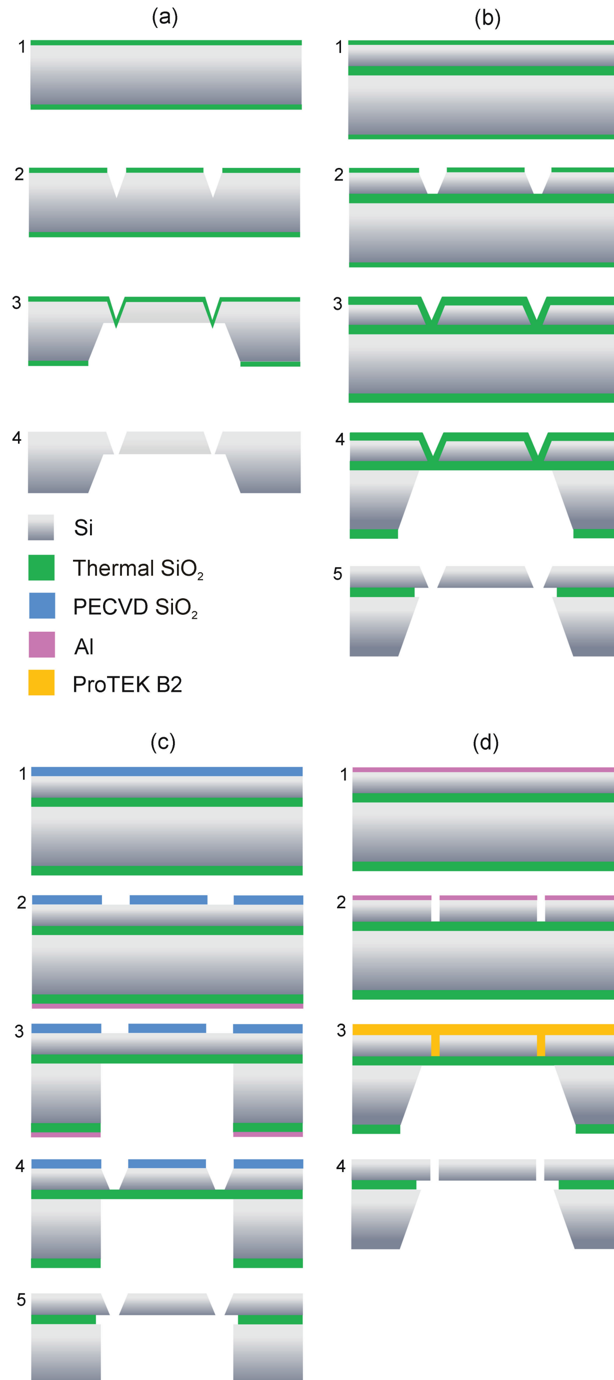


Figure 3.7. Fabrication processes for cantilever pressure sensors. (a) Bulk silicon -based process; (b) SOI process based on using thermal oxide as a wet etching mask; (c) Process based on low-temperature PECVD oxide and DRIE; (d) Process based on using a metal mask and wet etching with polymer coating protection.

cantilever is in the order of tens of microns.

Remarkable improvements were achieved when the SOI-based process (Fig. 3.7 (b)) was implemented. Again, TMAH was used for etching, but now the thickness of the cantilever is determined by the thickness of the device layer (10 μm), and the role of timing diminishes as the buried oxide (1 μm) acts as an etch stop. The gap width around the cantilever from 2 to 4 μm became achievable. In the etching of the device layer, a 95 nm thick thermal oxide film serves as a hard mask (step 2), whereas the thickness of the layer in the second oxidation must be selected to match the thickness of BOX (step 3). Thus, the effect of shear stress exerted on the cantilever after the etching through the handle wafer becomes highly compensated (step 4), and the final release can be done in a controlled manner by removing the buried oxide as well as the mask and the protective oxides (step 5). The resulting cantilevers are slightly curved as a consequence of stress originating from the modification of silicon surface during the thermal oxidation.

Severe problems arose when the process was repeated in order to produce thinner and more sensitive cantilevers using a wafer with a 5 μm thick device layer. The extensive bow of the components prevented the interferometric displacement measurement in acoustic wave sensing. As a solution, the process was further developed, Fig. 3.7 (c). SOI wafers with a 600 nm thick buried oxide originally grown on the handle wafer were used. Thermal oxidation was replaced by depositing a PECVD SiO_2 film on the device layer (step 1). The process was carried out in two steps, the final thickness being equal to the thickness of the BOX. After each step the film was densified by annealing. A non-densified film suffers from pinholes, its performance as an etch mask is poor, and the stress experienced by the top surface of the device layer is not compensated by the stress that is induced by the BOX on the other side. The annealed PECVD film was characterized by ellipsometry, and the etch durability was tested in reactive ion etching (RIE), tetramethylammonium hydroxide (TMAH), and buffered hydrofluoric acid (BHF). The properties were found out to be close to those of thermal oxide (Table 3.1).

The process continues by patterning the deposited PECVD hard mask with RIE to define the cantilever structures (step 2). On the handle side, cavity patterns are aligned and etched with DRIE using an aluminum film as a mask (step 3). As in the previous process, the cantilevers on the device layer are etched in TMAH (step 4), and released by removing the

Table 3.1. Properties of PECVD SiO_2 annealed at 1 000 °C, 30 min, atm.

Deposition rate [nm/min]	65
Densification [% of thickness]	5
Etch rate in RIE[1] [nm/min]	20
Etch rate in BHF[2], 32 °C [nm/min]	100
Etch rate in 25 m-% TMAH 86 °C [nm/h]	10
Refractive index	1.46

[1] P = 200 W, p = 30 mTorr, CHF_3 = 25 sccm, Ar = 25 sccm

[2] Honeywell Ammonium fluoride etching mixture AF 90-10

oxides (step 5). The radii of curvature of the resulting cantilevers were measured to be several meters, which is sufficient for acoustic sensing with an interferometric readout. The corresponding residual stress decreased by a decade compared with the double times thicker components fabricated with thermal oxide masks.

Thermal oxidation as a source of residual stress was verified by the process presented in Fig. 3.7 (d). All high temperature steps were avoided, as now a sputtered Al film (step 1) was used as a hard mask for etching the gaps surrounding the cantilevers in DRIE (step 2). The etching from the handle side was performed in TMAH with the device side being protected with an alkaline resistant polymer coating (Brewer Science ProTEK® B2) (step 3), and the final release in BHF and acetone (step 4). The stress and curving of the final cantilevers were determined to be comparable to the components fabricated with the PECVD oxide based process.

The conclusion is that the use of SOI substrates is crucial in successful fabrication of acoustic cantilevers. The process based on anisotropic wet etching and the use of thermal oxide as hard mask material is suitable for the reproducible production of approximately 10 μm thick components seen in the photograph of Fig. 3.8. The advantage is the convenience in mass production as a large batch of wafers can be processed simultaneously. Thinner cantilevers can also be fabricated, but a special attention must be paid to the selection of material properties and processing methods to control residual stresses.

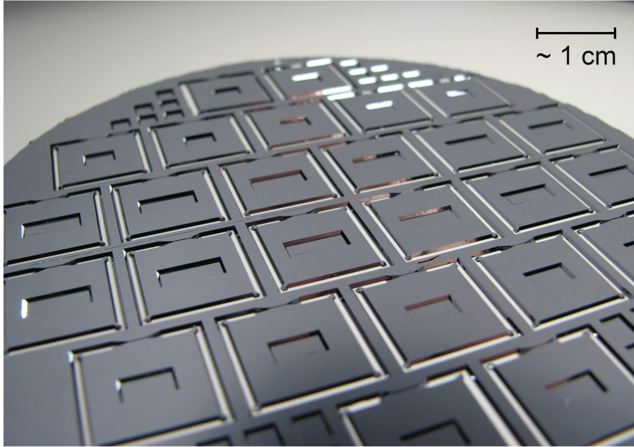


Figure 3.8. Final cantilevers on an SOI wafer seen from the handle side. The chip edges are determined as a part of the mask pattern to avoid dicing of the wafer with fragile cantilevers as a back-end process.

3.2.3 Functionality

There are several studies in which the cantilever microphones developed in this work are applied in photoacoustic trace gas analysis with detection limits in the sub-ppb level [102]. The use of several types of light sources such as black body radiators combined with mechanical choppers, electrically modulated broadband IR-sources and diode lasers has been demonstrated in measuring sample gases such as CO_2, CO, CH_4, H_20, and O_2 [100, 103–105].

The cantilever-enhanced photoacoustic detection can also be combined with Fourier transform infrared (FT-IR) spectroscopy to analyze gaseous, liquid and solid samples. Over five times higher SNR has been achieved compared with a commercial FT-IR PAS detector (MTEC model 300), as the value increased from 679 to 3480 in a standard carbon black test sample measurement [106].

Publication IV reports the improvements obtained in the detection sensitivity, when 10 μm thick cantilevers fabricated by the process in Fig. 3.7 (b) are replaced by 5 μm components resulting from the process in Fig. 3.7 (c). As a result of the thinning, the cantilever part k_0 remains only a few percent of the total spring constant (Eq. 3.1) of the system. Thus the dimensions of the sensor can be considered to be close to the optimum from the sensitivity point of view.

Examples of measured noise spectra and FT-IR PAS spectra for a broad-

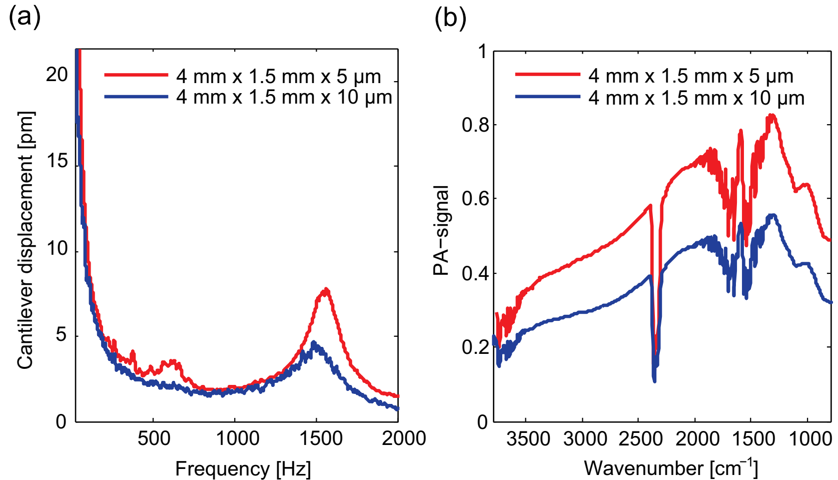


Figure 3.9. (a) Noise spectrum of an acoustic cantilever sensor dominated by Brownian motion of gas molecules. The fundamental resonance frequency peak is seen near 1500 Hz. (b) FTIR-PAS spectra of a solid carbon black test sample measured using helium as a coupling gas. The presented wavenumber range corresponds to a photoacoustic signal band from 125 Hz to 600 Hz.

band absorbing carbon black test sample are presented in Fig. 3.9. Meanwhile the noise measured with the thinner cantilever increases approximately 20 %, the increase of the signal is approximately 50 % on the corresponding frequency band. This indicates an improvement of 25 % in the SNR. In addition, polyethene (PE) was measured as an example of a true solid sample, verifying the increase of the signal and the SNR.

There are also a few other noteworthy PAS approaches that compete with the cantilever enhanced detection in order to reach ultrahigh sensitivity. These techniques take either the advantage of photoacoustic cell resonances and high power laser sources, or are based on utilizing resonating quartz tuning forks as acoustic sensors. The different methods are often compared with the help of noise equivalent absorption coefficient normalized with the light source power and measurement time (NNEA). The sensitivity obtained with cantilever detection ($1.7 \cdot 10^{-10}$ cm^{-1} W/$\sqrt{Hz}$) is approximately an order of magnitude better than the sensitivities measured with quartz enhanced ($3.3 \cdot 10^{-9}$ cm^{-1} W/$\sqrt{Hz}$) and resonant ($1.5 \cdot 10^{-9}$ cm^{-1} W/$\sqrt{Hz}$) PAS techniques [107–109].

3.3 Dopant-induced stress in mechanical silicon structures

The challenges with photoacoustic cantilever fabrication evoked an interest to study residual stresses in released silicon structures on a more general level. The results are reported in Publication V. As explained above, the type of the silicon oxide thin-film used during the processing had been noticed to have a connection to the mechanical deformation of the structures. This initiated a hypothesis about the origin of the stress being related to the segregation and the consequent redistribution of dopant atoms in silicon. The topic of stress in surface micromachined structures fabricated by boron etch stop, and dopant effects in polysilicon layers have been discussed in a few published reports [110–114]. Instead, the focus of this study was on crystalline silicon, especially on SOI-based devices, and the physics behind the stress generated by dopants reordering as a consequence of thermal oxidation.

3.3.1 Experiments

To study the residual stress, released cantilevers were fabricated as test structures, and their curvature was determined, Fig. 3.10. A series of ten SOI substrates with varying level of doping (from 10^{15} to $5{\cdot}10^{19}$ atoms cm^{-3}) was investigated. The emphasis was on the effects caused by boron and phosphorus, since they are the two most commonly used dopants. For comparison, also a sample highly doped with antimony was studied.

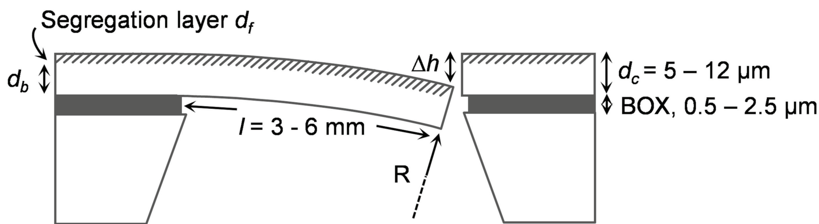


Figure 3.10. Cross-section of a cantilever test structure. The sample series included SOI substrates with varying parameters (dopant type and concentration, device layer and BOX thicknesses, original BOX growth boundary). Cantilevers with different lengths were fabricated, the width being 1.5 mm in all cases. The deflection Δh, used for determining the curvature, was measured using optical microscopy.

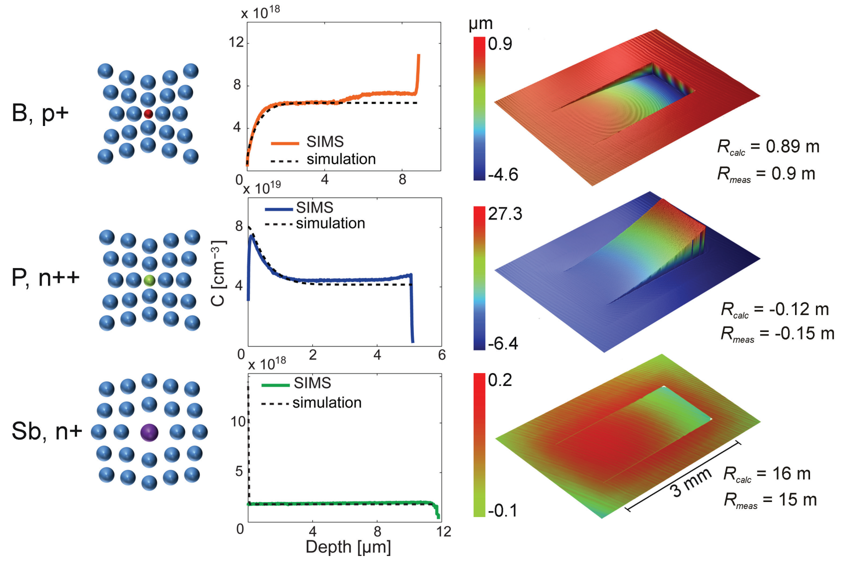


Figure 3.11. Cantilevers curving as a result of residual stress induced by uneven distribution of dopants. Boron and phosphorus contract the silicon lattice, while antimony expands. The bending profiles have been determined by optical profilometry. The simulated dopant profiles show an excellent match with those measured by SIMS, and the same applies when the measured radii of curvature R_{meas} are compared with the calculated values R_{calc}.

In the fabrication of samples, a process similar to the one presented in Fig. 3.7 (b) was used. High temperature processing steps, that have a tendency of inducing segregation of dopants in silicon, are present both in the SOI substrate fabrication and in the actual sample fabrication process. In order to inspect the redistribution profile, the dopant concentration throughout the SOI device layer was investigated by secondary ion mass spectrometry (SIMS) measurements.

The core results of the experiments, Fig. 3.11, show a clear connection between the dopant distribution and residual stress, detected as curving of the cantilevers. Boron, that induces mechanical contraction when it replaces a silicon atom in the crystal lattice, has escaped from the cantilever top surface. As a consequence, the structure bends under compressive stress. Phosphorus also contracts the lattice, but it gathers close to the top and induces a tensile effect. Antimony is a large sized atom that expands the lattice, but it shows strong accumulation only very near to the surface, and has hardly any effect on the cantilever deflection.

3.3.2 Theoretical analysis

Besides the experimental studies, the physics behind the bending of the cantilevers was also inspected theoretically. ATHENA process simulation software (Silvaco, Inc.) was used for predicting the dopant segregation, and the results were compared with the SIMS concentration profiles, Fig. 3.11 [115].

The simulation accuracy depends strongly on the selected diffusion model and the applied parameters. The "“fully-coupled”" model that couples defect levels to dopant concentration and diffusion behaviour, was used. The dopant type and concentration, gas flow parameters (for H_2 and O_2), oxidation ambient (steam), and time, including up and down ramping of temperature, as well as etching processes were applied based on those used in the experiments. In addition, high concentration extension that includes extra recombination reactions was used. The number of simulation grid points in thermal oxidation was increased in order to improve the accuracy (grid spacing 0.01 μm), and boron segregation and diffusion parameters in oxidation were adjusted as explained in [116]. The silicon interstitial injection rate parameter was set separately for phosphorus and boron according to the SIMS results so that a good fit was found throughout the sample series. This is important in order to avoid the overestimation of oxidation enhanced diffusion that results when the default values are used. The parameters applied in the simulations are listed in Table 3.2. Fig. 3.12 shows an example of an output for boron segregation resulting from thermal wet oxidation.

The simulated dopant profiles were used for calculating theoretical values for cantilever curvature and stress. The structure was considered to be bending as a two-layer beam composing of a segregation layer d_f and the rest of the beam d_b. The misfit strain $\Delta\epsilon$ is caused by the volume difference of the film material and the beam. This generates a force that can be connected to the curvature κ by taking into account the moment it induces and the beam stiffness. A detailed derivation is presented in [117], and as a result the following expression is obtained:

$$\kappa = \frac{6E_f E_b (d_f + d_b) d_f d_b \Delta\epsilon}{E_f^2 d_f^4 + 4E_f E_b d_f^3 d_b + 6E_f E_b d_f^2 d_b^2 + 4E_f E_b d_f d_b^3 + E_b^2 d_b^4} \tag{3.2}$$

The equation above makes no approximation of the segregated film being much thinner than the substrate. When $d_f << d_b$, the expression reduces

Table 3.2. Parameters used in ATHENA simulation for growing a 1 μm thick thermal oxide film.

Method	*high.conc full.cpl*
Grid	*grid.oxide=0.01 gridinit.ox=0.01*
Interstitial injection rate, P	*interstitial silicon / oxide theta.0=8e7*
Interstitial injection rate, B	*interstitial silicon / oxide theta.0=2.5e8*
Boron diffusivity	*impurity i.boron oxide*
	DIX.0=1 DIX.E=3.53
Temperature ramping, up	*diffuse time=66 temp=600*
	t.final=1000 nitro press=1.0
Oxidation	*diffuse time=330 temperature=1000*
Ambient	*weto2 press=1.0*
Gas flows	*f.H2=10.0 f.O2=7.0*
Temperature ramping, down	*diffuse time=85 temp=1000*
	t.final=650 nitro press=1.0

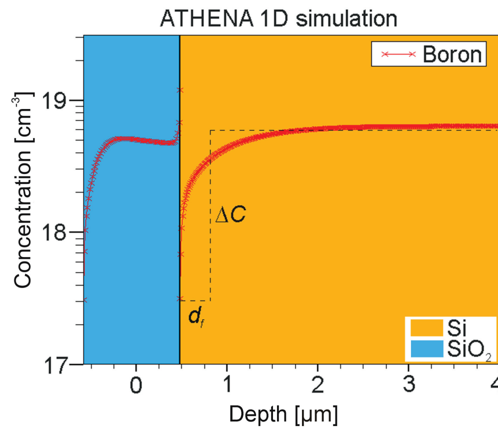


Figure 3.12. Boron distribution at Si/SiO_2 interface, resulting from ATHENA process simulation. The dashed line shows an approximation of a silicon structure consisting of two distinct layers with uniform dopant concentrations.

to Stoney's formula (Eq. 2.1). In the present case, the misfit strain is expressed by taking into account the lattice expansion coefficient β inherent to the dopant atom in question, and the change of dopant concentration ΔC obtained from the simulated distribution, $\Delta\epsilon = \beta\Delta C$. The value for film thickness d_f is searched by integrating the simulated concentration profile and finding a value that corresponds to a film that is uniformly doped with the surface concentration, see Fig. 3.12. The rest of the beam

d_b is approximated to be uniformly doped with the original concentration.

The match of experimentally determined and theoretically calculated values for cantilever curvature verify the segregation of dopants to be the main origin of the residual stress in the investigated structures. However, the theoretical approach based on a simplified two-layer model includes certain approximations that should be noticed. The curvature is assumed to be spherical and linearly coupled to stress. In addition, the change of Young's modulus E as a result of doping has shown to be negligible, and it is thus ignored (*i.e.* $E_f = E_b$ in Eq. 3.2) [26]. When the deformation of the structure is large, nonlinearities induced by material compression and stretching should be taken into account, and bending cannot anymore be expressed with a single radius [53]. On the other hand, the other possible sources of stress, inaccuracy of the measurements, and wafer-level unidealities bring their own uncertainties. Despite of the approximations, the accuracy of the presented model can be concluded to be adequate for estimating the order of magnitude of mechanical deformations in various silicon based MEMS devices.

3.3.3 Stress control

There are many feasible approaches for controlling the dopant-induced stress. If the application allows the use of lightly doped substrate material, the segregation-related effects remain negligible. Otherwise, a special care must be taken in selecting the processing methods so that high-temperature processing steps such as thermal oxidation are avoided. It was demonstrated that the use of PECVD SiO_2 or Al thin-films as a hard mask (processes presented in Figs. 3.7 (c) and (d)) was an effective solution for minimizing the stress, even when very highly doped silicon was used as a material, Fig. 3.13.

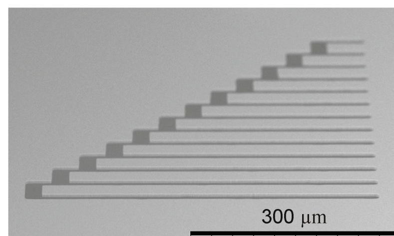


Figure 3.13. Highly phosphorus-doped, 5 μm thick SOI cantilevers fabricated without any high temperature processing steps show no residual stress. The structure is etched with DRIE using Al as a mask.

3.4 Nanoscale silicon structures

Dopant induced effects are also in the focus of the study presented in Publication III, but from a very different point of view. Now a gallium layer was implanted by focused ion beam locally on a silicon substrate and characterized as a mask in TMAH wet etching. The principle of the method is shown in Fig. 3.14. The dimensions of the final structures are accurately defined, and neither resists nor lithography masks are needed. The aim is to utilize the developed process in high precision 3D nanostructure fabrication, which was demonstrated by generating nanoscale gratings, channels and freestanding structures. The method is fast compared with direct milling, as the maximum ion current of 21 nA modifies an area of $600 \times 600\ \mu m^2$ into an etch resistant state in less than a minute.

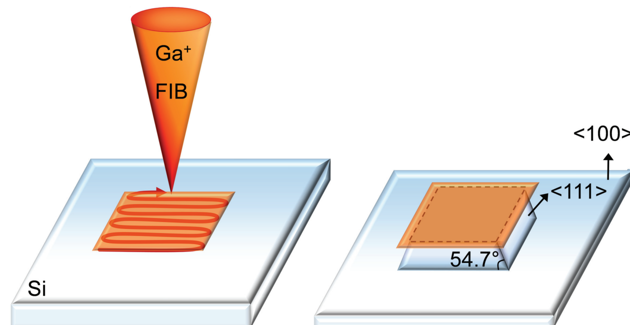


Figure 3.14. Direct writing FIB implantation and the subsequent anisotropic wet etching. The doped areas act as a mask against the etchant.

3.4.1 FIB-TMAH process

The minimum achievable linewidth of the method is limited by the shape of the ion beam, applied dose, and the distribution of implanted Ga^+-ions in silicon, Fig. 3.15. The vertical distribution determines the thickness of the masking layer that is approximately 50 nm at 30 keV ion energy.

The etch stop properties of FIB-implanted Ga on both <100> and <110> oriented silicon were investigated by implanting a series of samples with variable ion doses (from 2×10^{13} ions/cm^2 to 4×10^{16} ions/cm^2) and by etching them in TMAH until the doped layer is totally etched away, Fig. 3.16 (a). The higher the ion dose used for implantation, the deeper is the achievable etching depth around the patterns before the mask breakdown. The heights of the etched profiles were measured using a profilome-

ter, Fig. 3.16 (b). The threshold for the drastic etch rate lowering can be seen between 10^{15} ions/cm^2 and 10^{16} ions/cm^2. The results indicate a selectivity between the treated and untreated silicon being better than 2000:1 with the highest ion doses, which is comparable to the selectivities of the conventional SiO_2 and Si_3N_4 masks. The Ga^+-doped masking layer is amorphous, as the critical ion dose is approximately 10^{14} ions/cm^2.

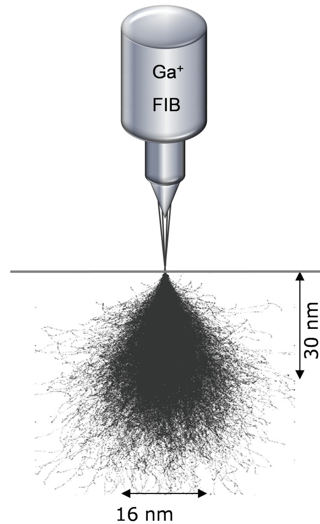


Figure 3.15. Distribution of gallium ions in silicon with the ion energy of 30 keV. The schematic is obtained by SRIM simulation software [118].

3.4.2 Fabricated structures

To investigate the limits of the process, various types of nanostructures were patterned with FIB and etched in 85 °C, 25 % TMAH solution. In order to obtain the maximum patterning resolution, the finest beam (1.5 pA) with a target FWHM of 10 nm was used, and the ion dose was optimized for each structure by varying the exposure time.

Grating structures were patterned on a <100> silicon substrate both with varying and constant periods, Figs. 3.17 (a) and (b). The smallest reproducible line was 40 nm, and smallest trench 60 nm (dose 10^{15} ions/cm^2).

Figs. 3.17 (c) and (d) show freestanding elements that are made of the Ga^+-doped masking layer (dose 4×10^{15} ions/cm^2). Again, <100> oriented substrate was used but now the release is obtained by aligning the patterns 45° off the substrate main axes (see Fig. 2.10 (a)). The narrowest features are only 25 nm wide. The released structures in Fig. 3.17 (e) demonstrate the capability of FIB direct-writing implantation in produc-

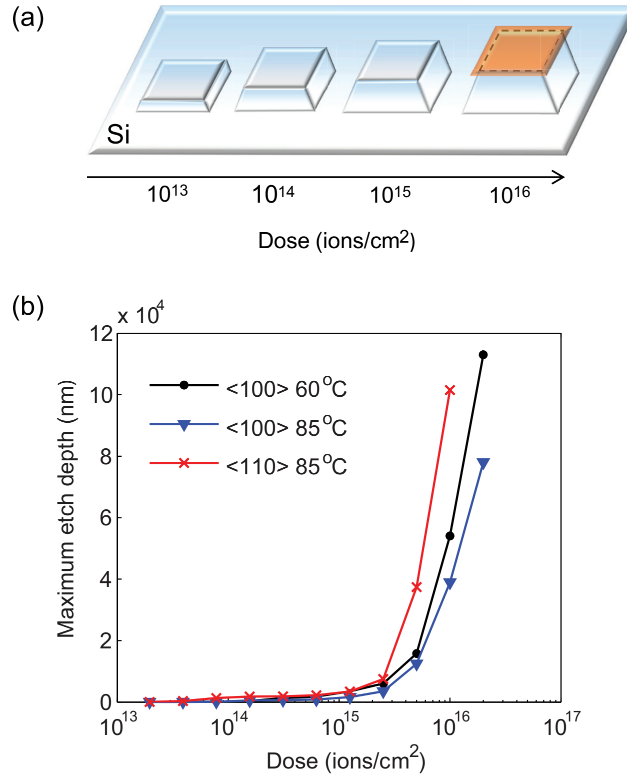


Figure 3.16. (a) Schematic drawing illustrating the mask selectivity experiment. (b) The masking capability of implanted Ga^+ mask in 25 % TMAH solution.

ing arbitrary, curved shapes.

Nanochannels with vertical sidewalls, Fig. 3.17 (f), were fabricated by utilizing a <110> -oriented substrate (dose 10^{15} ions/cm^2). With this approach, the TMAH etching anisotropy and high selectivity to the gallium implanted mask can be utilized in the fabrication of structures with high aspect ratios. Fig. 3.17 (g) shows a FIB-milled cross-cut of an ultra-thin single wall with an aspect ratio of more than 1:30.

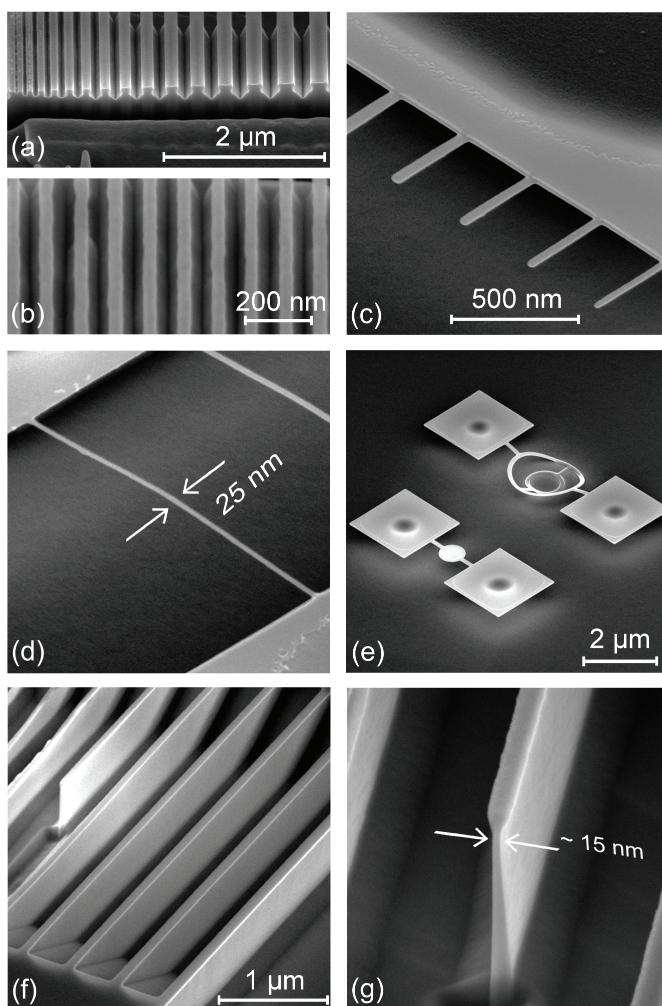


Figure 3.17. FIB - TMAH processed nanostructures [Publication III]. (a) FIB milled cross-cut of a varying period grating; (b) Grating with a constant 100 nm period; (c) Released beams; (d) A released bridge; (e) Circular, "MEMS-alike" test structures; (f) Nanochannels with vertical walls on <110> silicon; (g) A cross-cut of a single wall, height 570 nm. The Ga-doped masking layer can clearly be seen on the top.

4. Conclusions

In this thesis, microfabrication processes for mechanical single-crystal silicon devices were developed. As a result of the study, extremely accurate sensor structures were realized. These include SOI-cantilever microphones applied in photoacoustic spectroscopy with ultimate detection sensitivity in the sub-ppb level in gas analysis, and high-Q oscillators which are capable of approaching a surface with a single, non-tilting plane. The functional properties of the sensors, such as resonant behaviour, temperature sensitivity and optical reflectivity, were manipulated and fine-tuned by using conformal atomic layer deposited aluminum oxide coatings. In addition, a process combining traditional, anisotropic TMAH wet etching and state-of-the-art focused ion beam implantation techniques was developed in order to produce 3D nanoscale devices for emerging NEMS applications.

The acoustic sensors developed in this work are used in photoacoustic material analyzing equipment commercialized by Gasera Ltd. Process design rules were created starting from the materials selection and ending up to an optimized outcome as far as the stress control is concerned. In the fabricated components, the micron scale thickness and the square millimeter scale area are tailored for maximizing the signal-to-noise ratio in the applied photoacoustic cell. In the further development of the sensor, the mechanical fragility that limits the usability in practical photoacoustic spectroscopy measurements, and the expected yield of undamaged components per wafer are aspects that need to be carefully considered. A prospective way to proceed in the future is to pursue towards the miniaturization of the whole photoacoustic measurement scheme by integrating the cantilever on the same chip with the optics used for the displacement detection.

The fabrication of nanoscale devices in the research and development phase requires rapid prototyping methods that can be applied in combination with well-known clean room processing techniques. The prospective applications of the presented FIB based method include nanomechanical devices such as cantilever and nanowire sensors, nanofluidistics and integrated optical components with sub-wavelength features. In the future, mass production can be envisioned supposing the etched structures to be used for stamp fabrication in nanoimprint lithography [119]. Moreover, the manipulation of TMAH etchant by additive surfactants increases the versatility of the shapes that can be created.

In a wider scope, the achievements of this thesis deepen the understanding related to the stress control in silicon sensor fabrication. The effect of inhomogeneous dopant distribution on the deformation of mechanical structures was investigated. The behaviour was theoretically predicted by perceiving the dopant-induced change in the crystal lattice parameter. The scope of this work was on the experimental study, and despite of the approximations made, the accuracy of the presented model is adequate for evaluating the physical mechanism of the stress generation in the fabricated SOI test structures. When the results are practically applied to device design, finite element modeling (FEM) is advisable [120, 121]. The development of a FEM based model that predicts the behaviour of a structure with an arbitrary shape, doping type, and processing history would extend the value of the study and be a potential topic of future research. It can be concluded that a careful selection of substrate characteristics, thin-film materials, and fabrication methods have a key role in minimizing stress-related effects in high quality device production.

Bibliography

[1] H. G. Craighead. Nanoelectromechanical systems. *Science*, 290(5496):1532–1535, 2000.

[2] K. L. Ekinci. Electromechanical transducers at the nanoscale: actuation and sensing of motion in nanoelectromechanical systems (NEMS). *Small*, 1(8-9):786–797, 2005.

[3] B. Jalali and S. Fathpour. Silicon photonics. *Journal of Lightwave Technology*, 24(12):4600–4615, 2006.

[4] K. D. Hirschman, L. Tsybeskov, S. P. Duttagupta, and P. M. Fauchet. Silicon-based visible light-emitting devices integrated into microelectronic circuits. *Nature*, 384:338 – 341, 1996.

[5] M. A. Green. Recent developments in photovoltaics. *Solar Energy*, 76(1):3–8, 2004.

[6] K. E. Petersen. Silicon as a mechanical material. *Proceedings of the IEEE*, 70(5):420–457, 1982.

[7] J. B. Angell, P. W. Barth, and S. C. Terry. Silicon micromechanical devices. *Scientific American*, 248:44–55, 1983.

[8] T. Thorsen, S. J. Maerkl, and S. R. Quake. Microfluidic large-scale integration. *Science*, 298(5593):580–584, 2002.

[9] A. C. R. Grayson, R. S. Shawgo, A. M. Johnson, N. T. Flynn, Y. Li, M. J. Cima, and R. Langer. A BioMEMS review: MEMS technology for physiologically integrated devices. *Proceedings of the IEEE*, 92(1):6–21, 2004.

[10] A. Neukermans and R. Ramaswami. MEMS technology for optical networking applications. *IEEE Communications Magazine*, 39(1):62–69, 2001.

[11] A. Boisen, S. Dohn, S. S. Keller, S. Schmid, and M. Tenje. Cantilever-like micromechanical sensors. *Reports on Progress in Physics*, 74(3):036101, 2011.

[12] D. K. Shaeffer. MEMS inertial sensors: A tutorial overview. *IEEE Communications Magazine*, 51(4):100–109, 2013.

[13] V. Kaajakari. *Practical MEMS: Design of microsystems, accelerometers, gyroscopes, RF MEMS, optical MEMS, and microfluidic systems*. Small Gear Publishing, Las Vegas, US, 2009.

[14] S. D. Senturia. *Microsystem design*, volume 3. Kluwer Academic Publishers, Boston, US, 2001.

[15] K. D. Wise and K. Najafi. Microfabrication techniques for integrated sensors and microsystems. *Science*, 254(5036):1335–1342, 1991.

[16] J. Laconte, D. Flandre, and J.-P. Raskin. *Micromachined thin-film sensors for SOI-CMOS co-integration*. Springer, Dordrecht, Netherlands, 2006.

[17] G. T. A. Kovacs, N. I. Maluf, and K. E. Petersen. Bulk micromachining of silicon. *Proceedings of the IEEE*, 86(8):1536–1551, 1998.

[18] M. Elwenspoek and H. V. Jansen. *Silicon micromachining*. Cambridge University Press, Cambridge, UK, 2004.

[19] D. V. Dao, K. Nakamura, T. T. Bui, and S. Sugiyama. Micro/nano-mechanical sensors and actuators based on SOI-MEMS technology. *Advances in Natural Sciences: Nanoscience and Nanotechnology*, 1(1):013001, 2010.

[20] S. M. Spearing. Materials issues in microelectromechanical systems (MEMS). *Acta Materialia*, 48(1):179–196, 2000.

[21] C. R. Stoldt and V. M. Bright. Ultra-thin film encapsulation processes for micro-electro-mechanical devices and systems. *Journal of Physics D: Applied Physics*, 39(9):R163, 2006.

[22] K. C. Schwab and M. L. Roukes. Putting mechanics into quantum mechanics. *Physics Today*, 58(7):36–42, 2005.

[23] P. S. Waggoner and H. G. Craighead. Micro- and nanomechanical sensors for environmental, chemical, and biological detection. *Lab on a Chip*, 7(10):1238–1255, 2007.

[24] F. Patolsky, G. Zheng, and C. M. Lieber. Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species. *Nature Protocols*, 1(4):1711–1724, 2006.

[25] R. Hull (Ed.). *Properties of crystalline silicon*. Inspecs, London, UK, 1999.

[26] M. A. Hopcroft, W. D. Nix, and T. W. Kenny. What is the Young's modulus of silicon? *Journal of Microelectromechanical Systems*, 19(2):229–238, 2010.

[27] V. Lindroos, M. Tilli, A. Lehto, and T. Motooka (Eds.). *Handbook of silicon based MEMS materials and technologies*. William Andrew, Oxford, UK, 2009.

[28] F. H. Horn. Densitometric and electrical investigation of boron in silicon. *Physical Review*, 97(6):1521–1525, 1955.

[29] G. Celotti, D. Nobili, and P. Ostoja. Lattice parameter study of silicon uniformly doped with boron and phosphorus. *Journal of Materials Science*, 9(5):821–828, 1974.

[30] V. T. Bublik, S. S. Gorelik, and A. N. Dubrovina. Precision measurements of lattice periods of strongly doped germanium and silicon. *Soviet Physics Solid State*, 10(9):2247–2249, 1969.

[31] E. D. Palik, J. W. Faust, H. F. Gray, and R.F. Greene. Study of the etch-stop mechanism in silicon. *Journal of the Electrochemical Society*, 129(9):2051–2059, 1982.

[32] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel. Anisotropic etching of crystalline silicon in alkaline solutions II. Influence of dopants. *Journal of the Electrochemical Society*, 137(11):3626–3632, 1990.

[33] I. L. Berry and A. L. Caviglia. High resolution patterning of silicon by selective gallium doping. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 1(4):1059–1061, 1983.

[34] A. J. Steckl, H. C. Mogul, and S. Mogren. Localized fabrication of Si nanostructures by focused ion beam implantation. *Applied Physics Letters*, 60(15):1833–1835, 1992.

[35] L. Bischoff, B. Schmidt, H. Lange, and D. Donzev. Nano-structures for sensors on SOI by writing FIB implantation and subsequent anisotropic wet chemical etching. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 267(8):1372–1375, 2009.

[36] N. Chekurov, K. Grigoras, A. Peltonen, S. Franssila, and I. Tittonen. The fabrication of silicon nanostructures by local gallium implantation and cryogenic deep reactive ion etching. *Nanotechnology*, 20(6):065307, 2009.

[37] G. K. Celler and S. Cristoloveanu. Frontiers of silicon-on-insulator. *Journal of Applied Physics*, 93(9):4955–4978, 2003.

[38] R. C. Jaeger. Introduction to microelectronic fabrication. *Prentice Hall, Upper Saddle River, NJ, US*, 2002.

[39] A. S. Grove, O. Leistiko, and C. T. Sah. Redistribution of acceptor and donor impurities during thermal oxidation of silicon. *Journal of Applied Physics*, 35(9):2695–2701, 1964.

[40] S. Franssila. *Introduction to Microfabrication*. Wiley, Chichester, UK, 2010.

[41] B. Bhushan, S. P. Murarka, and J. Gerlach. Stress in silicon dioxide films deposited using chemical vapor deposition techniques and the effect of annealing on these stresses. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 8(5):1068–1074, 1990.

[42] K. R. Williams, K. Gupta, and M. Wasilik. Etch rates for micromachining processing-Part II. *Journal of Microelectromechanical Systems*, 12(6):761–778, 2003.

[43] T. Suntola. Atomic layer epitaxy. *Materials Science Reports*, 4(5):261–312, 1989.

[44] S. M. George. Atomic layer deposition: An overview. *Chemical Reviews*, 110:111–131, 2010.

[45] H. Kim, H.-B.-R. Lee, and W.-J. Maeng. Applications of atomic layer deposition to nanofabrication and emerging nanodevices. *Thin Solid Films*, 517(8):2563–2580, 2009.

[46] R. L. Puurunen, J. Saarilahti, and H. Kattelus. Implementing ALD layers in MEMS processing. *ECS Transactions*, 11(7):3–14, 2007.

[47] R. L. Puurunen. Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process. *Journal of applied physics*, 97(12):121301, 2005.

[48] K. Grigoras, L. Sainiemi, J. Tiilikainen, A. Säynätjoki, V.-M. Airaksinen, and S. Franssila. Application of ultra-thin aluminum oxide etch mask made by atomic layer deposition technique. *Journal of Physics: Conference Series*, 61(1):369–373, 2007.

[49] S. Greek and N. Chitica. Deflection of surface-micromachined devices due to internal, homogeneous or gradient stresses. *Sensors and Actuators A: Physical*, 78(1):1–7, 1999.

[50] J. Thornton and D. Hoffman. Stress-related effects in thin films. *Thin Solid Films*, 171(1):5–31, 1989.

[51] M. Ohring. *Materials science of thin films*. Academic press, San Diego, US, 2001.

[52] G. G. Stoney. The tension of metallic films deposited by electrolysis. *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, 82(553):172–175, 1909.

[53] L. B. Freund, J. A. Floro, and E. Chason. Extensions of the Stoney formula for substrate curvature to configurations with thin substrates or large deformations. *Applied Physics Letters*, 74(14):1987–1989, 1999.

[54] T. Ito and S. Okazaki. Pushing the limits of lithography. *Nature*, 406(6799):1027–1031, 2000.

[55] H. J. Levinson. *Principles of lithography, (3rd Ed.)*. SPIE, Washington, US, 2010.

[56] M. l. Totzeck, W. Ulrich, A. Göhnermeier, and W. Kaiser. Semiconductor fabrication: Pushing deep ultraviolet lithography to its limits. *Nature Photonics*, 1(11):629–631, 2007.

[57] R. F. Pease and S. Y. Chou. Lithography and other patterning techniques for future electronics. *Proceedings of the IEEE*, 96(2):248–270, 2008.

[58] L. J. Guo. Nanoimprint lithography: Methods and material requirements. *Advanced Materials*, 19(4):495–513, 2007.

[59] A. A. Tseng. Recent developments in nanofabrication using focused ion beams. *Small*, 1(10):924–939, 2005.

[60] C.-S. Kim, S.-H. Ahn, and D.-Y. Jang. Review: Developments in micro/nanoscale fabrication by focused ion beams. *Vacuum*, 86(8):1014–1035, 2012.

[61] D. Vick, V. Sauer, A. E. Fraser, M. R. Freeman, and W. K. Hiebert. Bulk focused ion beam fabrication with three-dimensional shape control of nanoelectromechanical systems. *Journal of Micromechanics and Microengineering*, 20(10):105005, 2010.

[62] S. Reyntjens and R. Puers. A review of focused ion beam applications in microsystem technology. *Journal of Micromechanics and Microengineering*, 11(4):287–300, 2001.

[63] N. Chekurov, K. Grigoras, L. Sainiemi, A. Peltonen, I. Tittonen, and S. Franssila. Dry fabrication of microdevices by the combination of focused ion beam and cryogenic deep reactive ion etching. *Journal of Micromechanics and Microengineering*, 20(8):085009, 2010.

[64] A. C. Fischer, L. M. Belova, Y. G. M. Rikers, B. G. Malm, H. H. Radamson, M. Kolahdouz, K. B. Gylfason, G. Stemme, and F. Niklaus. 3D free-form patterning of silicon by ion implantation, silicon deposition, and selective silicon etching. *Advanced Functional Materials*, 22(19):4004–4008, 2012.

[65] Z. Liu, K. Iltanen, N. Chekurov, K. Grigoras, and I. Tittonen. Aluminum oxide mask fabrication by focused ion beam implantation combined with wet etching. *Nanotechnology*, 24(17):175304, 2013.

[66] S. Takahashi, M. Ohashi, S. Fukatsu, Y. Shiraki, and R. Ito. Sub-100 nm pattern formation using a novel lithography with SiNx resist by focused ion beam exposure and dry-etching development. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 11(2):268–274, 1993.

[67] K. Sudoh and S. Sakakihara. Focused ion beam induced surface damage effect on the mechanical properties of silicon nanowires. *Journal of Engineering Materials and Technology*, 135:041002, 2013.

[68] K. E. Bean. Anisotropic etching of silicon. *IEEE Transactions on Electron Devices*, 25(10):1185–1193, 1978.

[69] J. B. Price. *Anisotropic etching of silicon with KOH-H2O-isopropyl alcohol*. H. R. Huff and R. R. Burgess (Eds.), Princeton, NJ: Electrochemical Society, 1973.

[70] R. M. Finne and D. L. Klein. A water-amine-complexing agent system for etching silicon. *Journal of The Electrochemical Society*, 114(9):965–970, 1967.

[71] O. Tabata, R. Asahi, H. Funabashi, K. Shimaoka, and S. Sugiyama. Anisotropic etching of silicon in TMAH solutions. *Sensors and Actuators A: Physical*, 34(1):51–57, 1992.

[72] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel. Anisotropic etching of crystalline silicon in alkaline solutions I. Orientation dependence and behavior of passivation layers. *Journal of the Electrochemical Society*, 137(11):3612–3626, 1990.

[73] K. Biswas and S. Kal. Etch characteristics of KOH, TMAH and dual doped TMAH for bulk micromachining of silicon. *Microelectronics Journal*, 37(6):519–525, 2006.

[74] J. T. L. Thong, W. K. Choi, and C. W. Chong. TMAH etching of silicon and the interaction of etching parameters. *Sensors and Actuators A: Physical*, 63(3):243–249, 1997.

[75] K. Sato, M. Shikida, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto. Anisotropic etching rates of single-crystal silicon for TMAH water solution as a function of crystallographic orientation. *Sensors and Actuators A: Physical*, 73(1):131–137, 1999.

[76] L. M. Landsberger, M. Naseh, S.and Kahrizi, and M. Paranjape. On hillocks generated during anisotropic etching of Si in TMAH. *Journal of Microelectromechanical Systems*, 5(2):106–116, 1996.

[77] P. Papet, O. Nichiporuk, A. Kaminski, Y. Rozier, J. Kraiem, J.-F. Lelievre, A. Chaumartin, A. Fave, and M. Lemiti. Pyramidal texturing of silicon solar cell with TMAH chemical anisotropic etching. *Solar Energy Materials and Solar Cells*, 90(15):2319–2328, 2006.

[78] S. Sridharan, N. Bhat, and K. N. Bhat. Silicon surface texturing with a combination of potassium hydroxide and tetra-methyl ammonium hydroxide etching. *Applied Physics Letters*, 102(2):021604, 2013.

[79] I. Zubel, M. Kramkowska, and K. Rola. Silicon anisotropic etching in TMAH solutions containing alcohol and surfactant additives. *Sensors and Actuators A: Physical*, 178:126–135, 2012.

[80] C.-R. Yang, C.-H. Yang, and P.-Y. Chen. Study on anisotropic silicon etching characteristics in various surfactant-added tetramethyl ammonium hydroxide water solutions. *Journal of Micromechanics and Microengineering*, 15(11):2028–2037, 2005.

[81] K. B. Sundaram, A. Vijayakumar, and G. Subramanian. Smooth etching of silicon using TMAH and isopropyl alcohol for MEMS applications. *Microelectronic Engineering*, 77(3):230–241, 2005.

[82] P. Pal, K. Sato, M. A. Gosalvez, B. Tang, H. Hida, and M. Shikida. Fabrication of novel microstructures based on orientation-dependent adsorption of surfactant molecules in a TMAH solution. *Journal of Micromechanics and Microengineering*, 21(1):015008, 2011.

[83] D. Resnik, D. Vrtacnik, U. Aljancic, M. Mozek, and S. Amon. The role of Triton surfactant in anisotropic etching of {110} reflective planes on (100) silicon. *Journal of Micromechanics and Microengineering*, 15(6):1174–1183, 2005.

[84] H. Jansen, H. Gardeniers, M. de Boer, M. Elwenspoek, and J. Fluitman. A survey on the reactive ion etching of silicon in microtechnology. *Journal of Micromechanics and Microengineering*, 6(1):14–28, 1996.

[85] B. Wu, A. Kumar, and S. Pamarthy. High aspect ratio silicon etch: A review. *Journal of Applied Physics*, 108(5):051101, 2010.

[86] M. J. de Boer, J. G. E. Gardeniers, H. V. Jansen, E. Smulders, M.-J. Gilde, G. Roelofs, J. N. Sasserath, and M. Elwenspoek. Guidelines for etching silicon MEMS structures using fluorine high-density plasmas at cryogenic temperatures. *Journal of Microelectromechanical Systems*, 11(4):385–401, 2002.

[87] T. M. Mayer, J. W. Elam, S. M. George, P. G. Kotula, and R. S. Goeke. Atomic-layer deposition of wear-resistant coatings for microelectromechanical devices. *Applied Physics Letters*, 82(17):2883–2885, 2003.

[88] R. L. Puurunen, A. Häärä, H. Saloniemi, J. Dekker, M. Kainlauri, H. Pohjonen, T. Suni, J. Kiihamäki, E. Santala, M. Leskelä, and H. Kattelus. Reducing stiction in microelectromechanical systems by rough nanometer-scale films grown by atomic layer deposition. *Sensors and Actuators A: Physical*, 188:240–245, 2012.

[89] A. Szeghalmi, M. Helgert, R. Brunner, F. Heyroth, U. Gösele, and M. Knez. Atomic layer deposition of Al_2O_3 and TiO_2 multilayers for applications as bandpass filters and antireflection coatings. *Applied optics*, 48(9):1727–1732, 2009.

[90] O. Hahtela, N. Chekurov, and I. Tittonen. Non-tilting out-of-plane mode high-Q mechanical silicon oscillator. *Journal of Micromechanics and Microengineering*, 15(10):1848–1853, 2005.

[91] O. Hahtela and I. Tittonen. Non-tilting out-of-plane mode high-Q mechanical silicon oscillator as a moving cavity mirror. *Applied Physics B*, 88(3):417–423, 2007.

[92] N. Chekurov. Fabrication process development for silicon micro and nanosystems. *Dissertation, Aalto University School of Electrical Engineering*, 2011.

[93] C. Haisch. Photoacoustic spectroscopy for analytical measurements. *Measurement Science and Technology*, 23(1):012001, 2012.

[94] F. J. M. Harren, G. Cotti, J. Oomens, and S. te Lintel Hekkert. *Photoacoustic spectroscopy in trace gas monitoring*. Encyclopedia of Analytical Chemistry, R. A. Meyers (Ed.), 2203–2226, Wiley, Chichester, UK, 2000.

[95] J. Li, W. Chen, and B. Yu. Recent progress on infrared photoacoustic spectroscopy techniques. *Applied Spectroscopy Reviews*, 46(6):440–471, 2011.

[96] K. Wilcken and J. Kauppinen. Optimization of a microphone for photoacoustic spectroscopy. *Applied spectroscopy*, 57(9):1087–1092, 2003.

[97] J. Kauppinen, K. Wilcken, I. Kauppinen, and V. Koskinen. High sensitivity in gas analysis with photoacoustic detection. *Microchemical journal*, 76(1):151–159, 2004.

[98] R. E. Lindley, A. M. Parkes, K. A. Keen, E. D. McNaghten, and A. J. Orr-Ewing. A sensitivity comparison of three photoacoustic cells containing a single microphone, a differential dual microphone or a cantilever pressure sensor. *Applied Physics B*, 86(4):707–713, 2007.

[99] T. Kuusela and J. Kauppinen. Photoacoustic gas analysis using interferometric cantilever microphone. *Applied Spectroscopy Reviews*, 42(5):443–474, 2007.

[100] J. Uotila. Use of the optical cantilever microphone in photoacoustic spectroscopy. *Annales Universitatis Turkuensis AI 395*, 2009.

[101] J. Kauppinen, T. Kuusela, P. Malmi, and J. Raittila. Brownian noise of the interferometric cantilever microphone used in photoacoustic trace gas detectors. *Pittcon 2009 Book of Abstracts*, 2009.

[102] J. Kauppinen, K. Wilcken, I. Kauppinen, and V. Koskinen. High sensitivity in gas analysis with photoacoustic detection. *Microchemical journal*, 76(1):151–159, 2004.

[103] J. Uotila. Comparison of infrared sources for a differential photoacoustic gas detection system. *Infrared Physics & Technology*, 51(2):122–130, 2007.

[104] J. Fonsen, V. Koskinen, K. Roth, and J. Kauppinen. Dual cantilever enhanced photoacoustic detector with pulsed broadband IR-source. *Vibrational Spectroscopy*, 50(2):214–217, 2009.

[105] H. Cattaneo, T. Laurila, and R. Hernberg. Photoacoustic detection of oxygen using cantilever enhanced technique. *Applied Physics B*, 85(2-3):337–341, 2006.

[106] J. Uotila and J. Kauppinen. Fourier transform infrared measurement of solid-, liquid-, and gas-phase samples with a single photoacoustic cell. *Applied Spectroscopy*, 62(6):655–660, 2008.

[107] V. Koskinen, J. Fonsen, K. Roth, and J. Kauppinen. Cantilever enhanced photoacoustic detection of carbon dioxide using a tunable diode laser source. *Applied Physics B*, 86(3):451–454, 2007.

[108] L. Dong, A. A. Kosterev, D. Thomazy, and F. K. Tittel. QEPAS spectrophones: Design, optimization, and performance. *Applied Physics B*, 100(3):627–635, 2010.

[109] M. E. Webber, M. Pushkarsky, and C. K. N. Patel. Fiber-amplifier-enhanced photoacoustic spectroscopy with near-infrared tunable diode lasers. *Applied optics*, 42(12):2119–2126, 2003.

[110] F. Maseeh and S. D. Senturia. Plastic deformation of higly doped silicon. *Sensors and Actuators A: Physical*, 23(1):861–865, 1990.

[111] X. Ding, W. H. Ko, and J. M. Mansour. Residual stress and mechanical properties of boron-doped p^+-silicon films. *Sensors and Actuators A: Physical*, 23(1):866–871, 1990.

[112] W.-H. Chu and M. Mehregany. A study of residual stress distribution through the thickness of p^+ silicon films [thermal oxidation effects]. *IEEE Transactions on Electron Devices*, 40(7):1245–1250, 1993.

[113] E. H. Yang and S. S. Yang. The quantitative determination of the residual stress profile in oxidized p^+ silicon films. *Sensors and Actuators A: Physical*, 54(1):684–689, 1996.

[114] F. Gaiseanu, J. Esteve, C. Cané, A. Perez-Rodriguez, J. R. Morante, and C. Serre. Doping and structural properties of the phosphorus doped polysilicon layers used for micromechanical applications. *Proceedings of SPIE 3874, Micromachining and Microfabrication Process Technology V*, 3874:412–421, 1999.

[115] SILVACO Int. ATHENA User's manual. Santa Clara, CA, USA, 2012.

[116] R. E. Pearson, K. D. Hirschman, and R. Manley. Process model verification for dopant segregation and oxidation enhanced diffusion. *University/Government/Industry Micro/Nano Symposium, 2008. UGIM 2008. 17th Biennial*, 2008.

[117] T. W. Clyne. Residual stresses in surface coatings and their effects on interfacial debonding. *Key Engineering Materials*, 116:307–330, 1996.

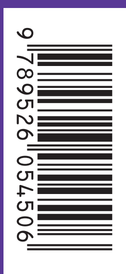
[118] J. F. Ziegler and J. P. Biersack. SRIM 2008 - the stopping and range of ions in matter. *http://www.srim.org/*, cited 1. Sept. 2009.

[119] S. Waid, H. D. Wanzenboeck, M. Muehlberger, and E. Bertagnolli. Optimization of 3D patterning by Ga implantation and reactive ion etching (RIE) for nanoimprint lithography (NIL) stamp fabrication. *Microelectronic Engineering*, 97:105–108, 2012.

[120] F. Ericson, S. Greek, J. Söderkvist, and J.-Å. Schweitz. High-sensitivity surface micromachined structures for internal stress and stress gradient evaluation. *Journal of Micromechanics and Microengineering*, 7(1):30–36, 1997.

[121] L. Durand, M. Massaoudi, M. Cabié, and A. Ponchet. Mechanical behaviour of a two-phase material from the behaviour of its components: Interface modelling by finite element method. *Materials & Design*, 29(8):1609–1615, 2008.

Aalto-DD 193/2013



ISBN 978-952-60-5450-6
ISBN 978-952-60-5451-3 (pdf)
ISSN-L 1799-4934
ISSN 1799-4934
ISSN 1799-4942 (pdf)

Aalto University
School of Electrical Engineering
Department of Micro and Nanosciences
www.aalto.fi

BUSINESS +
ECONOMY

ART +
DESIGN +
ARCHITECTURE

SCIENCE +
TECHNOLOGY

CROSSOVER

DOCTORAL
DISSERTATIONS