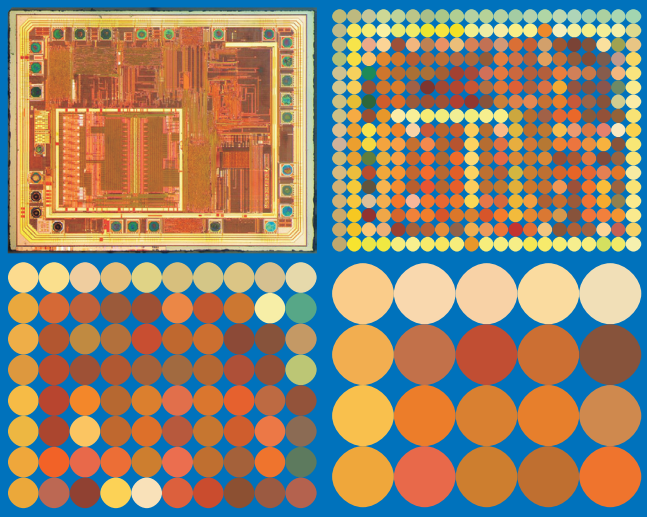
Department of Radio Science and Engineering

Partitioning and macromodeling -based realizable reduction of interconnect circuit models

Pekka Miettinen



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Partitioning and macromodeling -based realizable reduction of interconnect circuit models

Pekka Miettinen

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School of Electrical Engineering
Department of Radio Science and Engineering
Circuit Theory

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Abstract

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Abstract

With advancing technology of integrated circuits, the interconnects and their non-ideal parasitics between active elements play an increasingly important role for the signal behavior. In a typical design flow, extraction tools are often used to generate a circuit netlist from the original chip topology for post-layout verification simulations. To reach desired accuracy, the interconnects and their parasitics need to be modeled with high precision that generates huge RLCK netlists, which in turn poses significant run-time and memory problems for the design process. One avenue to speed up the verification step is to apply model-order reduction (MOR) algorithms to the extracted netlists attempting to model the system with a reduced-size representation.

This thesis details the research of partitioning and macromodel-based MOR approach for linear RLCK circuits. Using partitioning in MOR to first divide the circuit into smaller subcircuits makes it possible to use low-order approximations per each partition and still retain a good overall approximation accuracy for the total reduced circuit, when the individually reduced partitions are recombined. This use of low-order approximations in turn guarantees numerical stability and allows the approximations to be matched with relatively simple positive-valued RLCK macromodels, resulting in a realizable RLCK-in–RLCK-out reduction.

Partitioning is known to provide the MOR also many other benefits, such as block-level sparsity, facilitated terminal node handling, reduced computational memory demands, and an option for natural parallel processing. Thanks to the many desirable features provided, this thesis aims to show that the presented MOR approach is highly efficient and well comparable to previously published MOR methods, especially in the case of typical interconnect RLCK circuits.

The publications of this thesis first discuss the development of efficient RC and RL MOR methods, and the hierarchical approach to MOR offered by partitioning. Then, an RLC MOR method, PartMOR, using the same approach is presented. The latter four publications of this thesis focus on refining the presented methods and solving common difficulties in MOR: Singularity-generating structures in the original circuit can be avoided by isolating such structures with partitioning. Dense coupling of mutual inductances and capacitances between interconnects can be reduced with partitioning and a two-stage approximation. Finally, combining the presented methods together results in a complete RLCK-in–RLCK-out MOR algorithm package.

Keywords Circuit simulation, interconnect modeling, model-order reduction

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Tiivistelmä

Mikropiiriteknologian kehityksen myötä liitosjohtojen epäideaalisten ilmiöiden vaikutukset ovat nousseet signaalinkulun kannalta yhä tärkeämmäksi tekijäksi. Jotta piirien simulaatioissa päästäisiin vaadittuun realistisuuteen, on näitä epäideaalisuuksia mallinnettava suurella tarkkuudella, mikä voi tuottaa helposti tuloksenaan valtavia RLCK-piirikuvauksia. Mallien suuri koko puolestaan aiheuttaa simulaatioihin numeerisia ongelmia. Eräs keino helpottaa ongelmaa on käyttää malliredusointia, joka pyrkii approksimoimaan alkuperäistä kuvausta toisella, pienemmällä mallilla.

Tämä väitöskirja esittelee malliredusointiin soveltuvan algoritmikokoelman tutkimus- ja kehitystyön, jonka kantavana ideana on hyödyntää piirijakoa ja makromalleja. Käyttämällä piirijakoa alkuperäinen piiriongelma voidaan jakaa pienempiin osiin. Tämä mahdollistaa piirijakojen approksimoinnin matalan asteluvun malleilla, jotka säilyttävät silti riittävän approksimaatiotarkkuuden, kun kyseiset mallit yhdistetään redusoinnin lopuksi takaisin yhdeksi kokonaisuudeksi. Matalan asteluvun mallien käyttäminen puolestaan takaa redusoinnin numeerisen stabiiliuden ja mahdollistaa mallien esittämisen positiivisarvoisilla RLCK-makromalleilla. Näin malliredusointivuo pystyy tuottamaan tavallisilla piirielementeillä realisoitavia malleja ja varmistaa siten redusointitulosten helpon jatkokäytön.

Piirijako auttaa malliredusointia tutkitusti monin tavoin, kuten tuottamalla lohkotasolla harvoja matriiseja, helpottamalla moniporttisten piirien redusointia, vähentämällä muistinkulutusta ja tarjoamalla luonnollisen keinon rinnakkaisprosessoinnille. Tämä väitöskirja pyrkii osoittamaan, että esitetty piirijakoon ja makromalleihin pohjautuva lähestymistapa malliredusointiin on tehokas ja vertailukelpoinen vaihtoehto aiemmin julkaistuihin redusointimenetelmiin verrattuna — erityisesti liitinjohtotyyppisten RLCK-piirien tapauksessa.

Työn ensimmäiset julkaisut käsittelevät tehokkaiden RC- ja RL-redusointimenetelmien tutkimusta ja kehitystä, sekä piirijaon mahdollistamaa hierarkista lähestymistapaa malliredusointiin. Tämän jälkeen esitellään yleisempään RLC-redusointiin sopiva menetelmä, PartMOR. Väitöskirjan viimeiset neljä julkaisua keskittyvät esiteltyjen menetelmien hiomiseen sekä eräiden malliredusoinnin ongelmakohtien ratkomiseen: Singulaarisuuksia tuottavat rakenteet voidaan eristää redusoinnista piirijaon avulla. Tiheät kapasitiiviset ja induktiiviset kytkennät liitinjohtojen välillä voidaan redusoida piirijaolla ja kaksiportaisella approksimaatiolla. Lopuksi yhdistämällä esitetyt parannukset yhdeksi redusointivuoksi saadaan aikaan RLCK-piirien redusointiin soveltuva algoritmikokonaisuus.

Avainsanat Piirisimulointi, liitinjohtomallinnus, malliredusointi

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Preface

The research for this thesis was carried out between 2007–2013 in a research group led by Prof. Martti Valtonen at the Circuit Theory Laboratory, which merged in 2008 with three other laboratories to form the Department of Radio Science and Engineering at the Helsinki University of Technology. Helsinki University of Technology itself merged with two other universities in 2010. The Department of Radio Science and Engineering belongs currently to the Aalto University School of Electrical Engineering.

This work was partially funded by the Graduate School in Electronics, Telecommunications and Automation (GETA) and by the Academy of Finland. Financial support from the Nokia Foundation and the Foundation of Walter Ahlström is also acknowledged and deeply appreciated.

I wish to express my gratitude to Prof. Martti Valtonen for providing the friendly research environment in the circuit theory group. I wish to thank Mikko Honkala and Janne Roos for instruction on my research topic and additional guidance on how to be a research scientist on a daily basis. Thanks are due to Ari Sihvola for generous support with cross-disciplinary research attempts, and later at GETA for instruction on publishing practises. I would like to thank all the (also past) members of the circuit theory group, especially Luis Costa, Anu Lehtovuori, Kimmo Silvonen, Timo Veijola, and Jarmo Virtanen for inspiring coffee breaks, technical help, supportive atmosphere, and all the other stuff that is required for a successful research, but is not printed in the author line of a paper.

Lastly, I would like to thank my friends and family for support over the years. Thank you, muksupuksut, for pizza fridays. Thank you, Järjestysmiehet, for the music. Thank you, orcd2-team, for games, food, and other projects. Thank you, Marjukka, for everything else.

Helsinki, January 13, 2014,

Pekka Miettinen

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I P. Miettinen, M. Honkala, J. Roos, C. Neff, and A. Basermann. Study and development of an efficient RC-in–RC-out MOR method. In *Proceedings of the 15th IEEE International Conference on Electronics, Circuits and Systems, ICECS'08*, Malta, pp. 1277–1280, Aug. 2008.

II P. Miettinen, M. Honkala, and J. Roos. Partitioning-based RL-in–RL-out MOR method. *Mathematics in Industry 14: Scientific Computing in Electrical Engineering SCEE 2008*, J. Roos and L. R. J. Costa, Eds. Berlin, Germany: Springer-Verlag, pp. 547–554, Jan. 2010.

III M. Honkala, P. Miettinen, J. Roos, and C. Neff. Hierarchical model-order reduction flow. *Mathematics in Industry 14: Scientific Computing in Electrical Engineering SCEE 2008*, J. Roos and L. R. J. Costa, Eds. Berlin, Germany: Springer-Verlag, pp. 539–546, Jan. 2010.

IV P. Miettinen, M. Honkala, J. Roos, and M. Valtonen. PartMOR: Partitioning-based realizable model-order reduction method for RLC circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 3, pp. 374–387, March 2011.

V P. Miettinen, M. Honkala, J. Roos, and M. Valtonen. Improving model-order reduction methods by singularity exclusion. *Mathematics in Industry 16: Scientific Computing in Electrical Engineering SCEE 2010*,

B. Michielsen and J. -R. Poirier, Eds. Berlin, Germany: Springer-Verlag, pp. 395–404, Jan. 2012.

VI P. Miettinen, M. Honkala, J. Roos, and M. Valtonen. Partitioning-based reduction of circuits with mutual inductances. *Mathematics in Industry 16: Scientific Computing in Electrical Engineering SCEE 2010*, B. Michielsen and J. -R. Poirier, Eds. Berlin, Germany: Springer-Verlag, pp. 395–404, Jan. 2012.

VII P. Miettinen, M. Honkala, J. Roos, and M. Valtonen. Sparsification of dense capacitive coupling of interconnects. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 10, pp. 1955–1959, Oct. 2013.

VIII P. Miettinen, M. Honkala, J. Roos, and M. Valtonen. Realizable reduction of interconnect models with dense coupling. In *European Conference on Circuit Theory and Design (ECCTD) 2013*, Dresden, Germany, pp. 1–4, Sept. 2013.

Author's Contribution

Publication I: "Study and development of an efficient RC-in–RC-out MOR method"

The author carried out a large portion of the method implementation of this paper (namely, partitioning, rebuilding of the reduced partitions, and implementing TICER). Similarly, all the extensive simulations to compare the different methods were done by the author. Finally, conclusive analysis of the simulation results was done by the author for the major part. D.Sc. (Tech.) Mikko Honkala was responsible for implementing the remaining (major) part of the MOR flow, of analyzing the nodal formulation-based circuit-equation approach, and deriving the simplified macromodel approach together with D.Sc. (Tech.) Janne Roos. D.Sc. (Tech.) Roos contributed substantially to the paper through discussions, an initial study of the Liao and Dai and PRIMA methods, and by organizing the research results into the three comparison steps in the manuscript. M.Sc. Carsten Neff helped with discussions on the implementation. The author carried the responsibility of writing the publication manuscript.

Publication II: "Partitioning-based RL-in–RL-out MOR method"

The development and evaluation of the proposed method, as well as the writing of the manuscript, was done by the author. D.Sc. (Tech.) Mikko Honkala and D.Sc. (Tech.) Janne Roos helped with discussions and by commenting the text.

Publication III: "Hierarchical model-order reduction flow"

This paper and the related additional research was inspired by the discoveries in the test simulations performed during the development of [PI]. Thus, the contributions stated above for paper [PI] apply here for the development of the method. The author's additional contribution to the paper was writing two preliminary sections of the manuscript, discussions, and commenting the text. D.Sc. (Tech.) Janne Roos helped through discussions and by commenting the text.

Publication IV: "PartMOR: Partitioning-based realizable model-order reduction method for RLC circuits"

The original idea, development, and evaluation of the proposed method, as well as the writing of the manuscript was done by the author. D.Sc. (Tech.) Mikko Honkala helped substantially with discussions on the theory at various points during the development of the method and by commenting the text. D.Sc. (Tech.) Janne Roos helped with preparing the manuscript and with additional discussions.

Publication V: "Improving model-order reduction methods by singularity exclusion"

The original idea, development, and evaluation of the proposed method, as well as the writing of the manuscript was done by the author. D.Sc. (Tech.) Mikko Honkala and D.Sc. (Tech.) Janne Roos helped with discussions and by commenting the text.

Publication VI: "Partitioning-based reduction of circuits with mutual inductances"

The original idea, development, and evaluation of the proposed method, as well as the writing of the manuscript was done by the author. D.Sc. (Tech.) Mikko Honkala and D.Sc. (Tech.) Janne Roos helped with discussions and by commenting the text.

Publication VII: "Sparsification of dense capacitive coupling of interconnects"

The original idea, development, and evaluation of the proposed method, as well as the writing of the manuscript was done by the author. D.Sc. (Tech.) Mikko Honkala and D.Sc. (Tech.) Janne Roos helped with discussions and by commenting the text.

Publication VIII: "Realizable reduction of interconnect models with dense coupling"

The original idea, development, and evaluation of the proposed method, as well as the writing of the manuscript was done by the author. D.Sc. (Tech.) Mikko Honkala and D.Sc. (Tech.) Janne Roos helped with discussions and by commenting the text.

Symbols

$\mathbf{0}$	zero matrix
$\mathbf{A}$	system or generic matrix
$\tilde{\mathbf{A}}$	reduced order $\mathbf{A}$
$\mathbf{B}$	MNA matrix containing current variables for KCL equations
$\mathbf{B}_1$	non-zero submatrix of $\mathbf{B}$
$\tilde{\mathbf{B}}$	$\mathbf{B}$ after congruence transformation
$\tilde{\mathbf{B}}_1$	$\mathbf{B}_1$ after congruence transformation
$\mathbf{b}$	vector containing inputs, e.g., voltages
$\tilde{\mathbf{b}}$	reduced order $\mathbf{b}$
C	capacitance
$\mathbf{C}$	MNA matrix containing capacitance and inductance stamps
$\mathbf{C}_{11}$	MNA submatrix containing capacitance stamps
$\tilde{\mathbf{C}}$	$\mathbf{C}$ after congruence transformation
$\tilde{\mathbf{C}}_{11}$	$\mathbf{C}_{11}$ after SPRIM reduction
C_K	total node capacitance, sum of c_{iK}
c_{iK}	i:th capacitance branch connected to node K
c'_{ij}	approximating capacitance for node K between nodes i and j
G	conductance
$\mathbf{G}$	MNA matrix containing conductance stamps and current variables
$\mathbf{G}_{11}$	MNA submatrix containing conductance stamps
$\mathbf{G}_{12}$	MNA submatrix containing KCL current stamps
$\mathbf{G}_{21}$	MNA submatrix containing KCL current stamps
$\tilde{\mathbf{G}}$	$\mathbf{G}$ after congruence transformation
$\tilde{\mathbf{G}}_{11}$	$\mathbf{G}_{11}$ after congruence transformation
$\tilde{\mathbf{G}}_{12}$	$\mathbf{G}_{12}$ after congruence transformation
$\tilde{\mathbf{G}}_{21}$	$\mathbf{G}_{21}$ after congruence transformation
G_K	node conductance, sum of g_{iK}

g_{iK}	i:th conductance branch connected to node N
g'_{ij}	approximating conductance for node K between nodes i and j
$\mathbf{H}$	MNA matrix containing inductance stamps
$\mathbf{I}$	identity matrix
$I_{a,b}$	current running in branch between nodes a and b
I_{in}	current entering a branch
I_{out}	current exiting a branch
$\mathbf{i}_N$	vector containing MNA port currents
i	index or current
j	index variable
K	number of partitions between the terminal ports or the central node to be eliminated in TICER
k	index variable
$\mathbf{L}$	selector matrix
$\mathbf{L}_{22}$	MNA submatrix of $\mathbf{C}$ containing inductance stamps
$\tilde{\mathbf{L}}_{22}$	$\mathbf{L}_{22}$ after congruence transformation
L	inductance
$\tilde{\mathbf{L}}$	$\mathbf{L}$ after congruence transformation
$\mathbf{M}_i$	ith block moment of $\mathbf{Y}$
M_Σ	total (approximated) mutual inductance between two branches
m_n^{ij}	(i,j):th element of the nth block moment
$\mathbf{N}$	MNA matrix containing conductance stamps
N	number of ports in a circuit, also the dimension of the block moment
n	dimension of a matrix
n_{e}	number of external nodes
$n_{\text{e,p}}$	number of external nodes in a partition
n_{i}	number of internal nodes
n_{L}	number of inductances
p	number of partitions
$\mathbf{Q}$	MNA matrix containing capacitance stamps
q	order of reduction
q_{p}	order of one y-parameter element
q_{red}	total order of a cascaded (reduced) circuit system
R	resistance
T_K	node time constant
$\mathbf{U}_k$	voltage of port k
$U^{a,b}$	voltage between nodes a and b
$\mathbf{u}_N$	vector containing MNA port voltages

$\mathbf{v}$	vector containing node voltages
$\mathbf{X}$	$n \times q$ matrix obtained from block Arnoldi iteration
$\mathbf{X}_1$	$(n_\mathrm{i} + n_\mathrm{e}) \times q$ submatrix of $\mathbf{X}$
$\mathbf{X}_2$	$n_\mathrm{L} \times q$ submatrix of $\mathbf{X}$
$\tilde{\mathbf{X}}$	$n \times 2q$ projection matrix used by SPRIM
$\mathbf{x}$	vector containing unknown variables, e.g. voltages
$\tilde{\mathbf{x}}$	reduced order $\mathbf{x}$
$\mathbf{x}_n$	vector containing MNA node voltages and currents
$\mathbf{Y}$	admittance matrix
$\mathbf{Y}(s)$	$\mathbf{Y}$-parameter matrix in Laplace form
y_{ij}	(i,j):th element of the $\mathbf{Y}$ matrix
y_k^{ij}	(i,j):th element of the $\mathbf{Y}$ matrix of the kth cascaded block
y_k^A	y_k^A=y_k^{11}+y_k^{12}, an admittance element
y_k^B	y_k^B=y_k^{22}+y_k^{12}, an admittance element
α	number of elements or number of mutual inductances
β	number of self inductances
$\mathbf{\Gamma}$	nodal analysis matrix containing stamps for inductances
γ	number of self inductances
δ	number of resistances
ζ	number of resistances

Abbreviations

APLAC	an object oriented analog circuit simulator and design tool (originally Analysis Program for Linear Active Circuits)
BVOR	a block-structure-preserving MOR method
BSMOR	a block-structure-preserving MOR method
CPU	central processing unit
DC	direct current
EDA	electronic design automation
hiePrimor	a partitioning-based Krylov-subspace RLC MOR method
HiPRIME	hierarchical and passivity reserved interconnect macromodeling engine for RLKC power delivery
hMETIS	a software package for manipulating hypergraphs
IC	integrated circuit
KCL	Kirchhoff's current law
MATLAB	matrix laboratory, a programmable numerical calculation environment
METIS	a software package for manipulating graphs
MNA	modified nodal analysis
MOR	model-order reduction
NA	nodal analysis
PartMOR	a partitioning and macromodel-based RLC MOR method
POD	proper orthogonal decomposition
PRIMA	passive reduced-order interconnect macromodeling algorithm
PVL	Padé via Lanczos
PWL	piecewise-linear
ReduceR	efficient reduction of resistor networks
RLCSYN	RLC equivalent circuit synthesis for structure-preserved

	reduced order model of interconnect
ROM	reduced-order model
SparceRC	a partitioning-based RC MOR method
SPICE	simulation program with integrated circuit emphasis
SPRIM	structure-preserving reduced-order interconnect macro-modeling
TBR	truncated balanced realization
TICER	time constant equilibration reduction
VCCS	voltage-controlled current source

1. Introduction

1.1 MOR in general

When studying a phenomenon in a mathematically rigorous fashion, it is often useful to formulate a descriptory model to capture some key features of the system under study. Once this is done, the phenomenon may be observed in a controlled environment by virtual simulations, typically using a computer. However, in the case where the phenomenon is very complex, and accurate representation is required, the describing model may become too heavy to simulate in a reasonable time.

The idea of model-order reduction (MOR) is to simplify the original accurate models by approximating the model with another simpler model. In the best case, the reduced-order model (ROM) is of small size compared to the original but retains those characteristics of the original model that are most important to the user and still describes the original phenomenon with sufficient accuracy. In practice, the reduction process generates some error in a trade-off for a smaller, lighter system.

As a field of science, MOR is relatively young, but its applications are wide and interdisciplinary. In circuit design, one typical application of MOR is in the verification simulation step of large integrated circuit (IC) designs.

1.2 MOR in circuit design

With advancing IC technology, the level of miniaturization (Fig. 1.1) is constantly increasing. To verify that the result of the IC design process works as expected, the behavior of the physical circuit model is simulated as a computational model before actual production. This is important

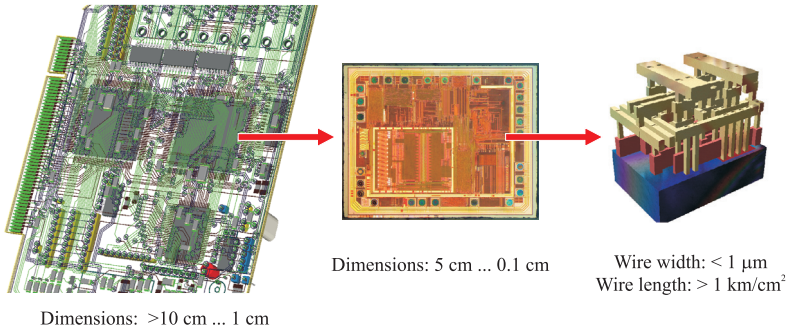


Figure 1.1. Size of circuit features in typical integrated circuits. ICs are typically placed on circuit boards (left figure) in the size range of ten centimeters. The dimensions of a typical IC are around a few centimeters (center figure). The minimum line widths of individual features in ICs (left figure) are currently well below 1 μm. With future technologies and advancing miniaturization, the dimensions are expected to decrease further. Left image: screen capture from KiCad EDA Software, center and right images: [1, 2]

because at the scale of microchips, various new interaction phenomena arising from the physical circuit layout need to be taken into account in the circuit design, such as signal delay and crosstalk in the connection lines between the active elements of the circuit. These non-ideal parasitics are typically added to the original circuit design by using an extraction tool to generate a per-unit-length-type RLCK circuit (a circuit containing resistances, inductances, capacitances, and mutual inductances) representation for the physical circuit board design. Depending on the level of precision and the connectivity in the circuit, the extraction generates thousands to millions of circuit elements that need to be added to the original designer-created circuit description (Fig. 1.2). This puts a heavy additional demand on the CPU and memory requirements for the verification simulation.

One solution to this problem is to use MOR. By accepting an error margin to the extracted RLCK model, the model is approximated such that only the most important characteristics of the parasitic phenomena are included in the model simulations, and less important factors are left out (Figs. 1.2 and 1.3). This simplifies the RLCK model to a more manageable size and speeds up the simulation considerably.

The reduction in system size is possible, in principle, because not all of the individual system characteristics generated by, e.g., the per-unit-length-type discretizations are typically of vital interest. For example, in a transmission line discretization — a non-ideal model of a short circuit —

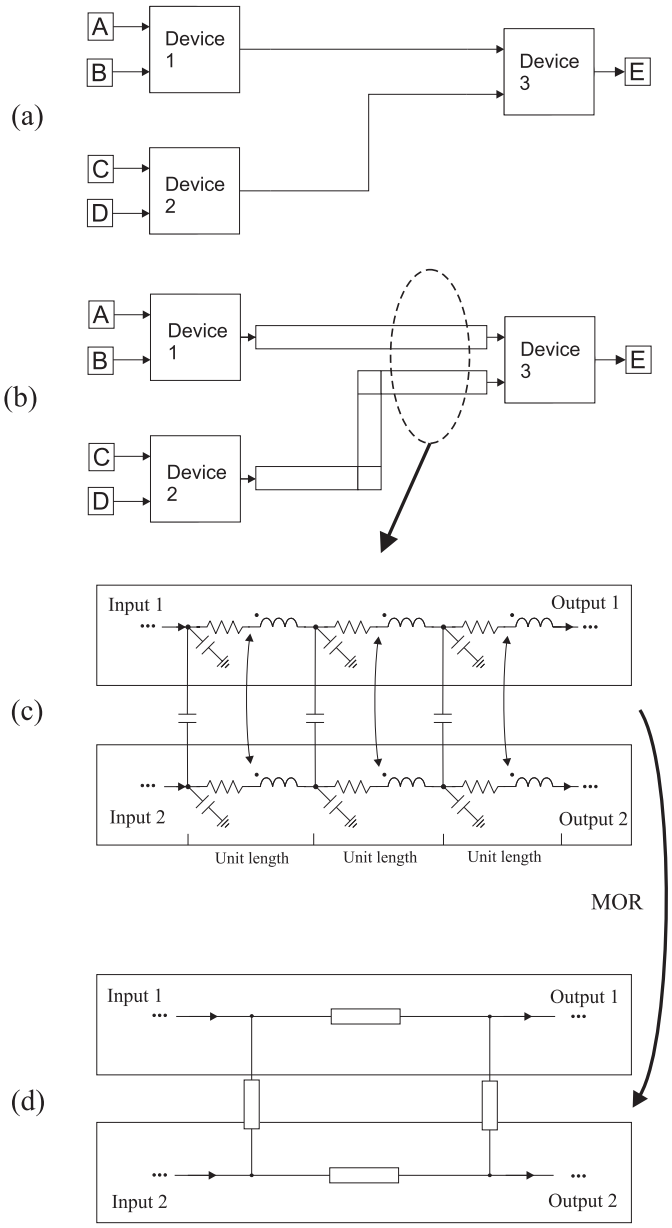


Figure 1.2. Parasitic elements and MOR. (a) Ideal design of a (part of a) circuit. (b) Non-ideal parasitic phenomena need to be taken into account when designing circuits with small physical size. This turns, e.g., short circuits between devices into lossy transmission lines. (c) In order to verify that the circuit works as intended, a typical approach is then to generate a per-unit-length-type discretization of the model for simulation purposes. (d) MOR can be used to approximate this discretization, resulting in a simpler model (shown as generic boxes) that focuses on the critical characteristics of the original model.

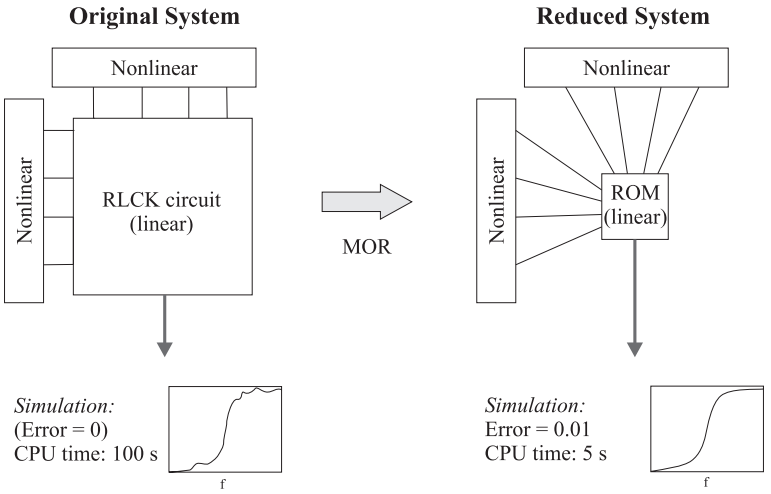


Figure 1.3. The concept of MOR: the RLCK circuit is approximated with a smaller model. This speeds up the simulation but generates error. Connections to other (e.g., nonlinear) parts of the circuit design are not affected.

the individual nodal voltages along the transmission line are reduceable, because a user is typically interested mainly in the input–output behavior of the model, i.e., of the voltages at the ends of the transmission line. Now, a simpler model can be devised by exploiting the idea that the model needs to provide only the relation between the two voltages.

This can be further illustrated in system-matrix terms, where the original system $\mathbf{A}\mathbf{x} = \mathbf{b}$ is reduced to $\tilde{\mathbf{A}}\tilde{\mathbf{x}} = \tilde{\mathbf{b}}$. If the reduced system-variable vector $\tilde{\mathbf{x}}$ contains only the unknowns for input and output ports, also the size of $\tilde{\mathbf{A}}$ and $\tilde{\mathbf{b}}$ can be reduced considerably, because the size of $\tilde{\mathbf{A}}$ is quadratically dependent on $\tilde{\mathbf{x}}$ (for minimum well-defined systems).

1.3 A short review of the MOR development in circuit theory

This sections gives a brief desciption of the development of MOR methods in circuit theory. A more detailed discussion on the topic can be found in one of the textbooks, e.g., [3, 4].

A typical target circuit for MOR is a linear RC circuit extraction of on-chip wiring [5]. More modern extraction tools (e.g., [6]) can also generate RLCK circuits, where the inductive effect is included in the circuit model. Thus, traditional MOR methods have been aimed mostly at the reduction of linear frequency independent RC and (more recently) RLCK circuits. With advancing technology, to achieve even more accurate verification simulations of the IC designs, the circuit models may need to be mod-

eled as frequency dependent $R(f)L(f)C(f)K(f)$ circuits [5]. Similarly, the development of MOR methods has to answer the problems generated by these representations. This is the specialized field of parameterized MOR (e.g., [7, 8]), which aims to create ROMs that can have multiple variable parameters. At the moment, however, even the more straightforward MOR of RLCK (or RC) circuits has still many open questions needing improvement in order to be used as a reliable and efficient tool in industrial scale circuit problems. To this end, the focus of this thesis is on the MOR of linear RLCK circuits.

Starting from the success of the asymptotic waveform evaluation (AWE) [9] in 1990, a large number of projection-based MOR methods have been proposed for the reduction of linear circuit systems. The AWE algorithm used the concept of moments to measure the accuracy of the reduced system compared to the original one. In essence, the method attempted to match a number of moments of the original system by using a Padé-like approximation resulting in a reduced-order model. However, the direct matching of high-order moments was shown to cause numerical unstability problems, and improvements to AWE were needed. An answer to overcome the unstability problem was to use implicit moment matching. The idea here was to project the original moment space onto an orthonormal Krylov subspace. The first such attempt was to use the Pade via Lanczos (PVL) [10] (1995) method, where the Lanczos process is used to generate the Krylov subspace. This approach was further extended, e.g., in [11, 12]. An alternative to the Lanczos was to use the Arnoldi process to generate the subspace [13]. Later, the Arnoldi process was used also in the passive reduced-order interconnect macromodeling algorithm (PRIMA) [14] (1998). Here, by using the Krylov-subspace vectors to obtain a projector matrix, a congruence transformation is used on the original system, which leads to a provably passive reduced-order model. The easy implementation and guaranteed passivity properties soon made PRIMA the typical general-purpose MOR method of choice. An important improvement to PRIMA was made in structure-preserving reduced-order interconnect macromodeling (SPRIM) [15] (2004) and second-order Arnoldi method for passive order reduction of RCS circuits (SAPOR) [16] (2004) by adding a structure-preserving feature to the process, thus also preserving the reciprocity of the system.

A different approach to MOR is by means of local nodal elimination. This was explored, e.g., in time constant equilibration reduction (TICER)

[18, 19] (1999) for RC circuits, which was extended to general RLC circuits in [20] (2003). The idea here is to locate those nodes in a circuit that contribute least to the input–output-behavior, approximate the local impact of the said nodes to neighboring nodes with low-order macromodels, and then remove the nodes. This allows the MOR to operate relatively locally, such that small reductions can be typically made to even those circuits that are difficult to reduce with other MOR methods. A more general idea of node reduction, using the Y–Δ transformation, was presented in [21] (2003).

A third major branch of MOR is to use control theory-based truncated balanced realization (TBR) methods, where the weaker state variables are truncated to achieve the reduced models [22]–[29] (starting from 1981).

The fourth approach to MOR is to use partitioning in the reduction process, which is the main topic of this thesis. This means dividing the original circuit into subcircuits or system matrices into submatrices and reducing each subcircuit/submatrix at a time. Partitioning in itself does not reduce the size of the system, which means that one of the above three other approaches must be used in conjuction with partitioning. However, by using partitioning in addition to otherwise limited MOR methods (such as low-order direct moment matching), the combined MOR method can overcome the shortcomings of the original approach.

The idea of using partitioning in MOR is not new. The first partitioning and macromodeling -based RC MOR method was presented by Liao and Dai in [30] (1995) with detailed algorithms for circuit partitioning and approximation by two possible macromodels. Another partitioning and macromodeling-based RC MOR method was presented in [31] (1999), where a single macromodel of second order was used. In ReduceR [32] (2010), the partitioning was done by matrix reorderings on a resistor network such that the partitions were replaced with single resistances. In this thesis, the partitioning-based MOR approach is discussed for the most part in conjunction with the direct macromodeling-based approximation approach similar to the original method by Liao and Dai. Other published partitioning-based MOR methods are, e.g.: partitioning and Krylov-subspace-based RLC MOR methods HiPRIME [33] (2002), BSMOR [34] (2005), hiePrimor [35] (2009), and BVOR [36] (2010). Most recently, a partitioning-based RC MOR method SparseRC [37] (2011) was presented, employing a sophisticated partitioning algorithm, extended moment matching projection, and using RLCSYN [38] to realize the ROM.

The above MOR approaches are applicable for linear circuit systems, as noted earlier. For the remainder of this thesis, it is further assumed that the circuits to be reduced are either strictly linear circuits or linear parts of nonlinear circuits that can be reduced separately with partitioning. MOR methods applicable directly to nonlinear problems also exist, where the reduceable part may contain also, e.g., diodes. Well-known MOR approaches aimed at these problems include proper orthogonal decomposition (POD) based methods and piece-wise linearization (PWL) based methods (e.g., [39] and [40], respectively).

2. Formulation of circuit equations

This section describes how a linear circuit network is typically represented as a system of equations. There are many systematic ways to formulate the circuit equations [41], e.g., nodal, loop, and cutset analysis, but the most common approach is to use the modified nodal analysis (MNA) [42].

The nodal analysis (NA) equations result from using Kirchhoff's current law (KCL) and branch constitutive equations between the nodes. Kirchhoff's current law states that the algebraic sum of all the currents incident at each node (i.e., coming from incident branches) is zero: $\Sigma i = 0$. If a current i in a branch flows towards a node, it is positive, and negative if it flows away from the node (and zero, if the branch is not incident to the node). The lumped circuit elements in a circuit network can then be modeled using Ohm's law for each branch connected to a node: e.g., $i = v/R$ or $i = \frac{\mathrm{d}q(v)}{\mathrm{d}t} = C\frac{\mathrm{d}v}{\mathrm{d}t}$, where v and q are the voltage and charge of a given node, R is the resistance and C is the capacitance of the branch, respectively.

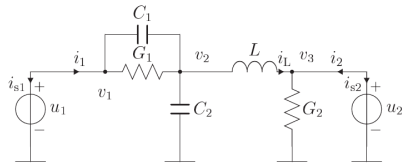
However, NA formulation can not be directly applied to circuit elements that can not be expressed in admittance form ($i = x \cdot v$), such as voltage sources or inductances. To this end, the MNA formulation extends the NA formulation by representing these elements using additional current variables. Thus, MNA formulation can be used to describe any circuit system in a systematic way.

In MOR, a convenient circuit representation concept is the use of admittance or impedance parameters. The idea here is to consider the circuit as an N-port (system with N external port nodes) and describe the total admittance or impedance between the port nodes, only. The aim of typical MOR methods is then to try to keep the admittance or impedance parameters the same before and after circuit reduction, while the overall circuit equation system may be greatly altered.

To obtain the admittance or impedance parameters for the N-port, the circuit is excited with voltage or current sources placed at the port nodes. These new sources are used to generate the admittance or impedance parameters, only, and are not left in the final reduced circuit. Since the reduction algorithms discussed in this thesis consider only the linear (RLCK) parts of the circuit, the original circuit may contain any combination of original voltage and/or current sources. The original sources are left out from the MOR and returned to the (ports of the) reduced circuit in the final steps of the MOR process.

It is worth noticing that the calculation of these parameters results in a set of slightly different circuit equations depending on the excitation. The differences are important for MOR methods because they translate to different matrix structures, which in turn may be an asset or a hindrance to the MOR method. Depending on the circuit topology, these may also have implications for system stability [PV].

2.1 Voltage excitation and y-parameters



$$\left[\begin{array}{ccc|ccc} C_1 & -C_1 & 0 & 0 & 0 & 0 \\ -C_1 & C_1+C_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & L_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{array}\right] \left[\begin{array}{c} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{i}_L \\ \dot{i}_{s1} \\ \dot{i}_{s2} \end{array}\right] = - \left[\begin{array}{ccc|ccc} G_1 & -G_1 & 0 & 0 & 1 & 0 \\ -G_1 & G_1 & 0 & 1 & 0 & 0 \\ 0 & 0 & G_2 & -1 & 0 & 1 \\ \hline 0 & -1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \end{array}\right] \left[\begin{array}{c} v_1 \\ v_2 \\ v_3 \\ i_L \\ i_{s1} \\ i_{s2} \end{array}\right] + \left[\begin{array}{cc} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & -1 \end{array}\right] \left[\begin{array}{c} u_1 \\ u_2 \end{array}\right]$$

$$\mathbf{C} \qquad \dot{\mathbf{x}}_n \quad = \qquad -\mathbf{G} \qquad \mathbf{x}_n \quad + \quad \mathbf{B} \qquad \mathbf{u}_N$$

$$\left[\begin{array}{c} i_1 \\ i_2 \end{array}\right] = \left[\begin{array}{cccccc} 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 \end{array}\right] \mathbf{x}_n = \mathbf{L}^T \mathbf{x}_n$$

Figure 2.1. Construction of the MNA matrices for y-parameters from a two-port RLC circuit example.

The admittance parameters (y-parameters) are derived by using voltage sources at the input and output ports to excite the circuit, as shown in Fig. 2.1. The time-domain MNA circuit equations for a linear N-port RLC

circuit can be expressed as [14]

$$\begin{cases} \mathbf{C}\dfrac{\mathrm{d}\mathbf{x}_n(t)}{\mathrm{d}t} = -\mathbf{G}\mathbf{x}_n(t) + \mathbf{B}\mathbf{u}_N(t), \\ \mathbf{i}_N(t) = \mathbf{L}^{\mathrm{T}}\mathbf{x}_n(t), \end{cases} \tag{2.1}$$

where $\mathbf{C}$ and $\mathbf{G}$ are the susceptance and conductance matrices, respectively, and $\mathbf{x}_n$, $\mathbf{u}_N$, and $\mathbf{i}_N$ denote the MNA variables (nodal voltages and branch currents of inductances and voltage sources), port voltages, and port currents, respectively. Here, $\mathbf{B} = \mathbf{L}$ is a selector matrix consisting of ones, minus ones, and zeros.

The matrices $\mathbf{C}$ and $\mathbf{G}$ are positive semidefinite and have a structure:

$$\mathbf{C} \equiv \begin{bmatrix} \mathbf{Q} & \mathbf{0} \\ \mathbf{0} & \mathbf{H} \end{bmatrix}, \mathbf{G} \equiv \begin{bmatrix} \mathbf{N} & \mathbf{E} \\ -\mathbf{E}^{\mathrm{T}} & \mathbf{0} \end{bmatrix}, \mathbf{x}_n \equiv \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix}, \tag{2.2}$$

where $\mathbf{Q}$, $\mathbf{H}$, and $\mathbf{N}$, are the matrices containing the stamps for capacitances, inductances, and resistances, respectively; $\mathbf{E}$ consists of ones, minus ones, and zeros, which represent the additional incidence stamps for branch currents and nodal voltages generated for the MNA equations; and the vector $\mathbf{x}_n$ contains the nodal voltages, $\mathbf{v}$, and branch currents, $\mathbf{i}$, for inductances and voltage sources. For RLC circuits, the dimension of the $\mathbf{C}$ and $\mathbf{G}$ matrix is thus $n \times n$, with $n = n_{\mathrm{i}} + n_{\mathrm{e}} + n_L + N$, where n_{i}, n_{e}, n_L, and N are the number of internal nodes, external nodes, inductances, and ports, respectively (typically, $N = n_{\mathrm{e}}$, when ports are between a node and ground). By taking the Laplace transformation of (2.1), solving for the port currents, and defining

$$\mathbf{A} \equiv -\mathbf{G}^{-1}\mathbf{C}, \quad \mathbf{R} \equiv \mathbf{G}^{-1}\mathbf{B}, \tag{2.3}$$

the y-parameter matrix can be written as

$$\mathbf{Y}(s) = \mathbf{L}^{\mathrm{T}}(\mathbf{I} - s\mathbf{A})^{-1}\mathbf{R}, \tag{2.4}$$

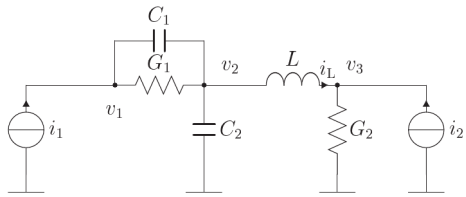
where $\mathbf{I}$ is the $n \times n$ identity matrix. The term $(\mathbf{I} - s\mathbf{A})^{-1}$ can be expanded into a Neumann series to obtain the block moments of the y-parameters

$$\mathbf{Y}(s) = \mathbf{M}_0 + \mathbf{M}_1 s + \mathbf{M}_2 s^2 + \cdots, \tag{2.5}$$

where

$$\mathbf{M}_i = \mathbf{L}^{\mathrm{T}}\mathbf{A}^i\mathbf{R}, \tag{2.6}$$

having the dimension $N \times N$. Note that the DC behavior is given by $\mathbf{Y}(0) = \mathbf{M}_0$.



$$\begin{bmatrix} C_1 & -C_1 & 0 & 0 \\ -C_1 & C_1+C_2 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & L_1 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{i}_\mathrm{L} \end{bmatrix} = - \begin{bmatrix} G_1 & -G_1 & 0 & 0 \\ -G_1 & G_1 & 0 & 1 \\ 0 & 0 & G_2 & -1 \\ \hline 0 & -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_\mathrm{L} \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

$$\mathbf{C} \qquad \dot{\mathbf{x}}_n \quad = \qquad -\mathbf{G} \qquad \mathbf{x}_n \quad + \quad \mathbf{B} \qquad \mathbf{i}_N$$

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \mathbf{x}_n = \mathbf{L}^T \mathbf{x}_n$$

Figure 2.2. Construction of the MNA matrices for z-parameters from a two-port RLC circuit example.

2.2 Current excitation and z-parameters

The impedance parameters (z-parameters) are derived by using current sources at the ports to excite the circuit, as shown in Fig. 2.2. In a similar fashion as in the derivation of y-parameters in the previous section, the MNA equations for a linear N-port RLC circuit can be expressed:

$$\begin{cases} \mathbf{C}\dfrac{\mathrm{d}\mathbf{x}_n(t)}{\mathrm{d}t} = -\mathbf{G}\mathbf{x}_n(t) + \mathbf{B}\mathbf{i}_N(t), \\ \mathbf{u}_N(t) = \mathbf{L}^{\mathrm{T}}\mathbf{x}_n(t), \end{cases} \tag{2.7}$$

where $\mathbf{C}$ and $\mathbf{G}$ are the susceptance and conductance matrices, respectively; $\mathbf{x}_n$, $\mathbf{u}_N$, and $\mathbf{i}_N$ denote the MNA variables (nodal voltages, $\mathbf{v}$, and branch currents of inductances $\mathbf{i}$), port voltages, and port currents, respectively; matrix $\mathbf{B} = \mathbf{L}$ is a selector matrix consisting of ones, minus ones, and zeros; and the vector $\mathbf{x}_n$ contains the nodal voltages, $\mathbf{v}$, and branch currents, $\mathbf{i}$, for inductances. For RLC circuits, the dimension of the $\mathbf{C}$ and $\mathbf{G}$ matrix is thus $n \times n$, with $n = n_\mathrm{i} + n_\mathrm{e} + n_L$.

Taking the Laplace transformation of (2.7) and solving for the port voltages, the z-parameter matrix is given as

$$\mathbf{Z}(s) = \mathbf{L}^{\mathrm{T}}(\mathbf{G} + s\mathbf{C})^{-1}\mathbf{B}. \tag{2.8}$$

This can be expanded to a series similarly to (2.5) in order to obtain the block moments for $\mathbf{Z}(s)$.

Noting that the matrices have a block structure,

$$\begin{cases} \left(s \begin{bmatrix} \mathbf{C}_{11} & \mathbf{0} \\ \mathbf{0} & \mathbf{L}_{22} \end{bmatrix} + \begin{bmatrix} \mathbf{G}_{11} & \mathbf{G}_{12}^{\mathrm{T}} \\ -\mathbf{G}_{21} & \mathbf{0} \end{bmatrix} \right) \begin{bmatrix} \mathbf{v}(s) \\ \mathbf{i}(s) \end{bmatrix} = \begin{bmatrix} \mathbf{B}_1 \\ \mathbf{0} \end{bmatrix} \mathbf{i}_N(s), \\ \mathbf{u}_N(s) = \begin{bmatrix} \mathbf{B}_1^{\mathrm{T}} & \mathbf{0}^{\mathrm{T}} \end{bmatrix} \begin{bmatrix} \mathbf{v}(s) \\ \mathbf{i}(s) \end{bmatrix}, \end{cases} \tag{2.9}$$

and eliminating the branch currents, the system (2.7) can also be expressed in the second-order form (noting that $\mathbf{G}_{21} = \mathbf{G}_{12}$):

$$\Rightarrow \begin{cases} (s\mathbf{C}_{11} + \mathbf{G}_{11} + \dfrac{1}{s}\mathbf{G}_{12}^{\mathrm{T}}\mathbf{L}_{22}^{-1}\mathbf{G}_{12})\mathbf{v}(s) = \mathbf{B}_1\mathbf{i}_N(s), \\ \mathbf{u}_N(s) = \mathbf{B}_1^{\mathrm{T}}\mathbf{v}(s), \end{cases} \tag{2.10}$$

$$\Rightarrow \begin{cases} (s\mathbf{C}_{11} + \mathbf{G}_{11} + \dfrac{1}{s}\mathbf{\Gamma})\mathbf{v}(s) = \mathbf{B}_1\mathbf{i}_N(s), \\ \mathbf{u}_N(s) = \mathbf{B}_1^{\mathrm{T}}\mathbf{v}(s), \end{cases} \tag{2.11}$$

where $\mathbf{\Gamma} \equiv \mathbf{G}_{12}^{\mathrm{T}}\mathbf{L}_{22}^{-1}\mathbf{G}_{12}$. Similarly, the z-parameters can be expressed using the second-order form as

$$\mathbf{Z}(s) = \mathbf{B}_1^{\mathrm{T}}(s\mathbf{C}_{11} + \mathbf{G}_{11} + \frac{1}{s}\mathbf{G}_{12}^{\mathrm{T}}\mathbf{L}_{22}^{-1}\mathbf{G}_{12})^{-1}\mathbf{B}_1. \tag{2.12}$$

3. Conventional MOR approaches

This section describes two projection-based MOR methods, PRIMA and SPRIM, and a nodal elimination-based method TICER in more detail. These methods have been used for comparison purposes in the publications of this thesis.

3.1 Krylov subspace approach

The objective of MOR is to present the system matrices in a smaller form. In projection-based methods, this is done by projecting the system equations onto a smaller subspace that spans the same space as the block moments of the original system, thus reducing the dimension of the system.

The passive reduced-order interconnect macromodeling algorithm (PRIMA) [14] is a classical example of Krylov subspace-based MOR. The method uses the block-Arnoldi iteration as a numerically stable method for generating the Krylov subspace. The generated orthonormal projection matrix $\mathbf{X}$ satisfies the following for the y-parameter circuit equation formulation:

$$\mathrm{colsp}(\mathbf{R}, \mathbf{AR}, \mathbf{A}^2\mathbf{R}, ..., \mathbf{A}^k\mathbf{R}) = \mathrm{Kr}(\mathbf{A}, \mathbf{R}, q), \tag{3.1}$$

where $\mathbf{A}$ and $\mathbf{R}$ are defined as (2.3), and

$$\mathrm{colsp}(\mathbf{X}) = \mathrm{Kr}(\mathbf{A}, \mathbf{R}, q), \quad k = \lfloor q/N \rfloor. \tag{3.2}$$

Here, the order of reduction $q = N \times k$ is the size of the reduced state vector, and k is the number of the block moments matched in the Krylov subspace.

The projection matrix is then used to perform a congruence transformation on the original system matrices of (2.1). This transforms the original

circuit equation matrices into smaller, reduced matrices:

$$\begin{aligned} \tilde{\mathbf{C}} &= \mathbf{X}^{\mathrm{T}}\mathbf{C}\mathbf{X}, \quad \tilde{\mathbf{G}} = \mathbf{X}^{\mathrm{T}}\mathbf{G}\mathbf{X}, \\ \tilde{\mathbf{B}} &= \mathbf{X}^{\mathrm{T}}\mathbf{B}. \end{aligned} \tag{3.3}$$

The structure-preserving reduced-order interconnect macromodeling (SPRIM) [15] improves the PRIMA method by preserving the block structure of the original matrices in the reduced matrices. To do this, SPRIM uses z-parameter formulation (2.7) for the circuit equations (in order to have a simpler matrix structure to start with). After constructing the projection matrix $\mathbf{X}$ similar to PRIMA, SPRIM partitions the matrix into two parts and a new projection matrix, $\tilde{\mathbf{X}}$, is formed, following the block-structure of (2.9):

$$\mathbf{X} = \begin{bmatrix} \mathbf{X}_1 \\ \mathbf{X}_2 \end{bmatrix} \rightarrow \tilde{\mathbf{X}} = \begin{bmatrix} \mathbf{X}_1 & 0 \\ 0 & \mathbf{X}_2 \end{bmatrix}. \tag{3.4}$$

The system matrices are reduced with congruence transformations, now resulting in

$$\begin{aligned} \tilde{\mathbf{C}}_{11} &= \mathbf{X}_1^{\mathrm{T}}\mathbf{C}_{11}\mathbf{X}_1, \quad \tilde{\mathbf{L}}_{22} = \mathbf{X}_2^{\mathrm{T}}\mathbf{L}_{22}\mathbf{X}_2, \\ \tilde{\mathbf{G}}_{11} &= \mathbf{X}_1^{\mathrm{T}}\mathbf{G}_{11}\mathbf{X}_1, \quad \tilde{\mathbf{G}}_{12} = \mathbf{X}_2^{\mathrm{T}}\mathbf{G}_{12}\mathbf{X}_1, \\ \tilde{\mathbf{B}}_1 &= \mathbf{X}_1^{\mathrm{T}}\mathbf{B}_1. \end{aligned} \tag{3.5}$$

The reduced-order model $\tilde{\mathbf{Z}}(s)$ is in second-order form (2.12)

$$\tilde{\mathbf{Z}}(s) = \tilde{\mathbf{B}}_1^{\mathrm{T}}(s\tilde{\mathbf{C}}_{11} + \tilde{\mathbf{G}}_{11} + \frac{1}{s}\tilde{\mathbf{G}}_{12}^{\mathrm{T}}\tilde{\mathbf{L}}_{22}^{-1}\tilde{\mathbf{G}}_{12})^{-1}\tilde{\mathbf{B}}_1. \tag{3.6}$$

SPRIM matches even twice as many moments as PRIMA with approximately the same computational work [15]. However, the most important benefit of SPRIM is that it preserves also the reciprocity of the original RLCK circuit. This makes it possible to synthesize the ROM as an RLC circuit using RLCSYN [38].

3.2 Nodal elimination approach

The idea of nodal elimination in MOR is to apply MOR at a very local level: one node is considered at a time, and it's impact to the overall behavior of the circuit is analyzed. The node under inspection is then removed from the circuit, and new elements are generated between neighboring nodes to offset the removal of the node.

The time constant equilibration reduction (TICER) [18] is a locally operating nodal elimination-based RC MOR method. The method is based on the assumption that a node with a small time constant, T_K, is regarded

as a less important node in computing propagation delays — and thus transient behavior — and can be removed. The elements connected to this node are also removed, and new elements are added to the neighboring nodes to maintain approximately the same electrical characteristics of the circuit.

Figure 3.1 presents the rules for generating new elements for each eliminated node. The element values are obtained by approximating the contribution of the two branches iK and jK by the first two terms of the expanded power series, and approximating that $|sC_K| \ll |G_K|$, where $G_K = \sum_{i=0}^{n-1} g_{iK}$ and $C_K = \sum_{i=0}^{n-1} c_{iK}$ and n is the number of branches connected to node K.

To eliminate a node K from a circuit, first all resistances and capacitances connecting other nodes to K are removed. Then, if nodes i and j were connected to K through conductances g_{iK} and g_{jK}, a conductance $g_{iK}g_{jK}/G_K$ is inserted from i to j. If node i had a capacitance c_{iK} to K and node j a conductance g_{jK} to K, a capacitance $c_{iK}g_{jK}/G_K$ is inserted between i and j, instead. Similar equations can also be constructed if $|sC_K| \gg |G_K|$, but this is a rare case in most typical interconnect circuit applications.

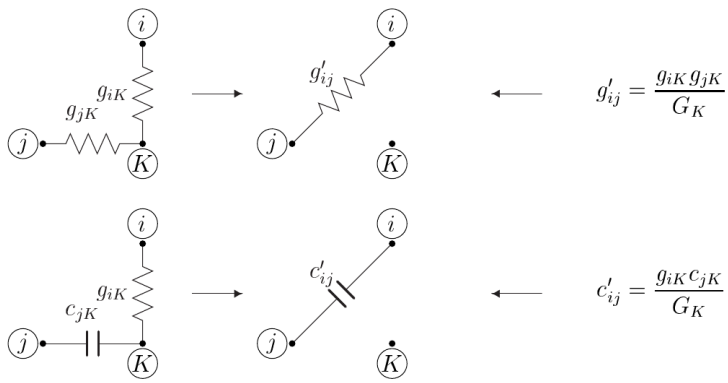


Figure 3.1. Rules for eliminating a node in TICER.

4. Partitioning and macromodeling -based MOR

This chapter introduces the concept of partitioning and macromodeling -based MOR, which is the main MOR approach discussed in this thesis. While some MOR methods have employed the approach, notably the Liao and Dai method, it has not been as well known or widely used as the projection or nodal elimination-based approaches described in the previous chapter. Although the partitioning and macromodeling -based approach has its own limitations, it has also some significant benefits in comparison to the previous two approaches [PIV]: Thanks to partitioning and low-order matching, the reduction can be realized with positive-valued elements, which the Krylov-subspace methods are (currently) unable to provide. On the other hand, elimination-based methods are either computationally intensive or require that the original circuit has a suitable capacitance-to-resistance element ratio. In addition to the characteristic benefits of the partitioning and macromodeling -based approach, this thesis aims to show that the presented methods are otherwise well comparable in reduction efficiency to previously presented methods using alternative approaches.

4.1 Background

The basic idea of the partitioning and macromodeling -based approach is to first use partitioning to divide the circuit into small parts. Due to their small size, these small parts can then be approximated accurately using relatively simple approximations (typically of zeroth, first, or second order). In turn, thanks to the simple nature of these approximations, they can then be realized using lumped element R/RC/RL/RLC macromodels that have positive-valued elements.

The approach can be conceptually divided into the four main steps de-

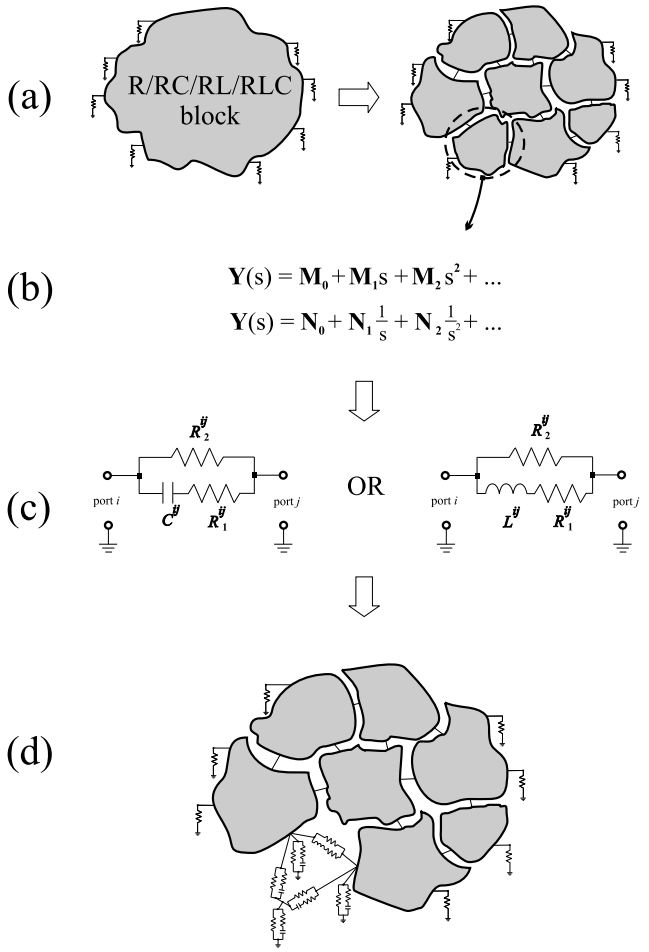


Figure 4.1. Partitioning and macromodeling -based approach as presented in [PIV]: (1) The circuit is partitioned into subcircuits. (2) For each subcircuit, the y-parameter moments are calculated. (3) The macromodels of each connection for each partition are synthesized using one or more moments. The exact structure of the macromodel depends on the MOR method used. (4) The generated macromodels replace the original partition and the process is repeated for each subcircuit. Figure reprinted from [PIV] ©IEEE 2011.

picted in Fig. 4.1: (a) The circuit is partitioned into N-port subcircuits. (b) The first few y-parameter moments are calculated explicitly for each subcircuit. (c) From these, the element values for a chosen macromodel are calculated by matching the y-parameter moments with the coefficients of the Taylor expansion of the macromodel transfer function. (d) After generating the macromodels for each subcircuit, the subcircuits (and macromodels) are recombined together.

The size of the subcircuits generated by partitioning (measured in the number of elements) is critical: if the subcircuit is too large, the low-order macromodel used is not accurate enough to model the partition and precision is lost. On the other hand, if the subcircuit is too small, the replacing macromodel is of the same size as the original subcircuit and no actual reduction takes place.

By using partitioning to match small sections of the original circuit with low-order approximations, the possible ill-conditioning and numerical stability problems related to direct high-order moment-matching approaches [9] are avoided. When the subcircuits are combined together, the order of the total reduced circuit is much higher, however, and better accuracy can be obtained depending on the number of subcircuits (and macromodels) used between the original external port nodes.

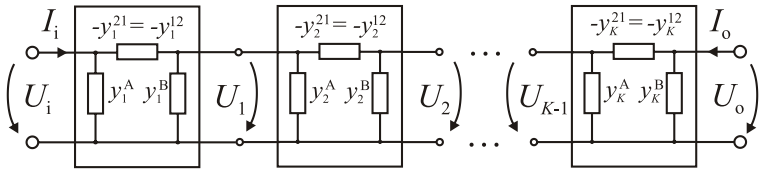


Figure 4.2. A cascaded reciprocal 2-port system described with y-parameters. In the figure, $y_k^\mathrm{A} = y_k^{11} + y_k^{12}$ and $y_k^\mathrm{B} = y_k^{22} + y_k^{12}$, where $k = 1, \ldots, K$. Figure reprinted from [PIV] ©IEEE 2011.

The order of a linear (RLC) circuit is the same as the number of linearly independent first-order differential equations needed to describe it [41]. In an RLC circuit, these equations are generated by the reactive elements, i.e., inductances and capacitances, and thus, conversely, the order of the network is the same as the number of independent reactive elements.

To illustrate the final order of the reduced circuit, a cascaded two-port system is shown in Fig. 4.2. This could be generated, e.g., from a two-port network that is partitioned into two-port blocks and reduced by a partitioning-based MOR method. Here, each y-parameter element may

contain linearly independent reactive elements that increase the order of the circuit. For a transfer function $y^{21}(s)$ for the total cascaded system, the terminal loads y_1^A and y_K^B are ignored, and the upper limit of the order of the (reduced) circuit is thus

$$q_{\mathrm{red}} = (K \times 3 - 2) \times q_{\mathrm{p}}, \tag{4.1}$$

where K is the number of subcircuits between the two external ports and q_{p} is the order of one y-parameter element in a partition (in this thesis $q_{\mathrm{p}} = 1$, typically). For simplicity, it was here further assumed that all the y-parameter elements are of the same order.

Although (4.1) applies explicitly for a two-port system, only, it is obvious that the order of the circuit increases in a similar manner when the number of cascaded blocks (subcircuits) is increased in an N-port system. Thus, when the circuit is partitioned into small subcircuits, despite the low-order approximation per partition, high accuracy for the total reduction can be reached, depending on the number of subcircuits used: if more precise reduction is required, the original circuit may be partitioned into even smaller subcircuits for a higher-order total reduction.

Since a macromodel is generated between each pair of ports and ground, the reduction leads to a full block matrix between the ports. However, due to partitioning and generation of new external nodes for each partition (which are combined into internal nodes when the partitions are recombined after MOR), the reduction is capable of retaining the block structure of the original system; for transmission line -type circuits, e.g., this results in a sparse, block-diagonal system matrix, where each block corresponds to one partition (see Fig. 5.1).

Finally, the partitioning in itself has also several other major advantages in addition those mentioned above that benefit the macromodeling -based MOR [PIII, PIV]. By using partitioning, the original problem can be naturally divided into smaller parts that can be processed separately. This provides a reduction algorithm numerous benefits, such as economical memory use, natural parallel processing, and facilitated port handling. In case of very large circuits (e.g., more than 10^8 elements), processing a circuit without prior partitioning may be impossible for many computers due to limiting memory resources.

4.2 Method limitations

This section describes the general limitations of the partitioning and macromodeling-based MOR.

4.2.1 Accuracy with complex circuits

As noted in the previous section, the original circuit is matched with a low-order approximation at each partition. This means that the order of approximation is low also for the total reduction. Thus, the circuit needs to be partitioned into small enough partitions such that each of the partitions can be approximated with sufficient accuracy using the low-order approximation.

For an intuitive example of how a low-order approximation can still reach good accuracy even in the case of a high-order original circuit, consider a circuit with α R/L/C/K elements. If the circuit is partitioned into α partitions, each partition can be modeled error-free with a first-order representation, since each partition contains only a single element. When the number of elements per partition increases, a low-order model begins to approximate the original circuit generating also error.

In general, the partitioning and macromodeling-based MOR works best with such original circuits that have a large number of similar circuit-element blocks of relatively equal importance and complexity, such as typical per-unit-length interconnect line discretizations. If this is not the case, additional heuristics should be used such that the partitioning differs in the size of the partitions.

If, for some reason, the circuit can not be partitioned into small enough partitions such that the low-order approximation captures the essential characteristics of that partition, the MOR error increases dramatically. This is for the most part still an open question for the partitioning and macromodeling MOR, and in these cases the two other MOR approaches discussed in the previous chapter might well result in better results.

4.2.2 Circuit density and the number of port nodes

As noted in the previous section, the partitioning and macromodeling-based method generates a dense block of elements between each pair of ports in a partition. Thus, in the case of a circuit with few internal nodes between each port, the reduction is less efficient. Using partitioning to

reduce the number of ports per subcircuit can help ([30] and see Sec. 5.2), but in the worst case this may result in more elements after MOR than before.

Similarly, if a dense mesh is partitioned into subcircuits without augmentative methods [PVI–PVIII], the resulting subcircuits typically have a high number of port nodes, which often have a major negative effect on the reduction efficiency (see Sec. 5.3).

4.3 The Liao and Dai method

The Liao and Dai method [30] is an example of the partitioning and macromodeling -based MOR approach. The method begins by describing the circuit with scattering parameters (S-parameters): each circuit element and multiport circuit node is described in S-parameter terms. Next, these elements are combined into larger entities using a set of rules in order to minimize the number of external ports in each of the resulting S-parameter subcomponent. This generation of suitably sized subcomponents with a minimum number of external ports results in circuit partitioning.

At each step of building the subcomponents, the S-parameters are updated by calculating new S-parameters for each newly merged subcomponent, and the S-parameter equations describing the subcomponents are also truncated to the first two low-order terms. After the partitioning is completed, the S-parameters are converted into y-parameters using a semisymbolic analysis. The y-parameters are then used to realize of the subcomponents with RC-macromodels.

For an N-port, the admittance between the ith port and ground is given by the sum of the ith row (or column) of its Y matrix, $\mathbf{Y}(s)$. The admittance connecting ports i and j is $-y_{ij}$. Thus, the circuit synthesis problem amounts to synthesizing admittances between a port and ground and between pairs of ports with lumped R and C elements. Once the block moments $\mathbf{M}_0$ and $\mathbf{M}_1$ have been calculated (explicitly) using (2.6) for the N-port, each element of $\mathbf{Y}(s)$ can be expressed with a series as

$$y_{ij} = m_0^{ij} + m_1^{ij} s + \ldots \approx m_0^{ij} + m_1^{ij} s. \tag{4.2}$$

The Liao and Dai method introduces three macromodels, presented in Figs. 4.3 and 4.4. Depending on the value of m_1^{ij}, different macromodel is chosen between ports i and j to ensure that the synthesized elements are of positive value: The T circuit in Fig. 4.3(a) may be used if $m_1^{ij} \geq 0$. If m_1^{ij}

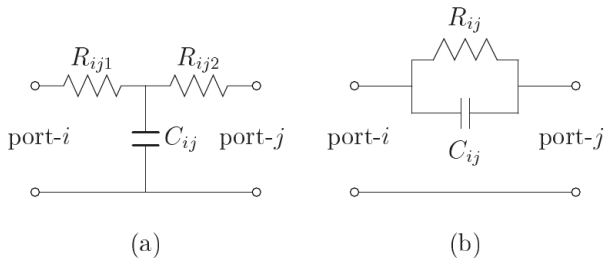


Figure 4.3. The Liao and Dai method macromodels for realizations between ports i and j.

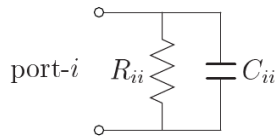


Figure 4.4. The Liao and Dai method macromodel for port nodes.

is negative, Fig. 4.3(b) must be used instead. In addition, the terminal macromodel, shown in Fig. 4.4, is used at each port node of the N-port. The element values for the macromodels are:

$$\begin{cases} R_{ij1} = \dfrac{-\sqrt{m_1^{jj}}}{m_0^{ij}(\sqrt{m_1^{ii}} + \sqrt{m_1^{jj}})}, \\ R_{ij2} = \dfrac{-\sqrt{m_1^{ii}}}{m_0^{ij}(\sqrt{m_1^{ii}} + \sqrt{m_1^{jj}})}, \\ C_{ij} = \dfrac{m_1^{ij}(\sqrt{m_1^{ii}} + \sqrt{m_1^{jj}})^2}{\sqrt{m_1^{ii} m_1^{jj}}}, \end{cases} \tag{4.3}$$

for Fig. 4.3(a),

$$\begin{aligned} R_{ij} &= -\frac{1}{m_0^{ij}}, \\ C_{ij} &= -m_1^{ij}, \end{aligned} \tag{4.4}$$

for Fig. 4.3(b), and

$$\begin{aligned} &R_{ii} = \frac{1}{m_0^{i0}}, \\ &C_{ii} = m_1^{i0}, \quad \text{where} \\ &y_{i0} = y_{ii} - \sum_{j=1(j\neq i)}^{N} y_{ij} = m_0^{i0} + m_1^{i0} s + ... \end{aligned} \tag{4.5}$$

for Fig. 4.4. These values are obtained by expanding the y-parameters of the macromodels into Taylor series and matching the series then with

(4.2). For a more detailed discussion on the matching of macromodel and block moments, see [PIV].

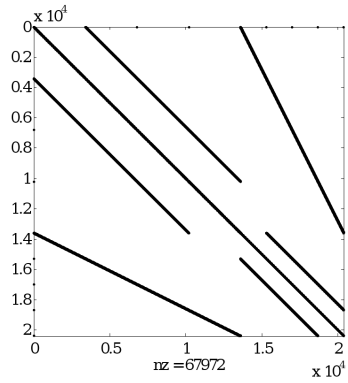
5. Current problems in MOR

This chapter describes some important problems and open questions in MOR of linear RLCK circuits. The publications of this thesis attempt to solve these problems in the special case of RLCK interconnect circuits by using the partitioning and macromodeling -based MOR approach. A more general overview of the current challenges in industrial MOR can be found in [43].

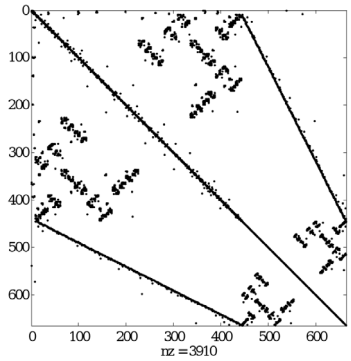
5.1 MOR efficiency with large circuits

The projection-based Krylov methods have two major problems [17]: firstly, the transformation matrix $\mathbf{X}$ is a full matrix that requires prohibitive amounts of memory with large-scale circuits, and secondly, the resulting ROMs of these methods are full matrices which makes the approximation properties of these ROMs suboptimal, because the original circuits are typically very sparse.

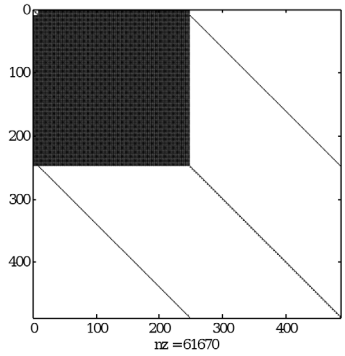
One of the motivations to use partitioning in MOR is to obtain block-sparse ROMs. In an optimal case, partitioning can retain the sparsity of the original system and still produce efficient reduction results. Figure 5.1 shows an example of a system matrix comparison between original and reduced circuits for partitioning-based [PVIII] and projection-based (SPRIM using RLCSYN realization) reduction. Here, the projection-based method generated reduced matrices that were highly inefficient due to full matrix block structures, and the simulation time was worse after reduction than for the original circuit.



(a)



(b)



(c)

Figure 5.1. Comparison of original and reduced system matrices of circuit equations $\mathbf{G} + s\mathbf{C}$: (a) original RLCK interconnect circuit, (b) partitioning-based reduction, (c) projection-based reduction. Here, the reduced circuits had the same level of accuracy (measured as the error in transient analysis). Simulation times for the circuits were: original 51.7 s, partitioning-based ROM 1.8 s, and projection-based ROM 89.8 s. For original circuit statistics, see `ckt2` in [PVIII].

5.2 Circuits with many ports

Projection-based MOR methods typically have problems with circuits with many external (port) nodes. In general, such nodes can not be reduced, because they connect the circuit to other parts of the design, such as nonlinear components, and the behavior at each port needs to be communicated somehow to each other port. The size of the projection matrix $\mathbf{X}$ is quadraticly dependent on n_{e}, and thus, the memory requirements for MOR increase rapidly if the circuit has many external nodes. Similarly, the size of resulting ROM increases with increased $\mathbf{X}$, which decreses the efficiency of the MOR considerably.

With partitioning, the number of port nodes per each partition, $n_{\mathrm{e,p}}$, can be reduced in certain cases. The goal here is to find partitions that have $n_{\mathrm{e,p}}$ much lower than the total n_{e} of the original circuit [30, 37]. Ideally, in these cases, partitioning may achieve to find a partitioning where the external nodes are divided between the partitions evenly, such that $n_{\mathrm{e,p}} \approx n_{\mathrm{e}}/p$, where p is the number of partitions. This way, the memory requirements (per each partition) remain low, and the efficiency of the MOR can be retained.

5.3 Densely coupled circuits

Nodal elimination and partitioning-based MOR approaches have inherent problems to reduce a circuit if the original circuit contains relatively dense mesh-like structures, such as in Fig. 5.2.

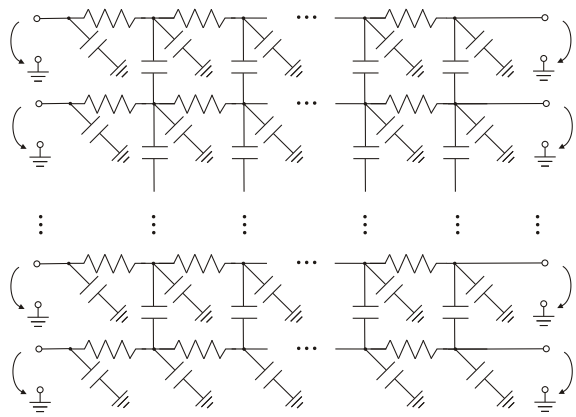


Figure 5.2. An RC mesh circuit.

With partitioning and macromodeling -based methods the problem is that if a dense mesh is partitioned into subcircuits, the resulting subcircuits typically have a high number of port nodes that connect one subcircuit to other subcircuits. As noted in the previous section, MOR methods can not reduce these nodes easily, and with large number of ports the resulting ROM becomes large and inefficient. On the other hand, if larger partitions are used (to improve the n_{e}-to-n_{i} ratio per partition), the low-order approximation may not be enough for accurate approximation. In this case, the reduction becomes difficult, and in the worst case, impossible without augmentative methods [PVI–PVIII]. Meshes consisting of mostly resistances can typically still be reduced efficiently, due to their simple moment characteristics.

With nodal-elimination-based approaches the problem is that if a node has more than three connecting elements, elimination of that node generates more elements to the reduced circuit than in the original circuit. Although the number of nodes could be reduced in this fashion, the resulting reduced circuit has more elements than the original, and the simulation time may be even longer than that of the original circuit. With densely coupled circuits, the nodes have typically a high number of connected elements, and thus, nodal-elimination is inherently inefficent (if capable at all) in reducing such circuits.

5.4 Realizability of MOR

One often overlooked issue in the development of new MOR methods is the realizability of the reduced-order models. If a potential MOR method produces only a reduced mathematical model of transfer function or state equations, instead of realizable circuit netlists, all downstream analysis and simulation tools need to be modified to handle these representations. Also the level of realizability is of essence; the macromodel realizations for MOR are well studied in [44] but contain voltage-controlled current/charge sources in addition to standard RLCK elements. Depending on the design flow, this may severely limit the utility and usability of MOR [31, 38]. Ideally, the reduced circuit is in the same form after the reduction as the original circuit: for an original RLCK circuit (with positive-valued elements), the reduced circuit should contain only RLCK elements (of positive value).

Realizable RLCK-in–RLCK-out (R/L/C/K-in–R/L/C/K-out) reduction meth-

ods have been proposed, some of which are: a nodal-elimination-based TICER [18] for RC circuits, an RLC extension to TICER [20], more general RLC node reduction using Y–Δ transformation [21], a moment-matching driving point RLC realization using macromodels (but not partitioning) [45], a partitioning and macromodeling -based RC MOR [30], [31], [46], [PI], a partitioning and macromodel-based RL MOR [PII] and a partitioning and macromodeling -based RLC MOR [PIV], with mutual inductance extension [PVI]. In [32], a partitioning-based realizable MOR for resistor networks is presented. Finally, RLCSYN [38] presents an RC(L) realization algorithm for structure-preserving MOR methods such as SPRIM. However, unlike the other methods listed above, the RC(L) elements generated by RLCSYN are often of negative value (yet the complete realization is still passive). RLCSYN is employed, e.g., in the RC MOR method SparseRC [37].

6. Discussion

The main topic of this thesis is the partitioning and macromodeling -based MOR approach. The presented publications aim to show that the approach is efficient and well comparable to projection or elimination-based MOR approaches when dealing with typical interconnect circuits. The partitioning and macromodeling -based approach is composed of two parts: 1) partitioning and 2) macromodel-based approximation. Both of these present benefits (and some limitations) to MOR.

Partitioning provides a MOR method many assets. Probably the most important benefit of partitioning is that it allows the manipulation of virtually any size of circuit, because the problem can be divided into smaller manageable parts. Thus, for very large circuits (e.g., $> 10^9$ elements), partitioning of some kind is typically required in any case before MOR can be done. After partitioning, the problem can be processed using parallel processing, which can further speed up the reduction process [35]. For MOR, partitioning is especially useful because it allows the method to retain the block-sparsity of the original system, which is typically very sparse to start with. This in turn can increase the efficiency of the reduction, both in terms of required CPU resources and in achieved reduction efficiency. The latter has been a major problem especially for the projection-based MOR.

Using macromodels and explicit moment-matching in MOR is restricting, and care must be taken when designing prospective macromodels such that they are numerically robust. Furthermore, in general, if high accuracy is needed, a large number of moments needs to be explicitly matched in this fashion, which easily leads to ill-conditioned systems and cumbersome macromodels. On the other hand, using pre-selected macromodels ensures that the realization of the ROM is composed of desired element types, only (here: RLCK elements).

The publications [PI, PII] and [PIV] in this thesis are centered around the idea that by combining partitioning with otherwise limiting direct moment-matching, the number of matched moments can be kept very low and the macromodels small, with still acceptable approximation accuracy. Since the macromodels can be chosen such that they have only positive-valued standard RLCK elements, the resulting MOR methods generate passive and stable ROMs with good numerical reliability.

The latter portion of this thesis discusses typical problems with MOR methods and ways to deal with them. Especially, densely coupled circuits are discussed in the last three publications, because dense coupling is a serious problem for partitioning and elimination-based MOR approaches (but not so for projection-based approaches). It is shown that thanks to the partitioning-based approach, the original dense circuit can be considered at small sections at a time, and relatively simple approximations can be employed to overcome the coupling between interconnect lines. Of the presented methods, [PVII] can be used also as an augmentative tool in conjuction with elimination-based (or projection-based) MOR approaches.

Taken together, the presented publications present a robust RLCK-in–RLCK-out MOR algorithm package for interconnect circuits.

7. Summary of Publications

7.1 Study and development of an efficient RC-in–RC-out MOR method [PI]

This paper presents an efficient partitioning and macromodeling -based MOR method for RC circuits. Starting from the method by Liao and Dai [30], the original method is conceptually divided into three parts: circuit partitioning, moment calculation, and macromodel synthesis. For each of these parts, alternative approaches are presented. Using test simulations and theoretical analysis, the most efficient solution is then presented. Preliminary test results as well as a large part of the technical implementation of these methods are documented in [47].

The comparison resulted in a MOR flow that uses hMETIS [48] as a circuit partitioning algorithm [49], MNA-based block moment calculation (see Chapter 2), and the simplified macromodeling method, where a single resistance was used instead of the model shown in Fig. 4.3(a). This means that although the presented RC MOR method uses the same original idea as in [30], all the constituting components are revised for the most part, resulting in a more efficient MOR algorithm.

The final, revised partitioning-based RC MOR flow was compared to PRIMA [14], perhaps the most widely used RLC MOR method available, and to TICER, a well-known RC MOR method. Comparison of these three methods showed promising results for the partitioning-based approach: in the general case, the studied method outperformed TICER by a clear margin. In case of the studied RC circuits, PRIMA also often showed less efficient reduction results.

Overall, the presented RC-in–RC-out method performed well in terms of reduced CPU time and reduction accuracy. The (surprisingly) good per-

formance of the method served as an incentive for later research with partitioning-based MOR and many of the publications in this thesis.

7.2 Partitioning-based RL-in–RL-out MOR method [PII]

In this paper, the ideas behind the RC MOR paper presented in [PI] are applied for RL circuits in a dual fashion, resulting in an RL MOR method. By using a nodal equation formulation

$$\begin{cases} (\mathbf{G} + \frac{1}{s}\mathbf{\Gamma})\mathbf{x}_n = \mathbf{B}\mathbf{u}_N, \\ \mathbf{i}_N = \mathbf{L}^{\mathrm{T}}\mathbf{x}_n, \end{cases} \tag{7.1}$$

the inductances can be stamped in place of capacitances in $\mathbf{\Gamma}$ (as inverses of the inductance values), mirroring $\mathbf{C}$ in (2.1). This allows the y-parameter moments to be calculated afterwards in a similar manner as in [PI], now resulting in a series

$$\mathbf{Y}(s) = \mathbf{M}_0 + \mathbf{M}_1\frac{1}{s} + \mathbf{M}_2\frac{1}{s^2} + \cdots. \tag{7.2}$$

For macromodel synthesis, two macromodels are presented, identical to those in [PI], except that capacitances are replaced by inductances. The series (7.2) can then be matched with the Taylor expansion of the macromodel y-parameters, again similarly as in [30] and [PI].

The test case results of RL circuit reduction for the presented RL MOR method were good in accuracy and reduction efficiency.

7.3 Hierarchical model-order reduction flow [PIII]

This paper discusses the benefits of performing MOR in a hierarchical manner. Hierarchy enables dividing the problem into parts which can be handled separately, thus allowing faster processing (via parallel processing) and/or processing the problem with even low-end computational resources (due to reduced memory requirements). If the circuit contains repeated structures, with hierarchy they need to be analyzed only once. Finally, a different MOR method may be chosen for each individual part of the original problem, if necessary.

Circuit partitioning presents a natural way to benefit from hierarchical analysis, which was discussed briefly in [PI]. In paper [PIII], the hierarchical approach is discussed in more detail and on a more general level, concerning two MOR methods, the RC MOR method presented in [PI] and

PRIMA. Especially, the hierarchical MOR algorithm flow is presented for implementation purposes.

It is shown that both the MOR methods discussed benefit from hierarchical analysis, the RC MOR method particularly (as partitioning is a vital step of the method), but also PRIMA, in the case of very large circuits.

7.4 PartMOR: Partitioning-based realizable model-order reduction method for RLC circuits [PIV]

Inspired by the success of the partitioning and macromodeling -based MOR approach in the previous publications, the paper [PIV] extends the RC and RL MOR methods from [PI–PIII] and [46] into an RLC MOR method: PartMOR. The general idea of the method is shown in Fig. 4.1.

In order to achieve sufficient accuracy, two macromodels are presented, which are used to match three moments of the y-parameters (compared to the one or two moments matched in [PI] and [PII]). A vital property of this matching is that it is done simultaneously partly at DC and partly at infinity. This enables the macromodel to capture the frequency behavior of the original circuit with much better accuracy, especially in the case of RLC circuits. The reduction is performed by generating the y-parameter moment series (see Chapter 2) for the subcircuit branch at DC and infinity,

$$\mathbf{Y}(s) = \mathbf{M}_0 + \mathbf{M}_1 s + \mathbf{M}_2 s^2 + \cdots, \tag{7.3}$$

$$\mathbf{Y}(s) = \mathbf{N}_0 + \mathbf{N}_1 \frac{1}{s} + \mathbf{N}_2 \frac{1}{s^2} + \cdots. \tag{7.4}$$

The series generated at infinity is obtained by transforming the circuit elements by $s \to 1/s$ and then generating the series similarly as for the DC counterpart. After generating the two series, one or two first terms of the series are matched with the Taylor expansion of the presented RRC or RRL macromodel [Fig. 4.1(c)], to obtain the macromodel element values. The choice between the macromodels is made such that the R/L/C elements generated in the macromodel are positive-valued. Finally, the macromodels for each partition are recombined to obtain the total ROM circuit realization.

Regarding PartMOR, the main advantage of partitioning is that small enough RLC interconnect circuit partitions can be typically approximated using few moments with still sufficient accuracy. The use of few moments,

only, enables using numerically stable explicit matching with low-order macromodels. As the macromodels in turn can be relatively simple, it is possible to generate them using positive-valued RLC elements, only.

Additionally, the presented frequency transformation $s \rightarrow 1/s$ allows PartMOR to circumvent a singularity in the circuit G matrix in some typical cases (see [PV]), which would otherwise cause the MOR to fail.

A wide range of test simulations are presented, showing that PartMOR achieves excellent reduction results in terms of accuracy and reduction ratio for all types of RC, RL, and RLC circuits simulated. Finally, a comparison to SPRIM [15] using the RLCSYN [38] macromodel synthesis method — an available, state-of-the-art, RLC-in–RLC-out (netlist-in–netlist-out) MOR method — is presented. It is shown that PartMOR outperforms SPRIM+RLCSYN in terms of reduction efficiency for the cases shown and does not have many of the limitations SPRIM+RLCSYN place on the reduction.

7.5 Improving model-order reduction methods by singularity exclusion [PV]

This paper presents a novel stand-alone method for overcoming a singular system matrix in MOR algorithms, which would otherwise foil successful algorithm operation and thus reduction. The method is outlined in Fig. 7.1.

The idea of the proposed singularity exclusion method is to analyze the original netlist as a preprocessing step to the actual MOR, and exclude those parts of the circuit from the MOR that would generate the singularities to the system matrices. After reducing the remaining circuit, the excluded parts can be reconnected with the reduced circuit, to obtain the final (partially) reduced model for the complete circuit. The use of the method is further encouraged by the characteristic that often the problematic circuit parts in interconnect circuits that generate the singularities are located between interconnect segments, and/or consist of few elements in total. Thus, by locating and excluding these areas from the MOR with automated processing, high reduction ratio can still be ensured, with no loss in accuracy.

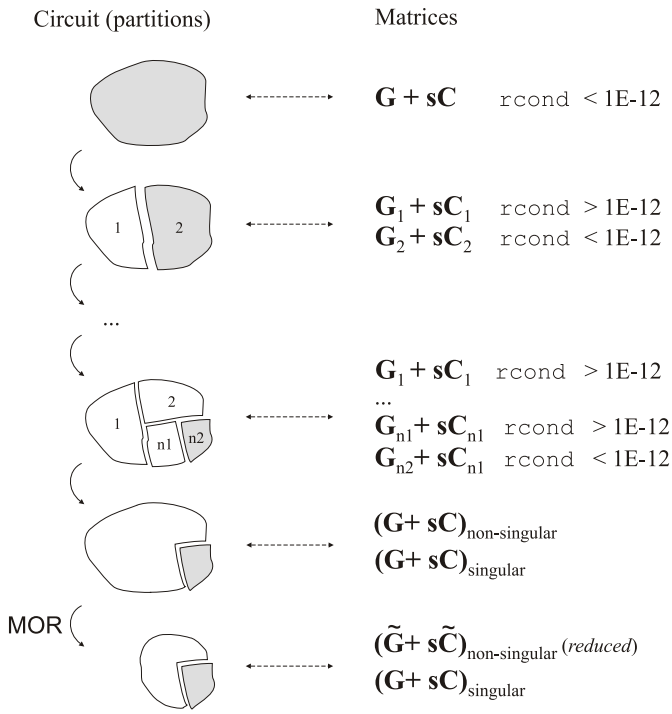


Figure 7.1. Exclusion of a singularity using the method in [PV]. The original circuit is partitioned into subcircuits in a progressive manner. At each step, the current partitions are evaluated for numerical condition (using Matlab rcond function). If the partition is ill-conditioned (e.g., if rcond $<$ 1E $-$ 12), it is partitioned further, and the generated (sub)partitions are analyzed again. When a suitably small partition size is reached, the partition with the ill-conditioning structure can be left out from the MOR. After the rest of the circuit is reduced, the unreduced partition can be reconnected to the reduced circuit.

7.6 Partitioning-based reduction of circuits with mutual inductances [PVI]

As discussed in the previous papers, partitioning is often a desirable, sometimes even mandatory, processing step in MOR methods. However, if a circuit contains dense mesh-like structures, such as coupling, partitioning becomes difficult or even impossible (Sec. 5.2). This reduces the usability of partitioning and limits the efficiency of partitioning-based methods considerably.

This paper presents an augmentative method to reduce the inductive coupling in a circuit to be used in addition to PartMOR or [PII], effectively turning these methods from RLC and RL MOR into RLCK and RLK MOR. By using the presented method, dense inductive coupling can be efficiently partitioned with the two (or other similar) MOR methods.

The basic idea of the presented method is to approximate the original circuit with a two-stage reduction. The method is outlined in Fig. 7.2(a, b, c).

First, the original circuit is considered at DC without the coupling as separate interconnect runs and partitioned into subcircuits. These subcircuits are reduced with PartMOR. Then, each pair of subcircuits is considered again and the inductive coupling between the branches is reduced separately by approximating that the current through the main branch stays relatively constant along the branch, such that $I_{\text{in}} \approx I_{\text{out}}$.

With the above approximation, the voltage over two branches (a, b) and (c, d) in Fig. 7.2(c) can be expressed

$$\begin{aligned} U^{a,b}(s) &= \textstyle\sum_{i=1}^{\beta} L_i^{a,b} I_{a,b} s + \sum_{i=1}^{\delta} R_i^{a,b} I_{a,b} + \sum_{i=1}^{\alpha} M_i I_{c,d} s \\ &\equiv L_{\Sigma}^{a,b} I_{a,b} s + R_{\Sigma}^{a,b} I_{a,b} + M_{\Sigma} I_{c,d} s, \end{aligned} \tag{7.5}$$

$$\begin{aligned} U^{c,d}(s) &= \textstyle\sum_{i=1}^{\gamma} L_i^{c,d} I_{c,d} s + \sum_{i=1}^{\zeta} R_i^{c,d} I_{c,d} + \sum_{i=1}^{\alpha} M_i I_{a,b} s \\ &\equiv L_{\Sigma}^{c,d} I_{c,d} s + R_{\Sigma}^{c,d} I_{c,d} + M_{\Sigma} I_{a,b} s, \end{aligned} \tag{7.6}$$

where $I_{a,b}$ and $I_{c,d}$ are the currents running through branches (a, b) and (c, d), and the branches have α mutual inductances, β and γ self inductances, and δ and ζ resistances, respectively. Now, the approximated total mutual coupling between the branches, M_{Σ}, can be added to the reduced macromodels generated for the main branches.

Since the reduction is realized with standard mutual inductances, the method is also easily integratable to any typical design flow using RLCK netlists.

7.7 Sparsification of dense capacitive coupling of interconnects [PVII]

Dense coupling is a problem for partitioning-based MOR approaches (Sec. 5.2). This paper presents a realizable RC(LM)-netlist-in–RC(LM)-netlist-out method to sparsify and reduce the capacitive coupling in circuits with interconnect lines. The method is applicable in conjunction with any partitioning-based model-order reduction algorithms, such as [PI], [PII], or [PIV], or as a separate stand-alone tool to sparsify only the capacitive coupling in any circuit simulation application, including other MOR methods such as TICER and PRIMA. It is shown that by using the method, circuits with even dense capacitive coupling can be partitioned and reduced efficiently.

The basic idea of the method proposed is to approximate the original circuit with a two-stage reduction, conceptually similar to [PVI]. The method is outlined in Fig. 7.2(a, b, d), where PartMOR is used for the reduction of main branches.

First, the original circuit is considered without the capacitive coupling (i.e., as separate interconnect runs) and partitioned into subcircuits. The subcircuits may be reduced using a pre-existing MOR method of choice. Then, each pair of subcircuits is considered again — this time including the capacitive coupling between the subcircuits — and the coupling effect is reduced separately by considering each pair of subcircuits as a separate N-port circuit, where the original capacitive coupling between the two subcircuits is re-introduced, as shown for branches (a, b) and (c, d) in Fig. 7.2(d). Now, the capacitive coupling between the two lines can be expressed with a y-parameter moment series newly calculated for the N-port at $s = 0$ as in (2.5).

The series is then approximated by its first two terms. The approximation is realized using a macromodel of a parallel capacitance C_{red}^{ij} and a resistance R_{red}^{ij} (where i and j refer to the indices of a matrix element), and the y-parameters of this macromodel are expanded to a Taylor series at $s = 0$. By matching the y-parameter moment series for the new N-port with the Taylor series, the element values for the macromodel can be then obtained. After generating the reduced macromodel for the coupling, it can be combined with the ROMs generated for the main branches.

The benefits of the method are that the netlist partitioning can be easily done, allowing efficient MOR; that even dense capacitive coupling does

not generate a dense system matrices for the MOR; and finally that the capacitive coupling is reduced to positive-valued (R)C-macromodels of few elements. Since the reduction is realized with standard circuit elements, the method is also easily integratable to existing realizable RC(LM)-in–RC(LM)-out MOR methods.

7.8 Realizable reduction of interconnect models with dense coupling [PVIII]

Continuing on the topic of dense coupling in original circuits, this paper combines the methods for the reduction of dense inductive and capacitive couplings, presented in [PVI] and [PVII], respectively. The paper discusses the specifics of integrating the two methods with PartMOR into a complete RLCK-in–RLCK-out MOR flow, capable of handling also typical densely coupled interconnects. The reduction flow is outlined in Fig. 7.2. Test simulations on interconnect circuits of the 65-nm technology node containing both inductive and capacitive coupling are presented and show efficient reduction results for reduced circuits.

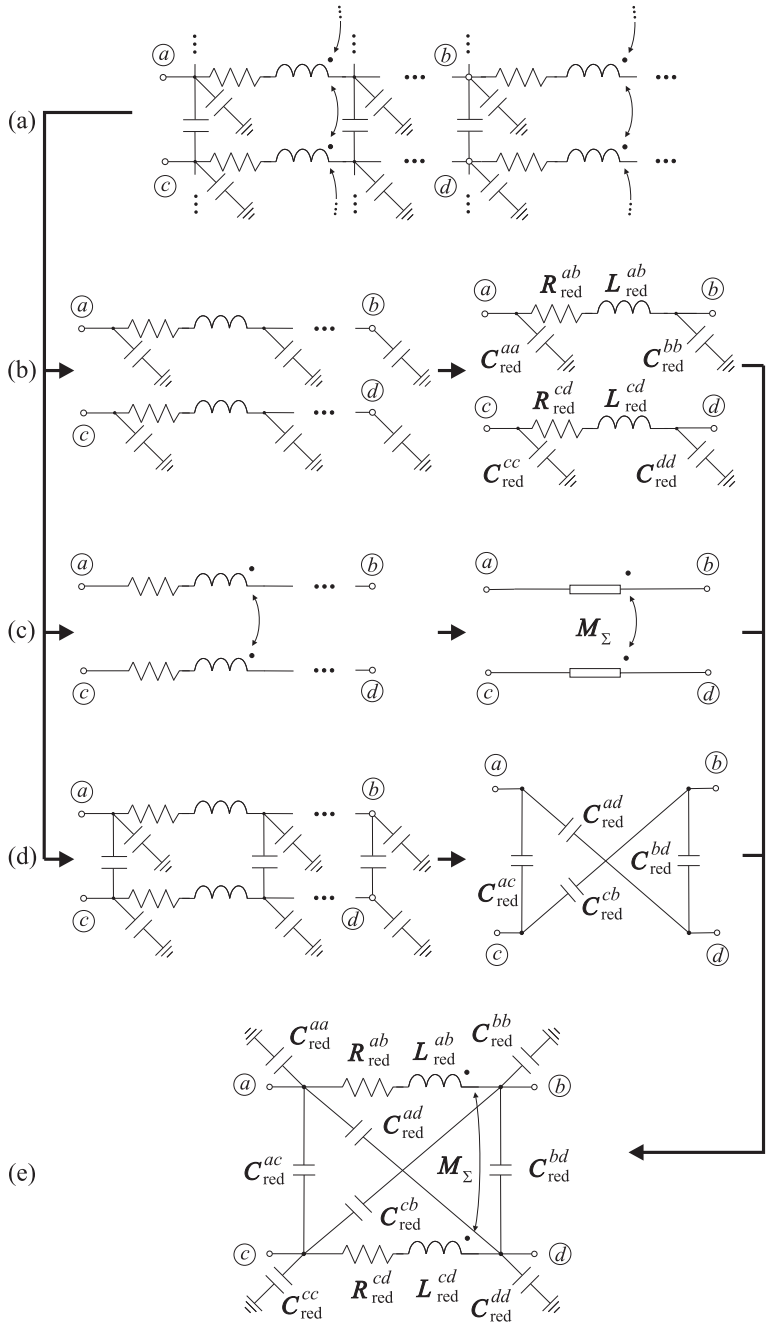


Figure 7.2. Sparsification of dense coupling between interconnects [PVIII]. (a) The original circuit with mutual inductive and capacitive coupling. (b) Reduction of main branch subcircuits (without coupling) using PartMOR. (c) Reduction of mutual inductive coupling. (d) Reduction of capacitive coupling. (e) The final macromodel for the two subcircuits and their coupling. The process is repeated for each pair of subcircuits that have coupling between the interconnect branches. Figure reprinted from [PVIII] ©IEEE 2013.

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Errata

Publication I

Page 1278: Replace $\mathbf{G}_{\mathrm{P}}$, $\mathbf{G}_{\mathrm{C}}$, and $\mathbf{G}_{\mathrm{I}}$ with $\mathbf{G}_{\mathrm{p}}$, $\mathbf{G}_{\mathrm{c}}$, and $\mathbf{G}_{\mathrm{i}}$, respectively.

Publication IV

Page 386: "– partitioning process with hMETIS was very fast in each case, and negligible compared to the total MOR algorithm CPU-time (<0.01s for circuits in Table II and III)."

Correction: "– partitioning process with hMETIS was relatively fast in each case, taking approximately 20–40% of the total MOR algorithm CPU-time."

Modern integrated circuits may contain billions of transistors and several kilometers of connecting wire per square centimeter. In order to simulate accurately the behavior of such circuits with virtual design tools, special computational algorithms must be used.

This thesis studies the use of model-order reduction using a partitioning and macromodeling -based approach to speed up the simulation of large integrated circuits. The presented divide-and-conquer type reduction algorithms can approximate the interconnect wire models in a circuit design with smaller representations, resulting in a reduced circuit model that is easier and faster to simulate.

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