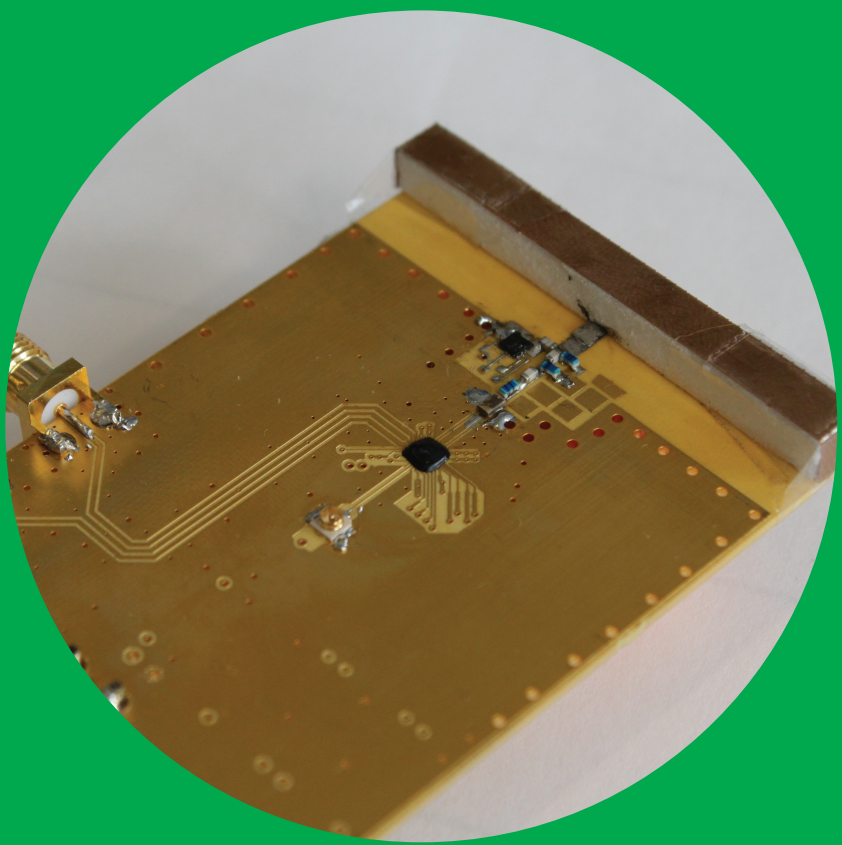
Department of Micro- and Nanosciences

Integrated radio frequency circuits for wideband receivers

Mikko Kaltiokallio



A!

DOCTORAL DISSERTATIONS

Aalto University publication series
DOCTORAL DISSERTATIONS 36/2014

Integrated radio frequency circuits for wideband receivers

Mikko Kaltiokallio

A doctoral dissertation completed for the degree of Doctor of Science (Technology) to be defended, with the permission of the Aalto University School of Electrical Engineering, at a public examination held at the lecture hall S1 of the school on 9 May 2014 at 12.

Aalto University
School of Electrical Engineering
Department Micro- and Nanosciences

Supervising professor
Professor Jussi Ryynänen

Preliminary examiners
Dr. Jan Craninckx, IMEC, Belgium
Prof. Peter Baltus, Technische Universiteit Eindhoven, The Netherlands

Opponent
Prof. Bram Nauta, University of Twente, The Netherlands

Aalto University publication series
DOCTORAL DISSERTATIONS 36/2014

ISBN 978-952-60-5615-9
ISBN 978-952-60-5616-6 (pdf)
ISSN-L 1799-4934
ISSN 1799-4934 (printed)
ISSN 1799-4942 (pdf)
http://urn.fi/URN:ISBN:978-952-60-5616-6

Unigrafia Oy
Helsinki 2014

Finland

Author
Mikko Kaltiokallio

Name of the doctoral dissertation
Integrated radio frequency circuits for wideband receivers

Publisher School of Electrical Engineering

Unit Department of Micro- and Nanosciences

Series Aalto University publication series DOCTORAL DISSERTATIONS 36/2014

Field of research Electronic Circuit Design

Manuscript submitted 14 November 2013 **Date of the defence** 9 May 2014

Permission to publish granted (date) 3 March 2014 **Language** English

☐ **Monograph** ☒ **Article dissertation (summary + original articles)**

Abstract

The multisystem, multiband problem in mobile terminals drives up the cost and complexity of the radios by requiring separate dedicated signal paths with discrete filtering. By removing the filters, the radios could be made more cost-efficient and flexible, and the signal path design would be simplified. However, in receivers, this demands that the front-end is capable of withstanding an extremely harsh interference environment while providing good sensitivity. This thesis concentrates on improving and developing receiver circuits that provide a wide reception bandwidth and tolerance against blockers.

Wideband receiver circuits are an attractive option to implement the future resource sharing radios with less dedicated hardware. A wideband dual-loop feedback LNA implemented in this work enables simultaneous matching and flat gain response over a 1.6 GHz reception band while only requiring a single inductor in the shunt-peeked load of the LNA. The use of a wideband LNA in a 60 GHz receiver has also been demonstrated. Additionally, wideband buffering circuits are reviewed and compared in this thesis.

The fast switching speed of the CMOS technology acts as the key enabler for the research performed in this work. One structure that utilizes this property is the N-path filter, which has been extensively utilized in the circuits presented. A feedback N-path filter in a wideband 2-to-6-GHz LNA has been implemented and analyzed. The analysis provides the evaluation of different design trade-offs and a guide to design such a system. Another circuit to use the Npath filter is the 0.7-to-2.7-GHz mixer-first receiver that was implemented together with a wideband CCE antenna. The work highlights the key challenges when wideband interfaces are implemented and suggests a solution to circumvent part of the challenges. The integrated circuit includes low-noise and low-distortion baseband stages to provide good overall performance. Additionally, the circuit demonstrates a novel duty-cycle control circuit for tuning the mixer-first receiver performance.

This thesis also includes an analysis and implementation of an active polyphase filter for LO quadrature generation. The analysis provides means for designing stable two-stage APPFs with optimal gain, image rejection ratio and bandwidth while being stable. This is demonstrated in a 1-to-5-GHz APPF that was implemented

Keywords radio receiver, mixer-first receiver, blocker tolerant, wideband LNA, duty-cycle control, active polyphase filter, wideband buffer

ISBN (printed) 978-952-60-5615-9 **ISBN (pdf)** 978-952-60-5616-6

ISSN-L 1799-4934 **ISSN (printed)** 1799-4934 **ISSN (pdf)** 1799-4942

Location of publisher Helsinki **Location of printing** Espoo **Year** 2014

Pages 196 **urn** http://urn.fi/URN:ISBN:978-952-60-5616-6

Tekijä
Mikko Kaltiokallio

Väitöskirjan nimi
Radiotaajuisia mikropiirejä laajakaistaisiin vastaanottimiin

Julkaisija Sähkötekniikan korkeakoulu

Yksikkö Mikro- ja nanotekniikan laitos

Sarja Aalto University publication series DOCTORAL DISSERTATIONS 36/2014

Tutkimusala Piiritekniikka

Käsikirjoituksen pvm 14.11.2013 **Väitöspäivä** 09.05.2014

Julkaisuluvan myöntämispäivä 03.03.2014 **Kieli** Englanti

☐ **Monografia** ☒ **Yhdistelmäväitöskirja (yhteenveto-osa + erillisartikkelit)**

Tiivistelmä

Tässä väitöskirjassa on keskitytty kehittämään ja parantamaan laajakaistaiseen vastaanottoon ja hyvään häiriönsietoon kykeneviä radiovastaanotinmikropiirejä. Niiden avulla vastaanottimet voitaisiin toteuttaa yksinkertaisemmin ja edullisemmin. Lisäksi ne voisivat toimia joustavammin.

Laajakaistaiset vastaanotinpiirit ovat yksi mahdollinen vaihtoehto kun pyritään toteuttamaan seuraavien sukupolvien radioita kustannustehokkaasti. Tässä työssä on kehitetty laajakaistainen kaksoistakaisinkytketty pienikohinainen vahvistin, joka kykenee samanaikaisesti saavuttamaan tasaisen taajuusvasteen ja riittävän sovituksen 1.6 GHz -taajuuskaistalla vain yhtä kelaa hyödyntäen. Väitöskirjassa on lisäksi toteutettu laajakaistainen vahvistin osana 60 GHz -millimetriaaltovastaanotinta. Työssä on myös vertailtu laajakaistaisia puskurirakenteita.

Nykyaikaisen CMOS-prosessiteknologian nopea kytkeytymisnopeus on keskeisessä roolissa tässä työssä kehitetyissä piiriratkaisuissa. Eräs rakenne joka hyödyntää tätä ominaisuutta on monitiesuodatin. Tässä väitöskirjassa monitiesuodattimia on käytetty laaja-alaisesti eri vastaan-otinratkaisuissa. Monitiesuodatinta on hyödynnetty muunmuassa takaisinkytketyssä laajakais-taisessa 2--6 GHz -vastaanottimessa, joka on analysoitu ja toteutettu. Kehitetty analyysi mahdol-listaa kyseisen vastaanottimen suorituskykyriippuvuuksien tarkastelun ja optimoinnin. Toinen vastaanotintoteutus, joka hyödyntää monitiesuodatinta, on 0.7--2.7 GHz -suorasekoitin-vastaanotin. Työssä toteuttiin vastaanottimen suunnittelu ja yhdistäminen laajakaistaisen CCE- antennin kanssa. Antennin yhdistämisen mukanaan tuomia haasteita on käsitelty sekä esitetty ratkaisu, joka ratkaisee osan haasteista. Lisäksi vastaanottimessa on toteuttettu vähäkohinaiset sekä pienisäröiset kantataajuusvahvistimet, jotka mahdollistavat hyvän kokonaissuorituskyvyn. Koska suorasekoitinvastaanottimessa suorituskyky riippuu keskeisesti sekoittimen suoritus-kyvystä, on tässä työssä lisäksi kehitetty analoginen kellon pulssisuhteen säätöpiiri, jonka avulla sekoittimen toimintaa kyetään säätämään.

Väitöskirjassa on kehitetty paikallisoskillaattoripolulle aktiivinen monivaihesuodatin, jonka avulla voidaan synnyttää kvadratuurisignaali sekoitinta varten. Työssä kehitetyn analyysin pohjalta voidaan suunnitella stabiili kaksiasteinen monivaihesuodatin, jolla on optimaalinen vahvistus, peilitaajuusvaimennus sekä toimintakaista. Toteutettu koepiiri mittaustuloksineen todentaa kehitetyn suodattimen toimivuuden 1--5 GHz -radiotaajuusalueella.

Avainsanat laajakaistainen vastaanotin, sekoitin, vähäkohinainen vahvistin, monitiesuodatin, LO-piirit, CMOS, häiriösietoisuus

ISBN (painettu) 978-952-60-5615-9 **ISBN (pdf)** 978-952-60-5616-6

ISSN-L 1799-4934 **ISSN (painettu)** 1799-4934 **ISSN (pdf)** 1799-4942

Julkaisupaikka Helsinki **Painopaikka** Espoo **Vuosi** 2014

Sivumäärä 196 **urn** http://urn.fi/URN:ISBN:978-952-60-5616-6

Preface

The work for this thesis was carried out in the Electronic Circuit Design Unit of Aalto University (former ECDL of Helsinki University of Technology) between 2006 and 2013. The work was executed in collaboration projects between the laboratory, Nokia Corp., Nokia Research Center, and the Finnish Funding Agency for Technology and Innovation (TEKES). Other partners that participated in the projects include Optenni, Sasken Finland, and AWR-Aplac. During the years in the laboratory I was also a postgraduate student of the Graduate School in Electronics, Telecommunication and Automation (GETA) which supported my research financially and provided great trips to interact with other like-minded students. I would also like to acknowledge the following foundations for supporting this thesis work: Nokia Foundation, Emil Aaltonen Foundation, Jenny and Antti Wihuri Foundation, and Walter Ahlström Foundation.

I would like to thank my supervisor Prof. Jussi Ryynänen for all the guidance and support during the years. We also had our disagreements and difficult times, but we still managed to come out on top and remain friends in the process, which one should not take for granted. I would also like to express my gratitude to Saska Lindfors for inspiring my early travels as an electronics researcher and Prof. Kari Halonen for providing me the possibility in the first place to work in the laboratory. Prof. Peter Baltus and Dr. Jan Craninckx deserve thanks for the pre-examination of this thesis and for providing valuable comments. Prof. Bram Nauta is highly acknowledged for reading this thesis and acting as the opponent.

During the course of this thesis work the I was involved in 11 IC tape-outs with CMOS processes of 130nm, 65nm and 28nm with the 65nm node covering the majority of the runs. While some of these implementations did not yield great scientific results and some did, every single one was a great learning experience. Furthermore, these tape-outs welded many

friendships and brought unforgettable memories to the people who participated in them. I want to thank each and everyone of my coworkers who participated in these ordeals. Tapio Rapinoja, Olli Viitala, and Tero Tikka deserve a special thanks for sharing technical and free-time interests with me. Other people who deserve to be mentioned include Risto, Jouni, Kari, Kim, Anu, Mikko, Pikkis, Late, and Varonen - just to name a few.

I am grateful to my parents, Kim and Päivi, for all the support you have provided me during my life. No words can express their value. My siblings Ossi and Maija-Leena have also played an important part in my life and I would not be who I am without you. I especially like to thank my dad and brother for interesting and inspiring technical discussions in the sauna of our summer cottage.

And most importantly, I want to express my greatest gratitude to my lovely wife Jenni and daughter Emilia. You are the most precious things in life to me.

Espoo, March 20, 2014,

Mikko Kaltiokallio

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I M. Kaltiokallio, V. Saari, T. Rapinoja, K. Stadius, J. Ryynanen, S. Lindfors and K. Halonen. A WiMedia UWB Receiver with a Synthesizer. In *IEEE European Solid-State Circuits Conference*, Edinburgh, United Kingdom, pp. 330-333, September 2008.

II M. Varonen, M. Kaltiokallio, V. Saari, O. Viitala, M. Karkkainen, S. Lindfors, J. Ryynanen and K. A. I. Halonen. A 60-GHz CMOS Receiver With an On-Chip ADC. In *IEEE Radio Frequency Integrated Circuits Symposium*, Boston, United States, pp. 445-448, June 2009.

III M. Kaltiokallio, A. Parssinen and J. Ryynanen. Wideband Trans-Impedance Filter Low Noise Amplifier. In *IEEE Radio Frequency Intergrated Circuits Symposium*, Anaheim, United States, pp. 521-524, May 2010.

IV M. Kaltiokallio, V. Saari, S. Kallioinen, A. Parssinen and J. Ryynanen. Wideband 2 to 6 GHz RF Front-End with Blocker Filtering. *IEEE Journal of Solid-State Circuits*, Vol. 47, no. 7, pp. 1636-1645, July 2012.

V M. Kaltiokallio, R. Valkonen, K. Stadius and J. Ryynanen. A 0.7–2.7-GHz Blocker-Tolerant Compact-Size Single-Antenna Receiver for Wideband Mobile Applications. *IEEE Transactions on Microwave Theory and Techniques*, Vol. 61, no. 9, pp. 3039-3049, September 2013.

VI M. Kaltiokallio, J. Ryynanen and S. Lindfors. Active Polyphase Filter Analysis. In *IEEE International Symposium on Circuits and Systems*, Paris, France, pp. 1125-1128, June 2010.

VII M. Kaltiokallio and J. Ryynanen. A 1 to 5GHz Adjustable Active Polyphase Filter for LO Quadrature Generation. In *IEEE Radio Frequency Intergrated Circuits Symposium*, Baltimore, United States, pp. 1-4, June 2011.

Author's Contribution

Publication I: "A WiMedia UWB Receiver with a Synthesizer"

The author designed the low noise amplifiers, RF buffers, down-conversion mixers and the LO quadrature chain for the integrated circuit described in the publication. Additionally, the author developed the baseband filter pre-distortion technique that was utilized in the circuit. The paper was written by Mr. Rapinoja, Dr. Saari and the author. Dr. Lindfors, Prof. Ryynanen and Prof. Halonen supervised the work.

Publication II: "A 60-GHz CMOS Receiver With an On-Chip ADC"

The paper is based on the previous work of the authors. The paper combined the 60-GHz front-end to an UWB receiver, which acts as an IF stage in the complete receiver. The author was responsible for the IF stage in the receiver. Dr. Varonen and Mr. Karkkainen were responsible for the 60-GHz front-end, Dr. Saari was responsible for the baseband filter and Mr. Viitala for the analog-to-digital converter. Dr. Lindfors, Prof. Ryynanen and Prof. Halonen supervised the work.

Publication III: "Wideband Trans-Impedance Filter Low Noise Amplifier"

The author had the main responsibility of the content of the paper. The filtering concept described in the paper was developed in the co-operation of the author and Prof. Ryynanen. The author was responsible for the design, implementation and measurement of the circuit. Dr. Parssinen and Prof. Ryynanen assisted in writing of the paper and supervised the

work.

Publication IV: "Wideband 2 to 6 GHz RF Front-End with Blocker Filtering"

The author developed the original filtering topology and the analysis described in the paper and carried out the implementation work. Dr. Saari and Mr. Kallioinen implemented the baseband filter in the circuit. Dr. Parssinen and Prof. Ryynanen supervised the work.

Publication V: "A 0.7–2.7-GHz Blocker-Tolerant Compact-Size Single-Antenna Receiver for Wideband Mobile Applications"

The original idea was developed under close co-operation by Dr. Valkonen and the author. Dr. Valkonen was responsible for the antenna implementation and the author for the integrated circuit implementation. The author had the main responsibility in writing the paper, whilst Dr. Valkonen wrote the antenna-related content in the paper. Dr. Stadius and Prof. Ryynanen assisted in writing of the paper and supervised the work.

Publication VI: "Active Polyphase Filter Analysis"

The author was responsible for developing the analysis and carried out the simulations for the paper. Dr. Lindfors and Prof. Ryynänen assisted in writing the paper and supervised the work.

Publication VII: "A 1 to 5GHz Adjustable Active Polyphase Filter for LO Quadrature Generation"

The paper is based on the original idea of the author. The author designed, implemented and measured the circuit discussed in the paper. Prof. Ryynanen supervised the work and proof-read the paper.

List of Abbreviations

3G	3rd generation mobile communication systems
4G	4th generation mobile communication systems
AD	analog-to-digital
ADC	analog-to-digital converter
APPF	active polyphase filter
BB	baseband
BER	bit error ratio
BG	band group
CA	carrier-aggregation
CCC-CDCS	capacitively-cross-coupled common-drain common-source
CCE	capacitive coupling element
CDMA	Code Division Multiple Access
CG	common gate
CM	common mode
CMFB	common-mode feedback
CMOS	complementary metal oxide semiconductor
CR	cognitive radio
CS	common source
CSCG	common source common gate
CW	continous wave
DA	digital-to-analog
DC	direct current
DCR	direct-conversion receiver
DSP	digital signal processing
DTC	discrete tunable capacitor

E-UTRA	Evolved Universal Terrestrial Radio Access
ENOB	effective number of bits
ESD	electrostatic discharge
FCC	Federal Communications Commission
FDD	frequency division duplexing
GCPW	grounded co-planar waveguide
GPS	Global Positioning System
GSM	Global System for Mobile Communications
IC	integrated circuit
ICP	input compression point
IDCS	inductively degenerated common source
IF	intermediate frequency
IIP2	input-referred second-order intercept point
IIP3	input-referred third-order intercept point
IMD2	second-order intermodulation distortion
IMD3	third-order intermodulation distortion
IQ	in-phase quadrature-phase
IR-UWB	impulse-response ultrawideband
IRR	image rejection ratio
LNA	low noise amplifier
LO	local oscillator
LTE	long term evolution
LTE-A	long term evolution advanced
MB-OFDM	multiband orthogonal frequency-division multiplexing
MIMO	multiple-input-multiple-output
NEF	noise excess factor
NMOS	N-channel metal-oxide semiconductor transistor
OFDM	orthogonal frequency-division multiplexing
PA	power amplifier
PCB	printed circuit board
PGA	programmable gain amplifier
PLL	phase locked loop
PMOS	P-channel metal-oxide semiconductor transistor
PPF	polyphase filter

PVT	process, voltage, temperature
Q	quality factor
QFN	quad-flat no-leads package
RF	radio frequency
RFIC	radio frequency integrated circuits
RX	receiver
SDR	software-defined radio
SF	source follower
SG	spreading gain
SMA	surface mount assembly
SNR	signal-to-noise ratio
TDD	time division duplexing
TIF	transferred impedance filter
TX	transmitter
UMTS	Universal Mobile Telecommunications System
UWB	ultrawideband
VGA	variable gain amplifier
WCDMA	Wideband Code Division Multiple Access
WLAN	wireless local area network
WPAN	wireless personal area network

List of Symbols

A	voltage gain
A_{dc}	dc gain
A_i	insertion voltage gain
A_v	voltage gain
BNF	blocker noise figure
BW	bandwidth
C	capacity
C_{fb}	feedback capacitance
C_L	load capacitance
C_{out}	output capacitance
C_{ox}	oxide unit capacitance
C_p	paracitic capacitance
C_{pad}	pad capacitance
$e_{n,out}$	output noise voltage
f	frequency
f_{3db}	output -3dB frequency
f_b	notch -3dB bandwidth
f_i	input pole frequency
f_n	notch offset frequency
G	gain
G_{IF}	gain at intermediate frequency
G_p	power gain
g_m	transconductance
G_t	transducer gain
I_b	bias current
I_{ds}	drain-source current

I_L	leakage current
I_o	output current
k	pole splitting factor of a polyphase filter
k_B	Boltzmann's constant, $1.3807 \cdot 10^{-23}$ J/K
K_f	transistor-specific flicker noise constant
L	transistor length
L_{att}	matching loss
L_i	input inductance
L_L	load inductance
n	harmonic index
NF	noise figure
p	relative intrinsic pole scaling factor
P_1	test tone 1 power
P_{1dB}	-1dB input compression point
P_2	test tone 2 power
P_B	blocker power
P_{in}	power at input
P_L	power at load
PN	phase noise
$P_{S,av}$	available power at input
R_a	antenna resistance
R_{fb}	feedback resistance
R_L	load resistance
R_m	mixer on-resistance
R_{ppf}	polyphase resistance
R_S	source resistance
R_{sw}	switch resistance
S	sensitivity
S_{11}	input matching
SNF	spot noise figure
SNR_{in}	input signal-to-noise ratio
SNR_{min}	minimum signal-to-noise ratio
SNR_{out}	output signal-to-noise ratio
SNR	signal-to-noise ratio
T	absolute temperature

$V_{1/f}$	flicker noise voltage
$V_{n,A}$	amplifier noise voltage
V_{in}	input voltage
$V_{in,rms}$	root-mean-square input voltage
V_L	load voltage
$V_{L,rms}$	root-mean-square load voltage
V_S	source voltage
$V_{S,rms}$	root-mean-square source voltage
V_t	threshold voltage
$Y_{a,n}$	harmonic conductance
Z_0	reference impedance
Z_a	antenna impedance
Z_{bb}	baseband impedance
Z_{fb}	feedback impedance
Z_{in}	input impedance
Z_L	load impedance
Z_{out}	output impedance
Z_{par}	parasitic impedance
Z_{rf}	RF impedance
Z_{sh}	shunt impedance
γ	Fourier series coefficient
λ	wavelength
ω_{3db}	-3dB frequency
ω_c	center frequency
ω_{IF}	IF frequency
ω_{LO}	LO frequency

1. Introduction

1.1 Background

The beginning of the 21st century has witnessed a rapid evolution in wireless communication systems. Mobile terminals have evolved from the single system phones of the 1990s to the current 4G multisystem smartphones of today. The role of mobile radio has never been more important than it is now. Mobile devices define the way we communicate and how we do business. They are a driving force, an enabler technology, behind new innovation and economies. Similar to oil, they expedite new growth and bring wellbeing to societies.

To keep up with growth and development, a higher data transmission capacity has been continuously demanded. Up until the present, this has been achieved by introducing new radio bands and communication standards, by increasing the channel bandwidth, and by using more advanced modulations. While this has worked well in the past, it has made the communication devices extremely complex. Designing such devices has become a massive and costly engineering task to complete. It has been recognized for a long time that this path of development cannot continue forever, and recently, new ways of confronting the multisystem problems have been researched.

The radio frequency (RF) front-end remains to be a bottleneck that limits the combination of the various systems into a general purpose radio, or a software-defined radio (SDR), as it is often called. In order to succeed, one of the key obstacles is to minimize the number of external components and deal with the implications of this effort. In order to resolve the RF front-end problems, new structures and solutions are required to replace or complement the current solutions. Since the CMOS technology

evolution is mainly driven by the microprocessor industry, the analog performance is not improving as much with the new process nodes and the only properties that keep improving are the transistor switching speed and capacitor layout density. Thus, the key in resolving the RF front-end problems is to take advantage of the properties of the latest CMOS technology. This trend already defines radio development and can enable completely new concepts that revolutionize the way we design and build handsets. These changes might emerge sooner than we might expect, but they will keep challenging and motivating future academic and industry research.

1.2 Objective of the thesis

An ideal radio receiver for a mobile device is a receiver that can be tuned to any frequency and system while simultaneously using no external components and only utilizing a single input. In addition, such a receiver would consume very little power and silicon area and would have a low noise figure. Most importantly, the receiver would have an extremely large dynamic range, meaning that the reception would not be corrupted by interferers. Unfortunately, such a receiver does not yet exist and many of the requirements contradict each other. However, if we take a more practical approach to these requirements, we can then formulate a more realistic goal for a receiver that takes us one step closer to an ideal solution.

The main objective of this thesis is to develop practical receiver circuits for mobile terminals that can operate flexibly across a wide frequency range and withstand the harsh interference environment faced by a wideband receiver. While the transmitter is an equally important part of a communication system as the receiver, it has been left out of the scope of this thesis. That implies that many issues related to the receiver-transmitter operation, for instance in a frequency division duplex (FDD) system, are not considered. However, the solutions presented in this thesis are valid even when implemented together with a transmitter.

1.3 Organization and contents of the thesis

The fast switching speed of the nano-millimeter-scale CMOS technology acts as the key enabler for the research performed in this work. By taking advantage of this property, the author has devised structures that implement flexible, frequency-tunable, and selective structures. The designed receiver circuits cover a frequency band ranging from 0.7 to 8 GHz, which encompasses all of the current and near-future mobile handset cellular and wireless connectivity frequencies except millimeter-wave frequencies.

In this thesis, aspects of advanced circuit design techniques, mixed-signal design, and RF design have been used to achieve the results. During verification of the results, extensive work on component, connector, and printed circuit board (PCB) modeling has been carried out in addition to the normal prototyping and measurements. The main scientific contributions are found in the publications [I-VII] and in Chapters 2-7 of this summary, which collects and highlights the obtained results while providing references to other relevant research done in related fields. This thesis is organized as follows.

Chapter 2 concentrates on the fundamental basics of wideband receiver design. The chapter covers the modern receiver architectures, wideband receiver applications, and receiver design parameters on a general level. The purpose is not to provide in-depth discussion on all aspects of receiver design, but to give the basic background information needed to understand the topics covered in this work.

The design principles of wideband, low-noise amplifiers (LNA) and a comparison of different wideband LNA topologies is presented in Chapter 3. The design trade-offs for the feedback LNA topology used in [I,II] are presented. A review and comparison of wideband buffer topologies is also presented. The experimental circuits utilizing the feedback topology demonstrate the solution in an ultrawideband (UWB) receiver.

The versatility of the N-path filter and passive mixer for frequency-agile and interference-tolerant receiver structures is presented in Chapters 4 and 5. In Chapter 4, general design principles and the theory of passive mixers are discussed first. Then a design trade-off study that presents the effects of the interface impedances around the passive mixer is provided and, additionally, the effects of the switch sizing are shown. The operating principle and examples of the N-path filter are presented at the end of Chapter 4. The N-path filter has been utilized in this thesis in three

different receivers [III-V] to improve the selectivity and linearity of the receivers that are presented in Chapter 5. The chapter also discusses the measured results and compares it to relevant research.

Finally, Chapter 6 presents the design aspects of a local oscillator drive and quadrature generation for down-conversion mixers. A novel method of controlling the local oscillator (LO) duty cycle is presented. With this method, the gain, noise, and linearity performance of the passive mixer can be adjusted, as has been reported in [V]. The chapter also includes the active polyphase filter (APPF) analysis [VI] and implementation [VII]. The analysis provides a means for designing stable APPFs with an optimal gain, image rejection ratio (IRR), and bandwidth while still being stable. This was demonstrated in [VII] where a 1-to-5-GHz APPF was implemented.

1.4 Main scientific contributions

The novel scientific results obtained in this thesis are related to the field of integrated receiver circuits that support the operating flexibility needed in software-defined radio (SDR) and cognitive radio (CR) systems. The proposed circuits represent improvements to the prior art and also present new approaches for solving existing problems in flexible and wideband receiver systems in mobile telecommunications. The main scientific contributions of this thesis to the scientific community are as follows:

1. A novel feedback N-path filter in a wideband 2-to-6-GHz LNA was implemented as part of a receiver. The feedback system was simplified and analyzed with the help of Y-parameters and a frequency translation technique. The analysis provided an evaluation of the different design trade-offs and a guide to design such a system. The experimental results verified the functionality of the system and showed that the technique provides results that are comparable to the other state-of-the-art blocker filtering techniques.

2. A 0.7-to-2.7-GHz, mixer-first receiver was implemented with a wideband capacitive coupling element (CCE) antenna. The work highlighted the key challenges when wideband SDR interfaces are implemented and suggested a solution for circumventing part of the challenges. Furthermore, the system measurements with the antenna provided valuable

insights to the implementation of a wideband SDR interface. The integrated circuit included low-noise and low-distortion baseband stages that provide good overall performance as well as innovative LO circuits to enhance the mixer performance.

3. Analysis of the mixer-first receiver input interface was conducted, which describes the different design trade-offs that are related to the implementation. The analysis was used to justify the design choices made during the implementation.

4. An adjustable, duty-cycle circuit for LO signal generation was implemented. The circuit allows for continuous tuning of the LO signal duty cycle, which greatly affects the passive-mixer performance in down- and up-conversion. The circuit was implemented as a part of a mixer-first receiver and its impact on the receiver performance was verified using measurements.

5. An active polyphase filter analysis for 1- and 2-stage polyphase filters with simplified transconductance models was implemented. The gain, stability, and IRR of the filter were analyzed and a design example was given to show how to design such filters.

6. An active polyphase filter implementation and experimental verification. The implementation consists of a high-frequency, adjustable g_m element that is optimized for active PPF. The filter achieves a tuning range of 1 to 5 GHz with an IRR better than 40 dB.

7. A new dual-feedback LNA topology for an UWB front-end was implemented. The topology enables simultaneous input matching and flat gain response over a 1.6 GHz reception band while only requiring a single inductor in the shunt-peaked load of the LNA.

2. Overview of wideband receiver design

This chapter concentrates on the fundamentals of wideband receiver design. It covers modern receiver architectures, wideband receiver applications, and receiver design parameters on a general level. The purpose is not to provide an in-depth discussion on all aspects of receiver design, but to give the basic background information needed to understand the topics covered in this work.

2.1 Receiver architectures

The purpose of the receiver is to capture the signal at the antenna and perform signal operations such that the information at a particular radio channel can be observed correctly while adding as little interference and noise on the channel as possible. Typically, this means that the signal needs to be amplified, down converted, filtered, and analog-to-digital (AD) converted while maintaining an adequate signal-to-noise ratio (SNR). In the field of radio frequency integrated circuits (RFIC), the goal is to simultaneously perform these tasks with as few external components, as small an integrated circuit (IC) die size, and as low power consumption as possible. The tasks of a radio front-end in a receiver include frequency band selection, low-noise amplification, and frequency down-conversion onto lower frequencies. How these tasks are partitioned varies between the receiver architectures and will be covered next for the superheterodyne and direct-conversion architectures. Other architectures, such as the low-IF [1] and wideband-IF [2] architectures are beyond the scope of this thesis.

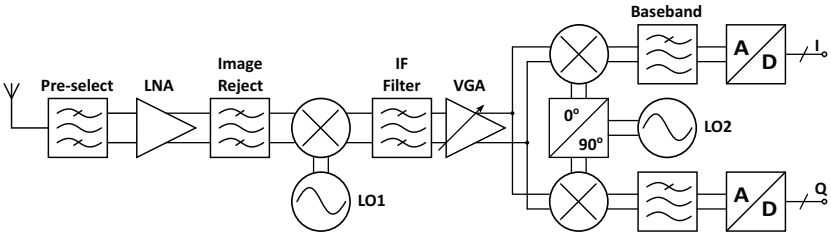


Figure 2.1. Superheterodyne receiver architecture.

2.1.1 Superheterodyne architecture

Of the wireless receiver architectures currently in use, the superheterodyne receiver architecture has been used for the longest time. This multiconversion architecture was introduced by Armstrong [3] to replace the tuned radio frequency receiver and it offers good sensitivity and selectivity. The drawbacks of the architecture are that it requires an external high-Q filter and multiple LO signals. Also the circuit complexity is high due to the number of filters deployed in the architecture.

In the superheterodyne architecture, shown in Fig. 2.1, the received signal is first filtered to reject strong out-of-band blockers and then amplified by the low noise amplifier (LNA) to suppress the noise of the following blocks. The signal is then filtered by the image reject filter, which attenuates the noise and interference on the image frequency. The choice of intermediate frequency (IF) determines the image reject filter requirements as well as the requirements of the IF filter through the offset from the receive band. If Hartley's [4] or Weaver's [5] image reject topology is deployed, then the image reject filter is not required, but this requires additional hardware and good matching between the circuit components to achieve sufficient image rejection. The first down-conversion (LO1) to IF is followed by the high-Q channel select IF filter, which relaxes the dynamic range requirements of the baseband. The variable gain amplifier (VGA) adjusts the level of the signal before the signal is down-converted by the second quadrature mixer. Before the analog-to-digital converter (ADC), the signal is further filtered by the baseband filter, which also acts as an anti-alias filter for the converter.

An interesting development related to the superheterodyne architecture has to do with the N-path filters, which can, potentially, flexibly implement the high-Q image-reject and IF filters used in the architecture. The filter concept has been functionally proven to work, but there are still unresolved issues, such as the amount of absolute selectivity and harmonic

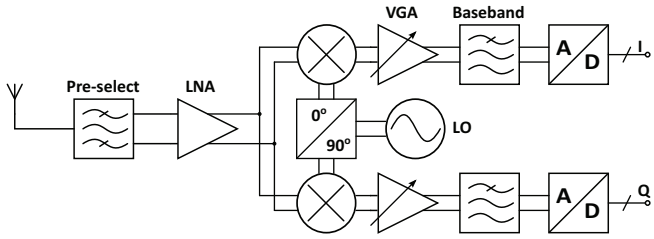


Figure 2.2. Direct-conversion receiver architecture.

down-conversion [6, 7]. If applicable, it could have a tremendous effect on wireless and cellular IC implementations in the future. N-path filters will be further discussed in Chapters 4 and 5.

2.1.2 Direct-conversion architecture

The direct-conversion receiver (DCR), also called the homodyne or zero-IF architecture, was first published by F. M. Colebrook [8] in 1924. It then lay unused for a long time, until the 1980s, when it was used in paging receivers [9, 10]. By this time, integrated circuit technology had evolved to a point where many of the challenges (see below) of the DCR could be addressed. From there, the architecture was widely adopted for cellular use, to a point where multiple receivers were simultaneously integrated on the same IC [11].

A block diagram of the direct-conversion receiver is shown in Fig. 2.2. As the name zero-IF suggests, with a DCR the RF signal is directly converted into a baseband after pre-select filtering and amplification by the LNA. The mixer needs to perform quadrature down-conversion into I- and Q-phases so that the signal information on both sides of the LO frequency is not corrupted [12]. The removal of the image-reject and IF filters results in hardware and power savings. Moreover, the VGA is typically located at the baseband and thus it is much more power efficient to implement an amplifier there than on the IF frequency of the superheterodyne architecture. Furthermore, power is also saved in the LNA, which needs not to drive the 50-Ω input impedance of the external image-reject filter.

There are a number of challenges with the DCR, with the direct current (DC) offset being one of them [9, 12]. One source of DC offset is the limited reverse isolation of the mixer and LNA. The LO signal can leak from the mixer through the LNA or via external bond wires and reflect back from the antenna or other discrete components. The reflected energy becomes an in-band blocking signal at the passband of the pre-select filter and the

LNA and is self-mixed at the mixer, resulting in a DC offset. Furthermore, the user hand affects the antenna reflection making it a dynamic problem in the receiver. Similarly, a strong blocking signal that is close to the passband of the LNA can make its way to the mixer and couple to the LO port, causing again a DC offset. What is worse, the DC offsets linked to the self-mixing are time-varying errors that need to be actively compensated for. Another major source of DC offset is component mismatches in the mixer and baseband circuits. An offset of only a few mV's at the mixer output is enough to saturate the output of the receiver with a baseband gain of 40-60 dB. The offset can be high-pass filtered in systems like UWB, wireless local area network (WLAN), or Wideband Code Division Multiple Access (WCDMA) without seriously degrading the SNR of the receiver. For narrowband systems, such as Global System for Mobile Communications (GSM), the offset must be actively compensated for by means of calibration or other methods [12–14]. Flicker noise is another challenge of the DCR architecture. For narrowband systems, like GSM, a high flicker noise corner frequency in the mixer and baseband active devices can add a substantial amount of low-frequency noise compared to the thermal noise of the system. Other challenges with the DCR include in-phase quadrature-phase (IQ) mismatch and even-order distortion, which are discussed in more detail, for example, in [9, 12–16].

2.2 Wideband receiver applications

Although the current cellular communication systems are mostly narrowband, the first wireless transmissions by Tesla and Marconi [17] used impulse-type, spark-gap generators for a wideband wireless transmission to convey information over the air. As mentioned above, the era of cellular communications has given rise to various narrowband systems, such as the GSM and Code Division Multiple Access (CDMA), which both use a pre-determined, fixed, and relatively narrow RF band for communication. These systems use complex channel coding and modulation such that they can provide maximal throughput with a narrow spectrum band that they have available [18]. These systems are so advanced that they are approaching Shannon's capacity limit [19], and further increase in the data rate mandates an increase in the transmission bandwidth, as can be observed from (2.1).

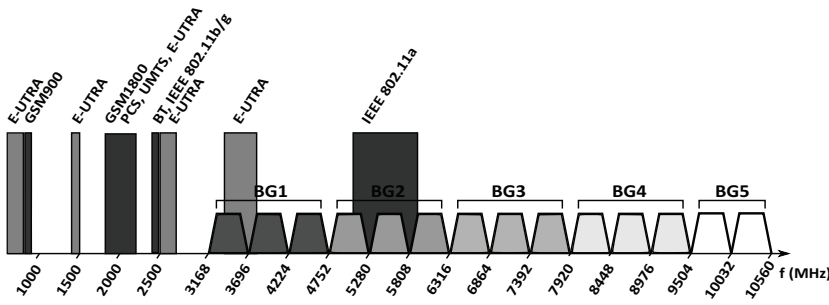


Figure 2.3. UWB band allocation and potential interferers in a mobile handset.

$$C = BWlog_2(1 + SNR). \tag{2.1}$$

In (2.1), C is the capacity limit of the system, and BW and SNR are the bandwidth and signal-to-noise ratio of the signal. Due to the fact that the SNR cannot be indefinitely increased to increase the capacity of the system, interest has shifted towards receiver systems with a wider channel bandwidth, such as the UWB and LTE. A wideband receiver front-end is defined loosely in this work as a receiver front-end that can receive signals from a wide radio frequency band. The RF band is defined to be so wide that the use of a single LC resonator is not practical. However, the instantaneous band, i.e. the channel baseband bandwidth, can either be wide or narrow. The UWB and the SDR, and CR concepts which utilize wideband RF front-ends are the targeted systems covered in this thesis.

2.2.1 Ultrawideband

Ultrawideband began as a military application in the 1960s [20], but it was not until 2002, when the Federal Communications Commission (FCC) allocated frequency range of 3.1 to 10.6 GHz to be available for UWB applications [21], that modern UWB research began. This spectral allocation initiated a widespread interest in the utilization of this new frequency resource [20–25]. The UWB is based on an under-lay technique where the radio system utilizes a very wide spectrum range that potentially includes other primary systems, as shown in Fig. 2.3. The transmitted power in UWB is spread across such a wide bandwidth that the spectral power density (-41.25 dBm/MHz) at any given narrow instantaneous band becomes negligible for the narrowband primary systems.

There have been two major approaches to the technical implementation of a radio utilizing this spectra. Namely, the multiband orthogo-

nal frequency-division multiplexing (MB-OFDM) UWB and the impulse-response ultrawideband (IR-UWB). The IR-UWB approach offers simple transmitter (TX) implementation that mandates the use of a complex, correlator-type, rake receiver [24, 26] to exploit the multipath summation of the UWB signal. The MB-OFDM UWB on the other hand takes advantage of the multipath phenomenon and offers good spectral efficiency [21]. However, the implementation of the radio hardware is more complex due to the frequency hopping, the number of supported bands, and the overall bandwidth of the RF parts. The circuits presented in this thesis are intended for the MB-OFDM UWB, which is also referred to as WiMedia UWB after the standardization proposal [27, 28]. They were designed in 2006 and 2007, when UWB was an important research topic. The UWB did not gain momentum in the industry and its research has diminished over the years.

MB-OFDM UWB by WiMedia Alliance was designed to enable wireless high-data-rate connectivity with a range up to 10 meters and data rate of 110 Mbps [27]. The data rate could be increased up to 1024 Mbps with a shorter range and better channel conditions. With such performance, it was envisioned that it would replace the connection cables between consumer electronics, personal computers, and mobile handsets. Also, it was seen as being capable of providing wireless high-definition video connectivity. The band allocation of the WiMedia UWB is shown in Fig. 2.3. The standard divides the 7.5 GHz frequency band into 14 bands with a bandwidth of 528 MHz and 5 band groups (BGs). Support for the band group 1 is mandatory, while the other band groups are optional [28].

The wide operational band of the UWB poses stringent co-existence challenges to the radio circuitry. One of the toughest imaginable co-existence environments for the radio would be in a mobile device where it would experience severe interference from several cellular and wireless systems simultaneously, as depicted in Fig. 2.3. The systems depicted in Fig. 2.3 have been derived from [29–33]. The transmit powers of the cellular systems are as high as +33 dBm (GSM), and even though these systems are located out-of-band, the remaining power after preselect filtering can cause intermodulation products to fall in-band in the receiver. This fact makes the out-of-band linearity requirements of the front-end strict. For narrowband intermodulation interference on top the UWB channel, some of the sub-carriers of the orthogonal frequency-division multiplexing (OFDM) signal could be nulled [27], and thus the

interference would be tolerable as long as it does not desensitize the receiver chain. However, the Evolved Universal Terrestrial Radio Access (E-UTRA) (LTE) and 802.11a standards operate at frequencies that are in-band blockers for the UWB radio (BG1 and BG2), and for such use cases, the only option is to use another band group available in the specification. As can be seen from Fig. 2.3, the higher frequency bands would be less congested and the relative bandwidth of the RF parts is also smaller, thus making the implementation easier in that sense. However, the high operating frequency increases the path loss of the signal and implementing the radio hardware is not a trivial task due to limitations of the integration technology at the higher frequencies. This work includes a UWB receiver targeted for the BG1 and BG3 frequencies, which is presented in Chapter 3, with comparisons to other similar works.

2.2.2 Software-defined radio and cognitive radio - the future trends

Motivation

Mobile handsets have evolved from single-system phones into the highly complex smartphones of today. While in the 1990s the radio system was assembled from a single radio chain, the current multi-system radios used by smartphones are highly parallel. Still, with the current solution, many of the systems (cellular, WiFi, GPS) have dedicated antennas, pre-select filters, inputs and outputs, and radio hardware operating on different bands. For example, the current multi-system radio platform typically includes one signal path for a GSM/WCDMA/LTE cellular systems, a second one for WLAN and Bluetooth systems, and a third path for a separate Global Positioning System (GPS) receiver [34]. With the launch of the long term evolution (LTE) technology, more and more bands need to be supported by the manufacturers (23 frequency division duplexing (FDD) and 11 time division duplexing (TDD) bands [31]), and this trend will continue with the adaptation of the long term evolution advanced (LTE-A) and carrier-aggregation (CA) technologies. Furthermore, government regulatory bodies currently force manufactures to build variants that are suitable only to a specific area. All this is driving up the implementation complexity and cost of the end-product. It is of great interest for the industry and the academia to find solutions that lower the circuit complexity, simplify the design, and increase the re-usability of the radio hardware

such that the implementation time and cost are reduced.

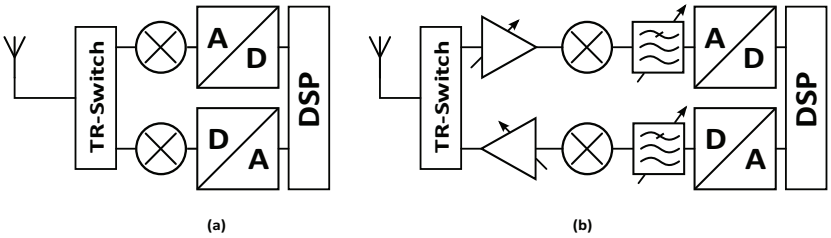


Figure 2.4. (a) Ideal SDR architecture. (b) Extremely reconfigurable approach.

Software-defined radio

The original idea of SDR was outlined by Joseph Mitola in 1995 [35], where he described a hardware system made up of a multi-band antenna, an RF conversion stage, wideband analog-to-digital (AD) and digital-to-analog (DA) converters, and general-purpose digital signal processing (DSP), as is depicted in Fig. 2.4a. By his own admission, he questioned wether such an ideal will ever be implemented, which is also evident from the demonstration presented in [36]. The bandwidth and dynamic range requirements proposed in [36] for direct SDR call for AD and DA converters with a 10 GHz sampling rate and a 16 effective number of bits (ENOB) [37, 38]. A converter with such requirements would consume about 1 kW [36] using the current technology, which clearly is not feasible for any kind of mobile solution operating on battery power. Instead of an ideal implementation, a more practical topology is shown in Fig. 2.4b, where a reconfigurable wideband LNA, power amplifier (PA), mixers, and reconfigurable baseband (BB) filtering are used together with the AD and DA converters. This kind of approach allows the sampling rate and dynamic range requirements of the converters to be scaled down to values where physical implementation is more practical. In fact, this is where the objectives and trends of the telecommunication industry and the SDR ideal begin to approach each other. Therefore, SDR research has concentrated on taking advantage of the CMOS scaling trend in radio building block design and trying to come up with solutions that serve the objectives of reconfigurability, re-usability, and digital-like operation [35, 39]. Although this kind of approach does not meet the criteria of the pure SDR proposed by Mitola, it suits the criteria for resource-sharing radios that are emerging in practical implementations [40–42].

SDR will most likely come as part of an evolution of the current multi-mode multi-band radios. As such, the requirements for the radio are set

Table 2.1. Existing communication standards and derived software-defined radio receiver user equipment requirements.

System	GSM [29]	UMTS [30][1]	WLANac [32][2]	E-UTRA [31][2]	SDR[5]
Band(s) (GHz)	0.9, 1.9	2.1-2.2	2.4, 5.2-5.7	0.7-2.7	0.7-2.7
Sens. (dBm)	-102	-117 (-92)[3]	-82	-104.7 (-94.7)[3]	-102
Ch. BW (MHz)	0.2	5	20/40/80/160	1.4-20	0.2-160
Duplex Type	TDD	FDD	TDD	TDD+FDD	TDD+FDD
Duplex (MHz)	na	45-400	na	30-400	30-400
TX power (dBm)	+33	+24	+20	+23	+33
Blocking (dBm)	0[4] @80MHz	-15 @85MHz	-63 @20MHz	-15 @85MHz	0 @80MHz

[1] Band I [2] Also MIMO [3] Coding gain (25/10dB) [43]
[4] Also -23/26 dBm@3MHz [5] Sum of the toughest requirements

by the cellular and wireless connectivity standards that it needs to fulfill. Certain critical RF problems are exacerbated in software radio due to its building blocks or, more accurately, the lack thereof. The simplification or even complete removal of the pre-select and duplex filters has serious consequences for the linearity requirements of the receiver, as can be seen in Table 2.1. The table collects the user equipment receiver requirements for the current wireless systems that are typically present in smartphones. The presented SDR requirements represent a collection of the most stringent requirements for each standard. However, the SDR radio would still have to fulfill all of the requirements of each standard as a whole.

Although GSM will eventually be phased out, a modern SDR radio still needs to support its requirements for a long time. This constitutes a bottleneck for SDR implementation, since the sensitivity, lower channel bandwidth, transmit power, and out-of-band blocking requirements are set by the GSM as can be seen in Table 2.1. The sensitivity requirement of -102 dBm is higher than for Universal Mobile Telecommunications System (UMTS) (WCDMA) or E-UTRA (LTE), but the coding gain of these

systems allows for a much lower SNR at the reception threshold and, in practice, the GSM requirement is the most stringent. Moreover, smartphone manufacturers often require much better sensitivity and blocking performance than what is specified in the standard. For example, a sensitivity target for a modern GSM system can be as low as -110 dBm [44]. The blocking requirement of 0 dBm at 80 MHz offset for the GSM system is also much higher than for the other systems. Also, the GSM specification also requires the receiver to withstand a -23 dBm blocker 3 MHz offset. These specifications translate into very strict linearity and LO phase noise requirements for the receiver, as will be studied in Section 2.3.4. The RF band requirement of 0.7-2.7 GHz, which is set by E-UTRA, is not a major obstacle and can be fulfilled with the wideband receiver architectures that are covered in this thesis. The baseband channel bandwidth should scale from 200 kHz (GSM) to 160 MHz (WLANac) in SDR. This also implies that the AD converter should be highly flexible in terms of sampling rate, resolution, and power consumption.

The interfaces of the SDR also pose stringent implementation requirements. The software radio architecture should support TDD and FDD duplexing with transmit powers ranging from +20 to +33 dBm. Since the antenna interface is wideband, a fixed frequency-selective duplex filtering cannot be applied to attenuate the TX power visible at the RX input. Instead, the antenna interface could make use of common-mode-to-differential isolation phenomenon of a transformer to achieve a wideband, SDR-compliant input. A TX-to-RX isolation better than -55 dB has been reported for a single-ended autotransformer implementation [45] and -70 dB for a differential implementation [46]. Another potential enabling circuit element is the N-path filter, which can fulfill many of the reconfigurability and linearity requirements in the SDR architecture. N-path filters are a central research area in this thesis and will be looked at more closely in Chapters 4 and 5.

Cognitive radio

In most countries, large portions of the spectrum are at present permanently and inefficiently allocated to systems with low real use. With the acknowledgement of the economic value of this scarce resource, there is a strong motivation to make use of this spectrum. Cognitive radio (CR) seeks to improve the spectrum utilization by detecting unoccupied bands (referred to as *holes* or *white spaces*) and opportunistically adapting to

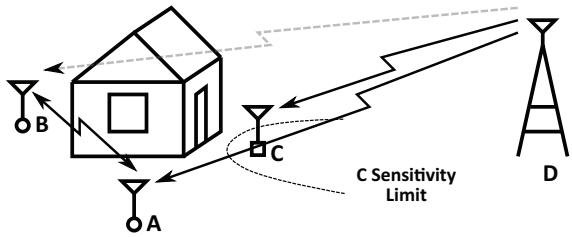


Figure 2.5. Shadowing problem and cooperation in cognitive radio.

them, while avoiding interference with primary users [47, 48]. Spectrum detection via sensing is the key feature that makes the CR possible. Sensing can be accomplished by matched filtering, energy detection, or cyclostationary detection [49]. The first two are sub-optimal options due to non-coherent signal processing, while cyclostationary detection allows the radio to extract signal features, such as the sinusoidal carrier, symbol rate, and modulation type [50]. However, implementing the feature detector requires more hardware than the simpler detectors [51].

Meeting the sensitivity requirements of the narrowband primary radios with a wideband CR receiver is already difficult. In order to avoid the *hidden terminal* or *shadowing* problem in CR, the sensitivity requirement must be raised by 30-40 dB because the CR does not have a direct measurement of the channel between the primary service RX and TX. The shadowing problem is depicted in Fig. 2.5, where A and B are CR terminals and C and D are the RX and TX of a primary service in this example. If D transmits on the primary user channel while the C receives close to the sensitivity limit of the system, then A and B must have much better sensitivity so that they can also see D. It can happen that one of the CR terminals, B in this case, is behind an obstacle or in a bad multi-path fading position where it cannot detect the primary user. In such a case, A could provide B with its spectrum-sensing results and thereby avoid colliding with the primary system. This type of collaborative sensing has been shown to reduce the probability of primary user interference from over 90% to below 10% [50], and the detection improves as the CR network size increases. To accomplish this, the CR terminals need some type of control channel to communicate. The channel could be implemented as a dedicated frequency channel or as an UWB underlay channel [52]. Whatever type of implementation is used, it must be guaranteed not to interfere with any primary systems.

CR and SDR share many properties from the perspective of the receiver

front-end. One similarity is the minimal pre-select filtering, which makes it possible for the RX to see the entire hostile spectrum from the antenna, and thus enables harsh interference and blocking scenarios. Also, both cognitive radio and SDR have wide reception bands, while the instantaneous channel bandwidth can be narrow in both. The duplex filtering dilemma also applies to CR if it uses FDD duplexing, which is the case with SDR. Finally the LO tuning range, phase-noise, and spurious requirements are stringent for both, again, because there is no pre-select filtering. The more demanding LO requirements stem from the higher blocker levels at the mixer where they down convert the LO phase noise and spurious tones.

There are two fundamental differences between SDR and cognitive radio. First, the SDR targets certain standards and their allocated bands, which are known a priori, whereas cognitive radio has no such knowledge (or very little). Where SDR can circumvent interference scenarios with careful frequency planning, CR suffers more from unknown interference [53]. Second, cognitive radio must sense and detect the unoccupied channels that it intends to use, while SDR has no such requirement. In order to avoid the hidden terminal problem described above, CR should be able to detect the primary users with an SNR of -20 to -30 dB. If the receiver uses feature extraction (cyclostationary detection) to perform the detection, then, knowing that non-linearity preserves the features in intermodulation components, the linearity requirement must be 20 to 30 dB larger to avoid false detection [53]. In particular, the LNA even-order distortion becomes a much more serious problem in wideband CR receivers, because it folds the intermodulation product to DC, where it may pass through the mixers and corrupt detection [54].

2.3 Receiver design parameters

There are several design parameters that play an important role in receiver circuit analysis, design, and verification. The intent of the author is to discuss the fundamental design parameters in a receiver and, where applicable, highlight the differences, or new requirements between the classical narrowband systems and wideband/SDR systems. More details related to the characteristics of wireless communication systems can be found in, for example, [15, 55–59].

2.3.1 Input matching

With RF receivers, the RF interfaces need to be matched to a specific impedance level for two main reasons. One reason has to do with the performance of the possible off-chip components, like baluns, duplexers, antennas, or pre-select filters. The components are designed to match a certain reference impedance level, typically 50 Ω, and a large deviation from this can lead to performance degradation in the form of a change in the component characteristics. The second reason is due to signal reflections in the off-chip transmission lines. When the distance between the source and the load, for example the antenna and LNA, is larger than $\lambda/4$, then reflections can occur [60]. The λ is the wavelength of the signal in question. For example, for a signal at 3 GHz and a substrate relative permittivity of 4, this distance becomes 12.5 mm, which can easily be reached on a printed circuit board (PCB) scale.

Input matching is defined with the help of scattering parameters (S-parameters) as

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}, \tag{2.2}$$

where Z_0 is the characteristic (source) impedance and Z_{in} is the input impedance of the circuit. The return loss is $20log|S_{11}|$. The amount of power lost due to mismatch is defined as

$$L_{att} = 10log[1 - |S_{11}|^2]. \tag{2.3}$$

The relationship between the return loss and the power loss due to mismatch are presented in Fig. 2.6. In Fig. 2.6a, matching circles of -3, -6, and -10 dB are printed on Smith's impedance chart to illustrate how the area of allowed matching impedances becomes reduced as better matching is required. In Fig. 2.6b, the power loss due to mismatch starts to increase rapidly after the -10 dB threshold, which is typically specified for RF circuits [61]. Also, for wideband antennas a return loss requirement of -6 dB is typically targeted [62], which means that the losses due to antenna mismatch can dictate the losses of the system input, and thus degrade the system noise figure. This is an important aspect for the circuit designer to keep in mind.

2.3.2 Gain

For a general amplifier structure, shown in Fig. 2.7, we can derive several gain definitions [60]. For receivers, the signal is typically processed in the

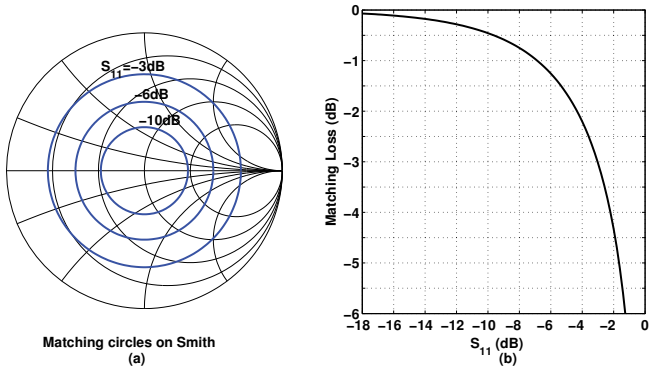


Figure 2.6. (a) Matching circles on Smith's diagram for $S_{11} = -10, -6, and -3dB$. (b) Matching power loss against matching.

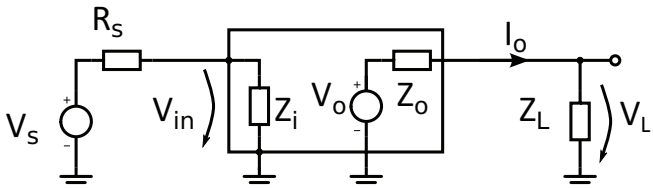


Figure 2.7. General amplifier stage with input and output impedances. For a wideband amplifier, the input is assumed to be perfectly matched; thus, $V_{in} = V_S/2$.

voltage domain after the first circuit block on the IC, and therefore, we can assume the output of the receiver to be matched to the characteristic impedance of the measurement device (or simulation). The power gain of the circuit is defined as

$$G_p = \frac{P_L}{P_{in}} = \frac{V_{L,rms}^2/Z_L}{V_{in,rms}^2/Z_{in}}. \tag{2.4}$$

For wideband circuits, matching can vary considerably over the reception bandwidth, and therefore the inserted power can also change. The transducer gain,

$$G_t = \frac{P_L}{P_{S,av}} = \frac{V_{L,rms}^2/Z_L}{V_{S,rms}^2/4R_S}, \tag{2.5}$$

assumes a perfect input match and describes how much of the available source power is delivered to the load. For wideband receivers, the latter definition is useful since it depicts the system gain response shape instead of the intrinsic response. Similarly, for voltage signals the voltage gain is defined as

$$A_v = \frac{V_L}{V_{in}} = \frac{I_o Z_L}{V_{in}}. \tag{2.6}$$

In narrowband applications where the matching of the input is good, we can assume that $R_s = Z_{in}$, and therefore the voltage gain is a good figure-of-merit. However, for wideband receivers $R_s \neq Z_{in}$ and using A_v will

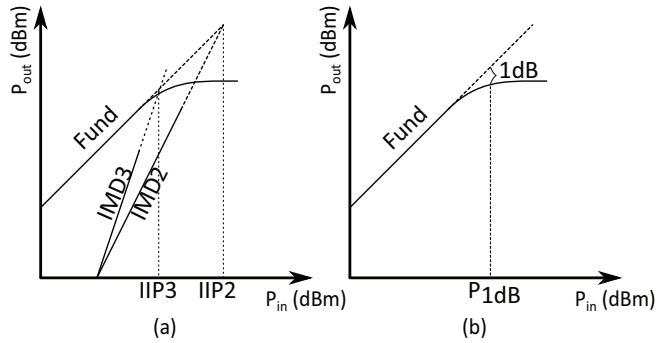


Figure 2.8. Graphical determination of (a) IIP2 and IIP3, and (b) input compression point.

result in deformed frequency responses. A more suitable figure-of-merit is the insertion gain A_i [63], which is expressed as

$$A_i = \frac{V_L}{V_S/2} = \frac{2V_L}{V_S} = \frac{2I_o Z_L}{V_S}. \tag{2.7}$$

Similar to the transducer gain, the insertion gain measures only the variation in the output signal.

2.3.3 Linearity

Different linearity measures of the receiver describe how well the system tolerates large signals and how these interfering signals are folded onto the reception channel. As the level of the interferers increases, they degrade the SNR of the weak desired signal and throughput of the system. With DCRs, typical linearity measures are the input-referred second- and third-order intercept points, IIP2 and IIP3, respectively, as well as the input compression point (ICP). Linearity is an important aspect of receiver design whose role has increased. Previously, with only a few radio systems, the focus of most academic studies was on minimizing the noise figure [61]. Now, since more radio systems are implemented on the same radio platform, the interference environment has become more hostile. Also, with manufacturers wanting to minimize cost, the use of external filtering components needs to be minimized. These issues have resulted in more linearity-oriented receiver research on how to improve the blocker, desensitization, and intermodulation performance of the receiver.

Intermodulation

With the IIP2 test, two sinusoidal test tones at ω_1 and ω_2 result in second-order intermodulation distortion (IMD2) at the frequencies $|\omega_1 \pm \omega_2|$ [64]. The behavior of the test signals and the IMD2 product is depicted in Fig.

2.8 (a) in relation to the test signal power P_{in}. As the test tone power increases, the Fund and IMD2 lines intersect. This imaginary, second-order, input-referred intercept point can be expressed as

$$IIP2 = P_1 + P_2 - (IMD2 - G), \tag{2.8}$$

where P_1 and P_2 are test signal powers (dBm) at the input, IMD2 is the intermodulation product at the output, and G is the small-signal gain of the system at the frequency of the intermodulation beat.

The IIP3 is determined in similar fashion as the IIP2. The two test tones result in third-order intermodulation distortion (IMD3) at the frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ [64]. As the test tone power increases, the increase in IMD3 is ideally threefold in dB. The IIP3 can be calculated from

$$IIP3 = P_1 + \frac{1}{2}P_2 - \frac{1}{2}(IMD3 - G), \tag{2.9}$$

where P_1 is the test signal power closer to the IMD3 frequency and P_2 is the other test signal power (dBm) at the input.

Compression and desensitization

There is an upper bound where the system can amplify the signal with constant gain. As the input power increases, the output power stops increasing in the same increments as the input power. This phenomenon is called compression. A -1 dB input compression point (ICP or P_{1dB}) can be defined graphically, as shown in Fig. 2.8b. It is the point where the extrapolated output power line and actual output power differ by 1 dB.

The reduction of sensitivity in the presence of a single large interferer is called desensitization [65]. Desensitization by blocker can be attributed to two separate mechanisms. First, it can be attributed to the gain compression in the desired weak signal due to third-order nonlinearity. As the power of the large blocking signal increases, a similar drop in the output power of the weak signal can be observed as for the compression test depicted in Fig. 2.8b. The second mechanism is due to second-order nonlinearity, which results in low-frequency noise to up-convert to the desired signal frequency, thus degrading the SNR [65].

2.3.4 Noise

The sensitivity determines the minimum signal level at which the received signal can be detected with sufficient quality, i.e., sufficiently low bit error ratio (BER). The sensitivity can be determined as

$$S = -174dBm + 10log(BW) + SNR_{min} + NF, \tag{2.10}$$

where -174 dBm is the k_BT noise power of the source at 290 K, BW is the channel bandwidth, SNR_{min} is the minimum signal-to-noise ratio, and NF the noise figure of the receiver. SNR_{min} is determined by the minimum BER, the used modulation, the coding gain, and, in the case of spread-spectrum systems, also the spreading gain (SG) [66].

The noise figure of a circuit can be determined from the noise factor equation, which is expressed as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{e_{n,out}^2}{4k_BT \cdot BW \cdot R_S(\frac{V_{out}}{V_S})^2}, \tag{2.11}$$

where $e_{n,out}$ is the output rms noise voltage, k_B is the Boltzmann's constant, T is the temperature in Kelvins, BW is the bandwidth, R_S is the source resistance, and V_{out} and V_S are the output and source voltages, respectively.

A quick way to approximate the noise performance of an RF block, for example in measurements, is to use the spot noise figure, which can be defined as

$$SNF = N_{out} - P_{out} + P_{in,av} + 174dBm, \tag{2.12}$$

where N_{out} and P_{out} are the output noise (dBm/Hz) and power of the block and $P_{in,av}$ is the available power from the source (dBm/Hz). For a DCR, another 3 dB is subtracted from the SNF due to the fact that noise folds to the baseband from both sides of the LO frequency [67].

Reciprocal mixing and blocker noise figure

Reciprocal mixing occurs when a blocker enters the down-conversion mixer and mixes with the LO phase noise that is at the frequency of the blocker. This phenomenon is depicted in Fig. 2.9. Note that even if the receiver linearity is sufficient to withstand the blocker and the baseband filtering is sufficient to avoid desensitization, reciprocal mixing can limit the performance of the receiver. The LO phase noise (PN) and blocker power (P_B) that reaches the mixer define the blocker noise figure (BNF) due to reciprocal mixing alone to be

$$BNF = 174dBm + PN + P_B. \tag{2.13}$$

For example, the specification for the GSM receiver requires that a blocker level of -26 dBm should be tolerated at a 3 MHz offset from the carrier [29]. If a phase noise of -140 dBc/Hz is assumed [45], then the blocker noise figure becomes 8 dB due to reciprocal mixing alone. The BNF should be substantially smaller than the receiver NF in order not to degrade

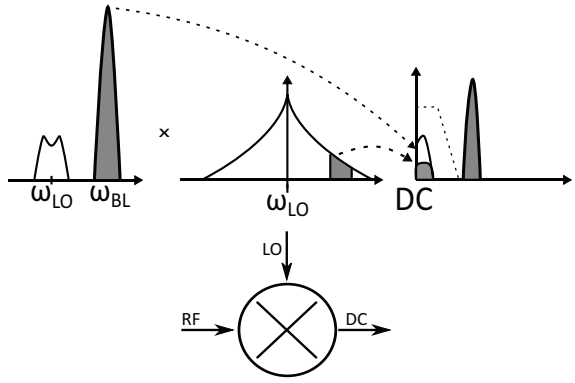


Figure 2.9. Reciprocal mixing with a blocker signal, which causes LO phase noise and spurious tones down-conversion to baseband.

the overall NF. Reciprocal mixing sets stringent requirements for the LO generated by the cellular systems, as is evident from the example. The pre-select filtering in these systems alleviate the out-of-band PN requirement, but for SDR and other wideband receivers the out-of-band blockers pose a serious challenge due to the lack of filtering. In SDR receivers, the synthesizer requirements are further exacerbated by the wide frequency synthesizing range.

3. Wideband low-noise amplifier design

The subject of this chapter is the design of wideband, low-noise amplifiers (LNA) for mobile applications. General wideband design principles are introduced and different wideband LNA topologies are presented. Then feedback LNA design trade-offs are discussed. A review and comparison of wideband buffer topologies is also presented. For the purpose of comparison, simulation examples are shown for the feedback LNA topology and wideband buffers. Experimental results of implemented wideband LNA circuits are presented at the end of this chapter. Original work by the author includes a dual-loop feedback LNA and the use of a UWB LNA in the IF stage of a 60-GHz receiver.

3.1 General wideband design principles

A narrowband LNA is usually the first circuit block in a conventional receiver. Its purpose is to provide sufficient matching for the input interface so that the preceding block (filter, switch, antenna) behaves as expected. The LNA also sets the minimum noise figure and sensitivity of the receiver and suppresses the noise of the following circuit blocks with its gain. The gain of the LNA has to be designed such that the following blocks are not overloaded and so that the dynamic range is sufficient. Even though the overall in-band linearity of the receiver is usually set by the circuit blocks following the LNA due to the gain, the linearity of the LNA has to be high enough to withstand large out-of-band blockers that may corrupt reception. The bandwidth of the LNA should cover the targeted system band, but, at the same time, the load should be designed to be as selective as possible to suppress out-of-band blockers. In LNA design, all of these design goals should be met simultaneously with minimal power and area consumption.

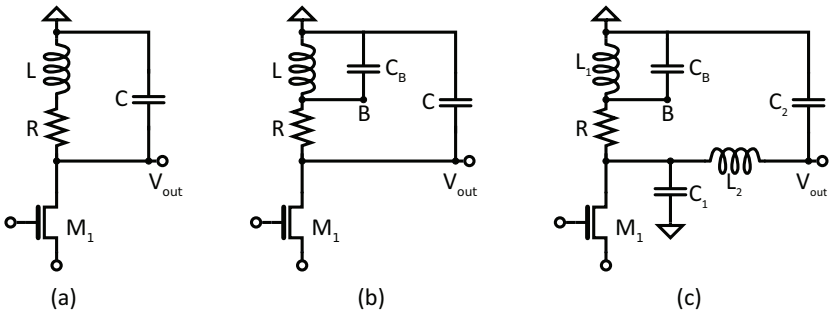


Figure 3.1. (a) A shunt-peaked load. (b) A bridged-shunt-peaked load. (c) A bridged-shunt-series-peaked load.

The design goals for wideband, low-noise amplifiers are the same as for their conventional narrowband counterparts. However, there are two main design issues that are characteristic of wideband LNA design. These are the input matching bandwidth and the load bandwidth. The input matching strategy differs from narrowband realization because the bandwidth of an input resonator that performs matching in the narrowband case is insufficient in the wideband case. With inductively-degenerated common-source (IDCS) LNA, more reactive components with high Q-values can be added to form LC-ladder-filter matching that has a wider bandwidth [68–71]. This leads to the utilization of many inductors and capacitors; this requires a large die area, and hence, such a solution is not practical for low-cost driven applications. Hence, circuit topologies that have a wider natural matching bandwidth are employed in wideband design. These are discussed in more detail in Section 3.2. The second differentiating property is the instantaneous gain bandwidth. Narrowband LNAs typically use LC resonators for their well-known advantages [72]. For a wideband LNA, several parallel low-Q LC resonators may be used if the bandwidth is sufficient [73]. Again, this leads to large implementation area since each LC resonator requires its own inductor. A purely resistive load is one alternative with a large bandwidth. The load has a bandwidth that is limited by the RC constant of the load node, i.e. the parasitics determine the high-frequency corner of the load. This generally limits the use of a resistive load to applications below 2 GHz. Also, a high resistance value should be used to minimize the noise penalty; this can potentially lead to voltage head-room and linearity problems.

For high-frequency applications, a shunt-peaked load, shown in Fig. 3.1a, is a better option for realizing the wideband load and is often utilized in wideband LNA designs [69, 74–76]. The shunt-peaked load con-

sists of a series-connected inductor and resistor together with a shunt capacitor [77, 78]. Compared to a resistive load with some arbitrary –3-dB RC bandwidth, the shunt-peaked load can extend this bandwidth by a factor of 1.85 [78]. Moreover, the resistance value of the shunt-peaked load is smaller than for a purely resistive load, which results in larger voltage headroom and smaller noise contribution from the resistor. A bridged-shunt-peaked load, shown in Fig. 3.1b, can be formed by connecting a capacitor from the middle node between the inductor and the resistor to the ground [78]. This type of load does not increase the bandwidth but achieves the same bandwidth with a smaller inductor value, and thus, smaller die area. Since all monolithic devices incur a parasitic capacitance, even a plain shunt-peaked load is in practice a bridged-shunt-peaked load. The parasitic loading of the middle node between the inductor and the resistor can be so high that no additional capacitor value is needed. Additionally, by utilizing an additional inductor to form a bridged-shunt-series peaked load network, as shown in Fig. 3.1c, an even higher bandwidth extension ratio of 4 can be achieved [78]. Bandwidth extension techniques are discussed in more detail in [77–80].

3.2 Wideband LNA topologies

The transistor can be connected in multiple ways to form a transconductor that is suitable for application as a low-noise amplifier. The possible topologies have been extensively covered elsewhere [81]. Of the possible topologies, the IDCS LNA is best suited for narrowband applications and therefore not discussed in this thesis. IDCS LNA analysis and implementations targeted for wider bandwidths can be found, for example, in [59, 69, 70, 82]. The three most common LNA topologies used in wideband applications are common-gate (CG) LNA, common-source common-gate (CSCG) LNA, and common-source feedback LNA, which are presented in Fig. 3.2a, 3.2c, and 3.2d, respectively.

One of the simplest wideband topologies is the CG LNA (Fig. 3.2a), where input matching is achieved by scaling the transistor transconductance g_m (M_1) to be inversely proportional to the desired matching impedance ($Z_{in} = 1/g_m$) [73, 83, 84]. The CG LNA has many desirable properties for use as a broadband LNA. Matching is relatively easy to achieve over a wide band, it has low power consumption, excellent third-order linearity, and good reverse isolation and it is not very sensitive to pro-

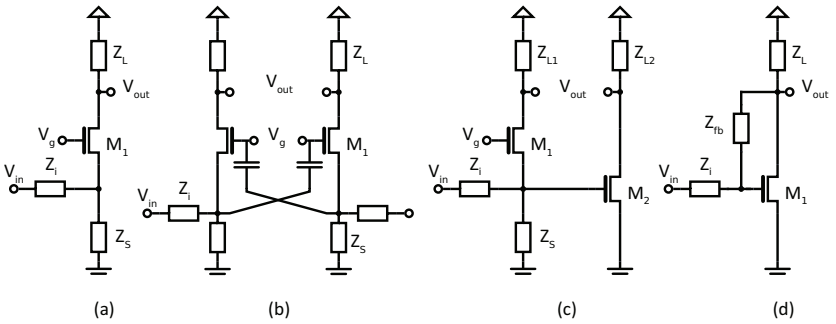


Figure 3.2. Wideband LNA topologies depicting (a) common-gate, (b) cross-coupled common-gate, (c) common-gate common-source, and (d) general common-source feedback topogies.

cess, voltage, or temperature variations (PVT). Also, the minimal number of stacked devices make it suitable for use in modern low-supply voltage processes. The limitations of the CG LNA topology are that it has a high noise figure (limit≈3 dB) and limited effective transconductance. To achieve wide matching bandwidth with CG LNA, the value of the series input impedance Z_i (input bond wire and series DC blocking capacitor) should be minimized over the reception band. Likewise, the input bonding pad capacitance and biasing source inductor (depicted with Z_s) further limit the matching bandwidth that can be achieved [59]. However, these reactive components can provide voltage gain for the input signal, which improves the noise performance. To improve the noise performance of the CG, a g_m-boosting technique can be applied [85]. An amplifying and inverting stage is connected from the source to the gate of the CG transistor, which reduces the noise excess factor (NEF) of the LNA by a factor of 1+A, where A is the gain of the boosting device [85]. In a differential LNA this can be accomplished by cross-coupling a capacitor from the negative branch source node to the positive branch gate node [86], as is shown in Fig. 3.2b. Differential CG LNAs using this technique have demonstrated noise figures of 2.5–3 dB [86, 87]. The differential CG LNAs have also been proven to have excellent IIP2 performance [87].

The noise-canceling CGCS LNA topology (Fig. 3.2c) was first introduced by Bruccoleri [88]. In this topology, the noise current of the matching device (CG M_1) creates noise voltages with opposite signs at the input and at the output of the CG stage. When the input noise voltage is amplified by the CS (M_2) amplifier, it is inverted simultaneously and the resulting noise voltages at the output nodes are, due to the CG stage, in phase and equal in magnitude with appropriate design values. At the same time,

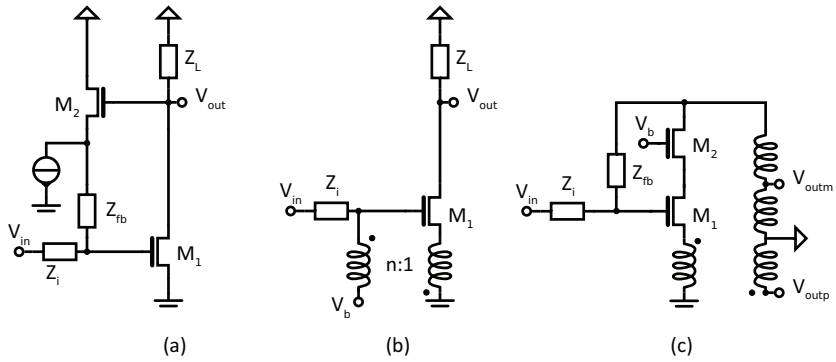


Figure 3.3. Wideband LNA feedback topologies depicting (a) source-follower, (b) transformer, and (c) dual-loop feedback topogies.

the signal voltages are equal and opposite in phase. With a combining network (e.g. a differential amplifier) the common-mode noise components can be rejected and the opposing signal components re-enforced. Additionally, the same noise-canceling phenomenon cancels the CG stage distortion currents as well. This implies that the CS stage determines the noise and linearity performance for this topology [89]. To achieve good noise and linearity performance, the power consumption of the CS stage has to be made high compared to the CG LNA. The CGCS topology is well suited for wideband LNAs since it has a low die area, wide matching and gain bandwidth, and a competitive NF. Additionally, the circuit naturally performs unbalanced-balanced conversion, which implies that a single-ended input can be utilized. When differential input signaling can be avoided, the PCB and antenna design are relaxed considerably. The IIP2 performance of this topology seems to be highly dependent on the details of the implementation: Values between +10 and +60 dBm have been reported [40, 89, 90]. The IIP3 performance of the CGCS topology has been improved to +10.5 dBm by differential implementation in [91].

An alternative method for implementing a wideband LNA is the negative-feedback amplifier (Fig. 3.2d). The use of feedback results in numerous benefits for broadband amplification, including a low implementation area and design stability against PVT variations. The ability to trade off between feedback factor and forward gain to achieve matching at the input is another beneficial trait of the feedback topology. Generally, by omitting Z_i in Fig. 3.2c, the input impedance of the feedback amplifier is $Z_{in} \approx Z_{fb}/A_v$, where A_v is the open-loop voltage gain of the amplifier. In practical circuits the feedback can be realized in many different ways, which affects the performance of the LNA. Since the plain resistor feed-

back (Z_{fb}) over a single stage results in a rather power-hungry realization (M_1 has to be sized for a high g_m), a source follower (SF) stage, shown in Fig. 3.3a, has been used to implement the feedback [92–94]. The resulting topology achieves a good NF (1.9-2.6 dB) and a very small die size due to lack of inductors. However, the additional stage increases power consumption, whereas the high voltage gain in the feedforward path degrades the overall linearity performance of the topology. Another topology results when the feedback is placed over a 2-stage amplifier [76]. Similar to the source follower feedback topology, the gain, noise, and size of the implementation are very competitive while the power consumption and linearity are moderate. This approach has two major drawbacks: The global feedback introduces potential instability, which has to be carefully considered during design, and the direct resistor feedback over the LNA reduces the reverse isolation of the topology. An interesting way to implement the feedback is to utilize a transformer to couple the signal back [75]. This topology is shown in Fig. 3.3b. The topology achieves a good NF, bandwidth, matching, and low power consumption [75]. The resulting IC implementation requires a large die area due to the high-quality transformer, whereas the linearity performance is moderate. Moreover, the design of the LNA requires the use and understanding of electromagnetic field simulators since foundry kits do not normally include transformers. Finally, the LNA can combine the aforementioned feedback topologies to form a dual- or multi-loop feedback topology [95, 96], [I], one that uses a resistive and transformer feedbacks, as presented in Fig. 3.3c. The measurements of the LNA [95] show an NF of 2.5 dB, an IIP3 of +12 dBm, and a gain of 12 dB, which make it highly competitive despite the complex topology.

A qualitative comparison of the different properties of the CG, differential CG, CGCS, source-follower feedback (FB SF), reactive feedback (FB Reac.), and dual-loop feedback (DL FB) is presented in Table 3.1. As a conclusion it can be said that none of the possible topologies is a clear winner with properties far superior to others. Each of them has its own advantages and disadvantages, and the final choice for the proper LNA topology depends on the application and its requirements. For example, simple CG or SF feedback LNAs may be the best choices available for a low power, low area application, while for other applications these may be quickly discarded as too noisy or non-linear topologies.

Table 3.1. Qualitative comparison of wideband LNA topologies.

	CG	Diff CG	CGCS	FB SF	FB Reac.	FB DL
Gain	+	+	+ -	+ -	+ -	+ +
Bandwidth	+	+	+	+	+ +	+ +
NF	- -	+	+ +	+	+ +	+ +
Linearity	+ +	+ +	-*	-	+ -	+
Matching	+ +	+ +	+ +	+	+ +	+ +
DC power	+ +	+	-	-	+ +	+
Reverse isolation	+ +	+ +	+	+	+	-
Area	+ +	+ +	+ +	+ +	-	+ -

* Contradicting IIP2 results exist [40, 89].

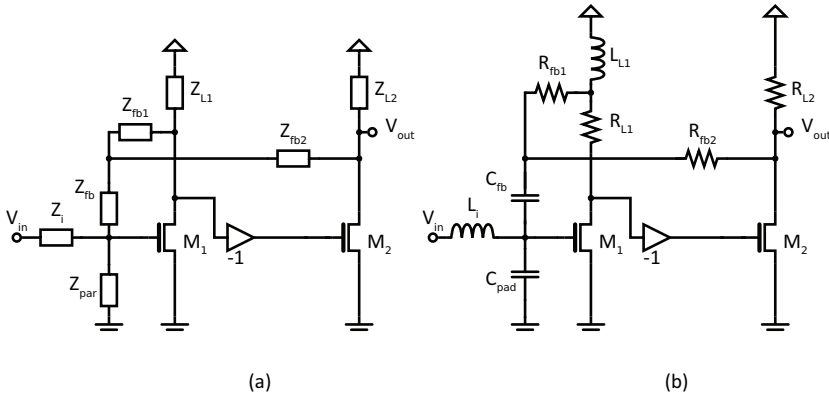


Figure 3.4. Wideband feedback LNA topology with (a) general impedances, (b) components used in trade-off comparison.

3.2.1 2-stage, dual-loop feedback LNA design trade-offs

The dual-loop topology, which was introduced in last section, was chosen as a candidate topology for a wideband UWB LNA presented in [I]. This topology is an original product of this thesis. The configuration of the topology is shown in Fig. 3.4a, where the dual-loop feedback is formed by connecting a feedback from the first (Z_{fb1}) and second (Z_{fb2}) stage loads to the input through a common feedback impedance, Z_{fb}. The use of the feedback from the second stage load means that a larger feedback impedance value can be used, which translates into a lower noise contribution. However, the global feedback can potentially cause instability in an actual differential implementation where the signal inversion, depicted in Fig. 3.4a, is done by crossing the differential signal paths. This works for a differential excitation, but for a common-mode signal the feedback remains positive. Therefore, the common-mode loop gain must be designed

Table 3.2. Simulation parameters for three cases.

	Case I	Case II	Case III
$I_{DC1}/g_{m,M1}$ (mA/mS)	5.5/64	9.6/105	7.4/71
$I_{DC2}/g_{m,M2}$ (mA/mS)	2.8/38	2.6/22	4.1/38
R_{L1} (Ω)	100	60	100
L_{L1} (nH)	2	3	2.5
R_{L2} (Ω)	300	300	200
R_{fb1} (Ω)	1k	1k	1k
R_{fb2} (Ω)	1k	1k	1k
C_{fb} (pF)	0.5	0.6	0.6

to be less than one in order to guarantee stability. The negative feedback from the first stage load acts as a negative feedback for differential and common-mode signals and helps to alleviate the common-mode stability problem. Another option is to introduce a common-mode rejection into the amplifier. Also, with two feedbacks it is possible to balance their individual effects on the LNA and to have more trade-off freedom during the design phase.

The actual implemented topology is presented in Fig. 3.4b. The single-ended schematic contains the chosen passive components used in this trade-off study. In addition to these components, the actual implementation in [I] has a DC blocking capacitor at the input and cascode transistors in each stage to increase gain. However, these differences do not change the basic behavior of the LNA, and therefore, this study is relevant to the actual implementation as well. Compared to the general topology (Fig. 3.4a), the feedback from the first stage load (R_{fb1}) is connected to the shunt-peak inductor in the topology (Fig. 3.4b). This results in a behavior where the first stage feedback affects the high-frequency matching and gain more, because the inductor is a high impedance at those frequencies. The second stage has no peaking and thus a drooping gain response due to the RC pole (parasitic C not shown). The second stage feedback has more affect on the low-frequency matching and gain.

The trade-off study was performed for three different cases. The values used in the study are presented in Table 3.2. In case I, gain bandwidth, power, and noise performance were given priority. In case II, linearity performance was preferred over other metrics, and in case III an overall compromise was sought between the first two cases. The input inductor, L_i, modeled the input bond wire and its value in these simulations was 1

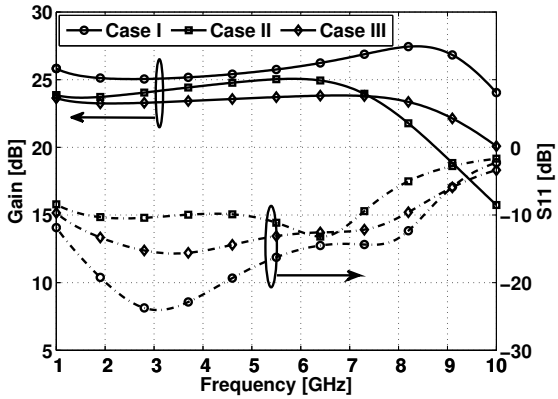


Figure 3.5. Wideband, dual-loop feedback LNA gain and matching comparison for three different parameter cases.

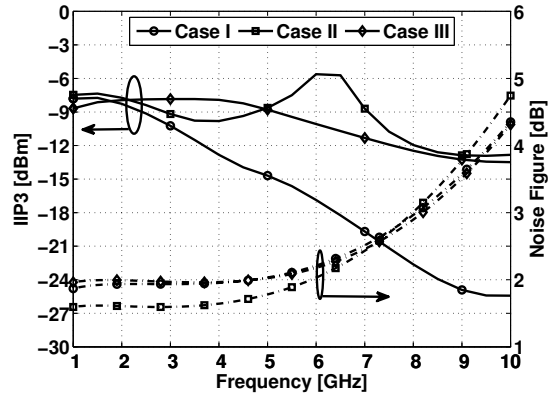


Figure 3.6. Wideband, dual-loop feedback LNA noise figure and third-order intercept point comparison for three different parameter cases.

nH, and the value of the pad capacitor, C_{pad}, was 300 fF. In addition, 50 fF capacitors were placed at the loads of each stage to reflect the post-layout extraction of interconnects and devices. The self-resonance frequency of the inductor was also modeled so that it followed the inductor size and was approximately the same as that exhibited by monolithic inductors for a modern CMOS process.

The simulated gain response and matching for the three cases are shown in Fig. 3.5, and the simulated NF and IIP3 are shown in Fig. 3.6. The first case had a wide gain bandwidth ranging from 1 to 10 GHz with a 2 dB gain variation over the band. The peaked gain response was due to the low value of the load inductor, L_{L1} (2 nH). The achieved matching bandwidth was also wide and extended from 1 to 8.5 GHz. The input inductor (1 nH) and the input capacitance of the pad and the input transistor limited

the matching at higher frequencies. The NF for case I at 1–4 GHz was 1.9 dB and increased to 3.6 dB at 9 GHz, which was due to the large size of the input transistor. The problem with the first case was the IIP3 performance, which degraded over the gain bandwidth from –8 dBm at 1 GHz to –25 dBm at 9 GHz.

For the second case, the current consumption and transconductance were increased to improve the linearity and noise performance, while the transconductance of the second stage was decreased. The decreased transconductance together with the higher load inductance (3 nH) resulted in a reduced gain bandwidth, as can be seen in Fig. 3.5. The linearity was improved so that it was better than –13 dBm while the NF was 1.6 dB at 3 GHz, but achieving sufficient input matching was challenging. In the last case, the design parameters were chosen so that they fell in between those set for the first two cases such that an acceptable all-around performance could be obtained. As can be seen from Fig. 3.5 flat gain response and matching were achieved between 1–8 GHz. Simultaneously, an NF of 2–3 dB was achieved and the simulated IIP3 was from –8 to –13 dBm between 1–8 GHz. The results of the last case served as a starting point for the implementation in [I].

This topology achieves good all-around performance in these simulations; however, the circuit design using this topology is complex due to its interdependent nature. Changing a single parameter produces changes in all of the design metrics at the same time, so the designer needs to understand these relationships in order to succeed in the design. The basic design procedure for the dual-loop feedback topology is given below to give insight into the design procedure with this type of LNA. Further analysis of the dual-loop feedback input matching conducted by the author can also be found in [97].

- Design the LNA without the feedbacks for sufficient gain and bandwidth. The linearity and noise performance can be traded by altering the transconductance ratios of the first and second stage. The bandwidth should be slightly higher than what is targeted as it will be reduced when the feedbacks are put in place.

- Insert the feedback over the first stage and size for matching. Seek to accomplish majority of the matching with this feedback to ensure stability.

- Insert the second feedback and adjust the value of the feedback to fulfill matching criterion. This gives a starting point for the LNA design.

3.3 Wideband buffers

With wideband receivers, a buffer is often needed to isolate the LNA from the mixer and to increase the load impedance of the LNA. This guarantees a higher voltage gain for the LNA, and therefore, the noise of the mixer is also suppressed more compared to an unbuffered case. Another reason for using a mixer-buffer is the bandwidth of the interface. By designing a low impedance mixer interface, the gain variation over a multi-gigahertz band can also be small even without inductors. When an active mixer is used, the low impedance interface also minimizes the voltage gain before the mixer switches and thereby improves the linearity performance of the active mixer.

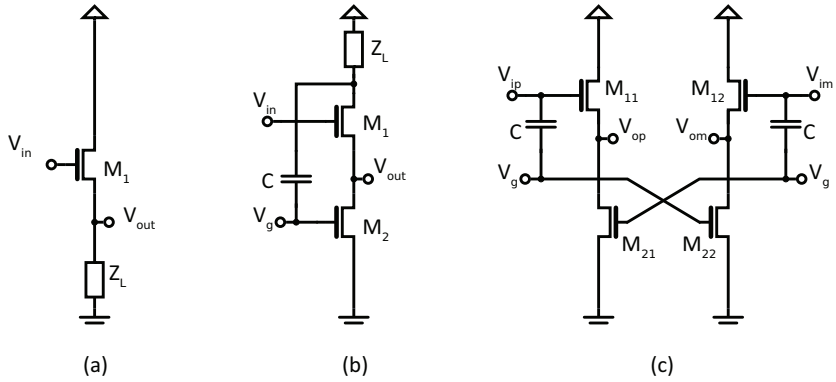


Figure 3.7. Wideband buffers utilizing (a) common-drain (voltage follower), (b) capacitively-coupled, common-drain common-source, and (c) differential common-drain common-source topologies.

In Fig. 3.7, three different buffer topologies are shown. A conventional common-drain (source follower, Topo I) buffer is depicted in Fig. 3.7a, a capacitively coupled common-drain common-source (CDCS, Topo II) buffer is depicted in Fig. 3.7b, and a differential, capacitively cross-coupled, common-drain common-source buffer (CCC-CDCS, Topo III) is depicted in Fig. 3.7c. The CDCS buffer topology has been used in the receivers in publications [I-II], whereas the CCC-CDCS buffer topology has been used in the receivers in publications [III-IV].

A simulation comparison is provided for a differential implementation

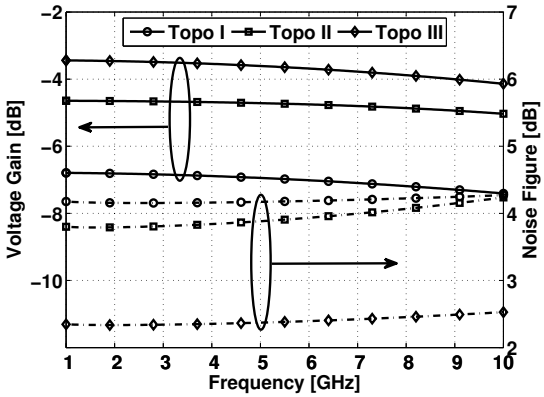


Figure 3.8. Wideband buffer topology comparison for gain and noise figure.

of each to gain an insight into their differences. The driven load was a 100 Ω resistor and a 100 pF capacitor (not shown in the figures). The buffers were biased so that the single branch DC current was 2 mA. An NMOS transistor was used as a current source for the source-follower in Fig. 3.7a. The voltage gain and noise figure results are shown in Fig. 3.8 and the IIP3 results in Fig. 3.9 for a 50Ω source. Of the three topologies, the simple source-follower topology provided the lowest gain, the highest noise figure, and the lowest IIP3 result for the simulation band of 1–10 GHz. By using the capacitor to couple a signal from the CD transistor drain to the CS transistor gate (Fig. 3.7b), the gain of the buffer can be increased by 2 dB. While the noise performance is slightly better, the additional noise introduced by the Z_L (100Ω) keeps the NF of the CDCS buffer close to the plain CD buffer. The third topology can be used for differential signaling. With the CCC-CDCS buffer, the input signal is directly cross-coupled to the CS transistor from the opposing signal branch, as is depicted in Fig. 3.7c. This further improves the gain and avoids the additional load resistor of the CDCS buffer. This has two impacts: The NF is 1.5 dB better, and because the voltage headroom is improved (VDD 1.2 V), the linearity is also better (IIP3 23 dBm). Another beneficial property of the CCC-CDCS buffer is its common-mode rejection. Common-mode signals are effectively cancelled by the summation of the output currents of the CD and CS transistors in opposing phases. The rejection is limited by mismatches, and in this case it was better than 40 dB for a Monte Carlo of 1000 runs.

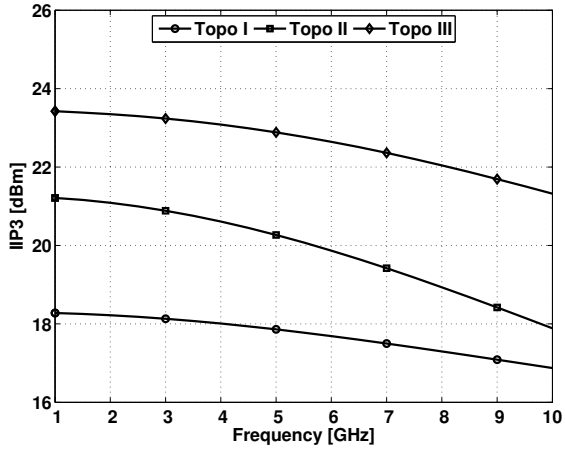


Figure 3.9. Wideband buffer topology comparison for third-order intercept point.

3.4 Experimental results

3.4.1 LNA for an UWB receiver

The block diagram of the dual-band UWB receiver implemented in [I] is presented in Fig. 3.10. The receiver consists of a dual-band front-end, a WiMedia-compliant [27] baseband filter, a fast-hopping synthesizer, and a dual-scheme LO quadrature generation. The 5^{th}-order Chebyshev baseband filter has a bandwidth of 240 MHz and adjustable gain control together with offset-compensating, current-steering DA converters. The synthesizer uses three parallel, phase-locked loop (PLL) units to achieve good spectral purity and a high hopping speed (< 3 ns). Quadrature signals are generated for the mixers either with a divide-by-2 (DIV2) divider or an active polyphase filter (APPF), which reduce the required synthesizer frequency range. Transconductance elements, implemented with inverter-like structures, replace the resistors of a conventional passive PPF in the APPF. The APPF will be further discussed in Chapter 6.

One problem with the wide UWB reception band is that it leads to degraded out-of-band filtering of the interfering signals, and thus, the linearity requirements of the receiver become more stringent. Despite preselect filtering, these interferers (GSM900, 2.4-GHz WLAN, etc.) can corrupt UWB reception due to intermodulation or desensitization. This situation is relaxed with BG3 because of the less hostile spectrum. For the BG1 LNA, an LC-notch filter is used to attenuate interferers around 2.4 GHz, as is shown in Fig. 3.11. The filter utilizes a cross-coupled pair to

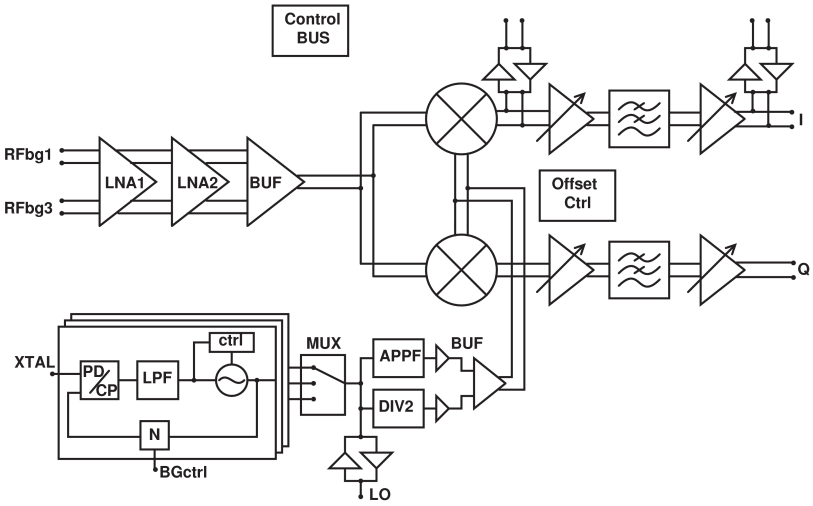


Figure 3.10. UWB receiver block diagram [I].

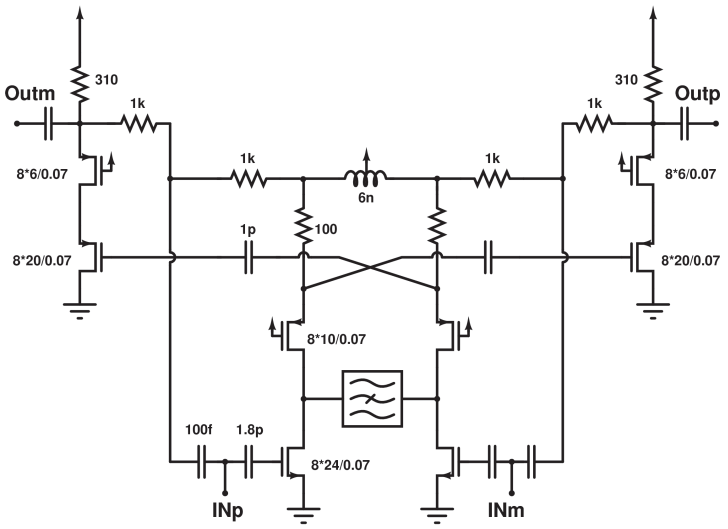


Figure 3.11. LNA schematic for band group 1 [I].

enhance the Q-value of the LC notch.

In order to achieve wideband matching for an UWB LNA, either a feedback path or a parallel common-gate stage can be used [76,98]. The topology that we have chosen for the BG1 LNA relies on two feedbacks from the first stage and second stage loads, as is depicted in Fig. 3.11, to provide sufficient matching, even with the additional parasitic capacitance and series inductance introduced by the packaging. Furthermore, with the double feedback the degeneration inductor could be avoided when compared to the IDCS LNA topology. This saves die area and makes the layout easier to draw for the differential amplifier. We use a cascode configura-

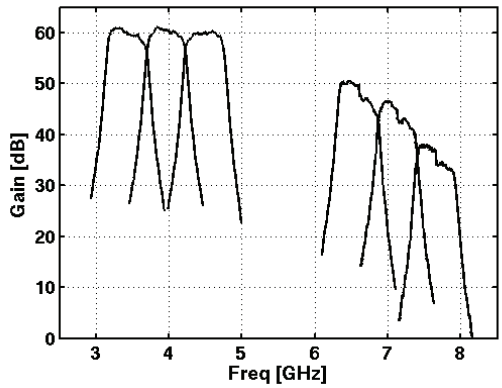


Figure 3.12. Receiver gain response for BG1 and BG3 [I].

tion in the amplifier stages to achieve a higher gain. In the first stage a shunt-peaked load provides gain peaking, while the resistive load of the second stage cancels the peaking, and thus only one inductor is needed in this topology. The differential signal paths must be crossed so that negative feedback is maintained, because both amplifier stages invert the signal phase. The amplifier has a positive feedback for common-mode signals; this can potentially cause instability. The modest gain and small feedback factor from the second stage output ensure stability for this amplifier implementation. Furthermore, the second feedback is used as an additional feedback to gain another degree of freedom in design while the feedback from first stage accomplishes most of the matching. All of the resistors in the LNA were made tunable with switches so that process variations could be covered. The BG3 LNA also uses a two-stage feedback topology similar to the one shown in Fig. 3.11. The design trade-offs of this topology were discussed in Section 3.2.1.

We use enhanced source-follower buffers similar to the ones presented in [74] and Fig. 3.7b after the LNAs to drive the active mixers. The BG3 buffer uses an additional inductor in the load to provide additional gain peaking. The output signals of the buffers are directly connected to the sources of the double-balanced, Gilbert-cell mixer switches [99]. This low-impedance node suffers less from the parasitic capacitance of the two signal paths, resulting in a near-flat frequency response.

The chip was fabricated using a standard 1.2-V, 65-nm CMOS process and it was bonded directly onto a PCB. The active area of the design is 2.7 mm^2, which includes the reported blocks, the control bus, the decoupling capacitance, and the interconnect wiring.

Table 3.3. Measurement Results [I].

	Band Group 1		
RF Band (MHz)	3168-3696	3696-4224	4224-4752
Gain max/min (dB)	58.5/24.5	59/25	59/25
NF (dB)	6.2	6.1	5.7
S11< -10dB (GHz)	2.6 - 4.9		
ICP (dBm)	-29.5		
In-band IIP2 (dBm)	18.5		
In-band IIP3 (dBm)	-16		
Blocker IIP3[1](dBm)	-6		
Freq. Hopping (ns)	< 3		
Technology	65nm CMOS		
Active Area (mm^2)	2.7		
Supply (V)	1.2		
Idc (mA)	35 (RF) + 60 (BB) + 42 (LO) = 137		

[1] Measured with 2420 and 880 MHz signals at a 15 dB power difference of the input test tones.

The measured frequency responses of the receiver in the BG1 and BG3 mode are presented in Fig. 3.12. The gain has been measured from the baseband filter output, and thus the effects of the RF front-end, baseband filter, and LO generation are all visible in the figure. The gain level of the first sub-band in BG3 is already 10 dB lower than for BG1, which indicates that the LO signal amplitude is not sufficient for the mixers. This was also verified in the reception band, where the operational band of the divider and the APPF overlap. Additionally, there is a 15 dB difference in gain of the three sub-bands, which suggests that the frequency response of the LO path droops heavily. Because this kind of behavior was not visible with the BG1 measurements, it can be concluded that the APPF and LO path does not perform in a satisfactory way.

The BG1 gain of the RF front-end is 60 dB within 1 dB. The matching for the BG1 input covers a frequency range of 2.6 to 4.9 GHz with the PCB board and connectors. The measured noise figures of the receiver are 6.2, 6.1, and 5.7 dB for UWB band groups 1, 2, and 3, respectively. The rest of the measured results for BG1 are shown in Table 3.3.

A comparison of the MB-OFDM UWB radios is made in Table 3.4 for the different CMOS technology nodes. The experimental results of our receiver demonstrate a competitive performance against other state-of-the-art UWB receivers implemented with CMOS technology given the circuit

Table 3.4. Comparison of MB-OFDM UWB receivers.

Gain dB	Band GHz	NF dB	IIP3 dBm	P_{DC} mW	Area mm^2	Integrated Blocks	CMOS Tech.	Ref
37	3-5	4.1	-22	237	6.6	TRX, BB, SX	130-nm	[76]
73	3-5	8.4	-19	105	1.0[1]	TRX, BB, SX	130-nm	[73]
84	3-8	8.1	-13[2]	284	15.6	TRX, BB, ADC, SX	180-nm	[100]
24	3-8	5	5	114	0.4[1]	TRX, buf SX	65-nm	[98]
64	3-10	7.8	-17[2]	224	3.5	TRX, BB, SX	90-nm	[82]
59	3-5	6.2	-16	164	2.7	RX, BB, SX	65-nm	[I]

[1] Active area [2] Minimum gain

complexity and implemented circuit blocks in the chip. When comparing the longer line width implementations [73, 76, 100] against the shorter line width implementations [82, 98], [I] a 20% smaller averaged power consumption can be observed in favor of the smaller line widths. Similarly, the NF and die area are lower for the smaller line widths. In particular, the BG3 UWB front-ends benefit from the small line width. Also, for a more complete comparison, UWB receivers implemented with SiGe technology can be found, for example, from [69, 71, 101, 102].

3.4.2 60-GHz CMOS receiver with an on-chip ADC

The previous work on the UWB receiver presented in [I] was utilized in a 60-GHz CMOS receiver with an on-chip ADC [II]. The use of the UWB receiver together with a millimeter-wave front-end enables the implementation of a high capacity wireless connection. A block diagram of the complete receiver is shown in Fig. 3.13, where the IF amplifier is the wideband UWB LNA used in [I]. Superheterodyne architecture was used to minimize the circuit hardware operating at millimeter-wave frequencies, which reduces power consumption and layout size.

The gain of the millimeter-wave 4-stage LNA was designed to be 19 dB to suppress the noise contribution of the mixer and the succeeding circuit blocks. Additionally, the feedback matching of the IF amplifier could be

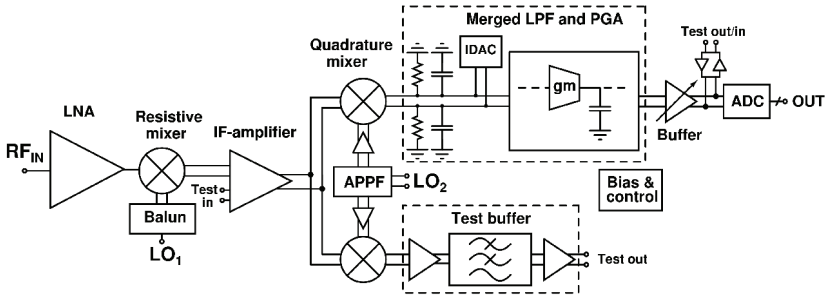


Figure 3.13. 60-GHz wideband receiver block diagram [II].

omitted in this design and therefore the noise performance was further improved. The IF amplifier uses a cascode configuration and a shunt-peaked load to guarantee wide bandwidth and sufficient IF frequency (2 to 6 GHz) for the receiver. The higher IF frequency reduces the image frequency noise folding in the superheterodyne architecture because of the millimeter-wave front-end selectivity. A separate buffer drives the double-balanced quadrature mixer, which separates the signal into I and Q paths. The quadrature signal for the mixer is generated using an active polyphase filter (APPF). The baseband filtering section is composed of a merged programmable gain amplifier (PGA) and a 5-stage gm-C Chebyshev filter prototype with pre-distorted filter coefficients in [16,103]. The -3 dB cutoff frequency of the filter is 275 MHz. A 6-bit, 600-MS/s flash ADC performs the analog-to-digital conversion and together with the baseband filter support the MB-OFDM reception described in the WiMedia standard for UWB [27].

The measured performance of the receiver is presented in Table 3.5, where it is compared to other 60-GHz front-end implementations. The experimental results demonstrate the feasibility of a broadband, single-chip, 60-GHz receiver with an ADC in deep-submicron CMOS. The wideband IF amplifier helps to achieve a low system NF and competitive gain, die size, and power consumption. The receiver compares favorably with the existing state-of-the-art, millimeter-wave front-ends given the high integration level and degree of circuit complexity. Also, to the best of the author's knowledge, this receiver is the first 60-GHz implementation that includes a front-end, an IF stage, a merged baseband filter, and an ADC on the same chip.

Table 3.5. Comparison of 60-GHz receiver front-ends.

Gain **dB**	**NF** **dB**	**ICP** **dBm**	**S_{11}** **dB**	**V_{DD}** **V**	**P_{DC}** **mW**	**Area** **mm^2**	**Integrated blocks**	**Technology**	**Ref**
40	5.0-6.7	-36	<-15	2.7	527	5.78	LNA, mix, IF amp, IF mix PLL, freq tripler	0.13-μm SiGe BiCMOS	[104]
22	5.7-8.8	-27.5	na	1.2	36	0.185[4]	LNA, polyphase filter, mix, IF mix, LO	90-nm CMOS	[105]
22.5[1]	8.4[2]	na	<-6.3	1.2	144	2.64	Antenna, LNA, mix, TIA, synthesizer	90-nm CMOS	[106]
55.5[1]	6.1-6.4[2]	-26	<-10	1.0	24	1.55	LNA, mix, VGA, buffer amp	90-nm CMOS	[107]
51	9.0	-30	<-15	na	189	3.83	LNA, mix, IF amp, IQ demodulator buffer, VCO, PLL	90-nm CMOS	[108]
25[3]	7.0[3]	-26[3]	<-30	1.5	103	0.68	LNA, mix, OOK demodulator limiter amp, VCO	90-nm CMOS	[109]
14.7	5.6	-22	na	1.2	151	0.5	LNA, mix, LO tree, freq divider	65-nm CMOS	[110]
35.5	5.6-6.5	-39	<-15	1.2	84	2.6	LNA, mix, IF mix, buffer, synthesizer, divider	65-nm CMOS	[111]
79	7.0	-38.5	<-12	1.2	198	2.8	LNA, mix, IF amp, IF mix IF IQ-gen, BB LPF+PGA, ADC	65-nm CMOS	[II]

[1] Power gain instead of voltage gain [2] DSB NF [3] LNA and mixer only [4] Active area

4. Passive mixers and N-path filters

The main purpose of a downconversion mixer is to perform a frequency translation from the RF to the IF frequency. This is accomplished by using non-linear devices, e.g. diodes or transistors, or by using a time-varying element, i.e. a switch. Also, depending on the LO signal waveform and amplitude, the mixer element can act as a current-commutating switch or as frequency multiplying element. Depending on the implementation, mixers are typically categorized as active and passive mixers. An active mixer is a mixer implementation where a bias current flows through the frequency translating device, whereas with a passive mixer there is no bias current flow through the device. In general, active mixers can provide voltage gain and use a smaller LO amplitude, while passive mixers provide lower 1/f noise corner frequency and higher linearity, but require a large LO signal. Active mixers have been conventionally conceived of as having a better noise figure, but recent advances in passive mixer implementations have demonstrated competitive noise performance [112–116].

This chapter discusses the properties and design principles of passive mixers and, in particular, the passive mixer-first receiver. General design principles and the theory of passive mixers are discussed first. Then, a design trade-off study that presents the effects of the interface impedances around the passive mixer is provided and, additionally, the effects of the switch sizing are shown. Active mixers are omitted from this thesis because of the fact that most of the mixers [III-V, VII] are passive (only the mixer in [I- II] is active). The last part of the chapter describes a passive-mixer-based circuit element, the N-path filter. The operating principle and examples of an N-path filter application are presented in Section 4.4. In this thesis, the N-path filter has been utilized in [III-V]. These circuits are presented in Chapter 5.

4.1 Passive mixer design considerations

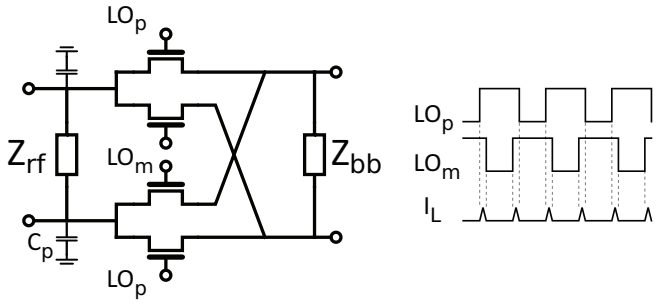


Figure 4.1. Passive mixer and LO timing diagram with overlap leakage.

The passive mixer is a widely employed mixer topology that is known for its high linearity performance and low flicker noise. Additionally, the mixer has zero DC current consumption and it occupies a very small die area. However, the passive mixer also has its drawbacks. Perhaps the most serious of the drawbacks is the mixing of interference from the odd LO harmonics. The passive mixer also incurs a signal loss, which in a typical receiver translates into a more stringent baseband noise requirement and a higher LNA gain specification. Also, due to the square-wave LO signal, the LO buffering becomes power hungry at higher frequencies.

A schematic of a balanced passive switching core with interface impedances is depicted in Fig. 4.1. If the Z_{bb} is low and the Z_{rf} is high, then the passive mixer can be conceived of as a current-commutating mixer, but when the impedances are reversed and the Z_{rf} is low and the Z_{bb} is high, the passive mixer operates as a voltage sampling mixer. In the case of the current-commutating mixer, a low baseband impedance can be provided via operational amplifier virtual ground. In either case, minimizing the passive mixer loss is critical. This can be achieved by minimizing the switch on-resistance with respect to its interfaces. Besides using large devices, using a large overdrive voltage accompanied by a square-wave switching waveform minimizes the on-resistance.

Minimizing the channel resistance of the switch also minimizes the thermal noise of the passive mixer switch [117]. However, the flicker noise of the mixer can still severely degrade the NF of the mixer in narrowband systems [118], and it is of importance since the mixer switching pair is typically the dominant source of flicker noise in a receiver [119]. The flicker noise of a transistor can be modeled using an empirical equa-

tion [120]:

$$V_{1/f}^2 = \frac{K_f I_{ds}^{af}}{C_{ox} L^2} \frac{1}{f^{ef}}, \tag{4.1}$$

where C_{ox} is the unit capacitance of oxide, K_f is a device-specific constant, L is the length of the device, and I_{ds} is the drain current of the device. The variables af and ef are the current and frequency exponents. By observing (4.1), it can be concluded that the flicker noise can be lowered by reducing the channel bias current to zero, which is the case for a passive mixer; however, in practical passive mixers a flicker noise is still present. One reason for this is the leakage current in the switching core, which is induced by the overlapping of the switches' conduction phases on the transitions, as is depicted in Fig. 4.1 [121]. Using a sharp square wave reduces the amount of flicker noise because the leakage is minimized [117, 122]. Another source of flicker noise in a passive mixer is the parasitic input capacitor, C_p, shown in Fig. 4.1. During one switching phase, the capacitor samples the noise of the baseband input through the switch and then discharges it to the opposite baseband branch during the opposite phase. This charging and discharging creates a train of spiked current pulses. The average value of the pulses causes flicker noise [117, 123]. A third flicker noise mechanism for a passive mixer is flicker noise conversion due to a blocker or any other large amplitude signal [117].

The linearity of a passive mixer is generally conceived of as excellent due to deep triode-region operation. With the current-commutation mode, the low baseband interface impedance will further improve the mixer linearity performance [124]. If a transimpedance amplifier is used to implement the low in-band baseband impedance, then an additional capacitor at the mixer output will improve linearity by reducing the load impedance level at higher frequencies. The sharp square waveform also has an important role: By maximizing the zero crossing slope, the phase modulation of the signal is minimized, which improves linearity [125]. In a direct conversion receiver, the passive mixer IIP2 and DC offsets can also be problematic. Careful and symmetrical layout and using common-centroid strategies alleviate these problems. Also, using a balanced structure in the mixer helps to mitigate IIP2 and DC-offset problems [126]. Furthermore, non-coherent LO noise is rejected as common-mode noise in a balanced structure [127] and the LO-to-RF feedthrough and substrate coupling also benefit from a balanced mixer structure [128].

Harmonic mixing also needs to be considered with passive downconversion mixers. For efficient conversion, the LO signal driving the mixer

needs to be a square wave with a large amplitude, and it therefore also has a high energy content at the odd harmonics of the LO. As was previously mentioned, the harmonic mixing folds the frequency components from the odd harmonics of the LO frequency to the desired baseband frequency, as shown in Fig. 4.2. These components can be filtered in a narrowband system by placing an LC resonator at the mixer input. However, such a resonator cannot be used in a wideband system, and therefore harmonic mixing can cause problems with interference mixing. A harmonic rejection better than 40 dB can be achieved by employing an 8-phase passive mixer [114], but in difficult interference cases the rejection should be in the order of 100 dB to avoid desensitization. This kind of requirement can be caused, for instance, by a 0 dBm interferer at the 3^{rd} or 5^{th} LO harmonic frequency at the mixer input. In such cases, an additional preselect filter can ensure proper attenuation for the LO harmonic frequencies. Harmonic rejection techniques are discussed in detail, for example, in [129–133].

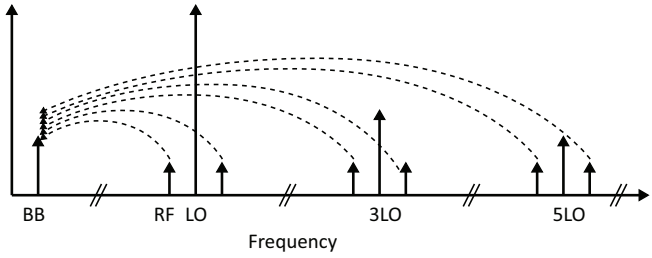


Figure 4.2. Harmonic mixing phenomenon in a passive mixer.

4.2 Passive mixer-first receiver analysis

The model for the passive mixer analysis is depicted in Fig. 4.3a, where a quadrature passive mixer is connected to a source and an ideal operational amplifier with gain A and input-referred noise $\overline{v_{n,A}^2}$. Each of the switches operates on an ideal non-overlapping LO waveform with a duty cycle of 25%, as shown in Fig. 4.3c. This means that the source only sees one baseband branch at a time and ideally there is no charge leakage from one branch to another. Due to the transparent nature of the passive mixer switches, the baseband impedance visible to the mixer, Z_L, will also be visible to the source as an up-converted version of the baseband input impedance, as depicted in Fig. 4.3b.

To calculate the input impedance of the passive mixer, we must first ac-

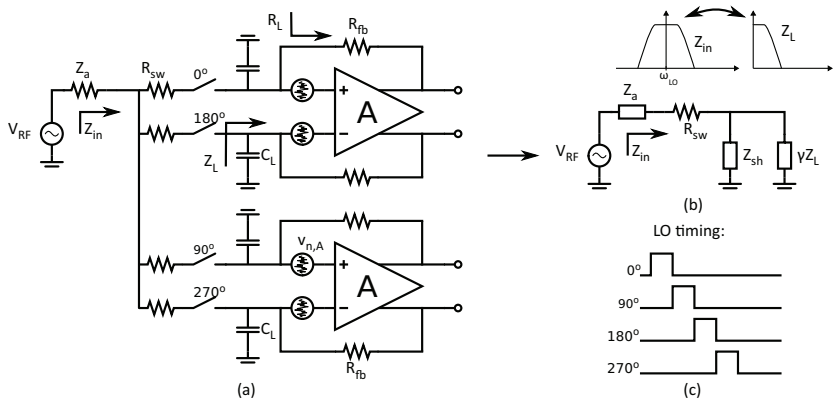


Figure 4.3. Passive mixer receiver model for analysis.

knowledge the fact that odd harmonics will also be present with a square-wave LO and will reduce the power of the desired signal. This loss can be modeled as a frequency-dependent conductance at odd harmonics [134]

$$Y_{a,n} = \frac{1}{n^2} \frac{1}{Z_a(n\omega_{LO}) + R_{sw}}, \tag{4.2}$$

where n is the harmonic index, R_{sw} is the switch resistance, and Z_a is the source impedance. These losses can be summed together to form a shunting impedance, Z_{sh}, connected to the mixer output, as shown in Fig. 4.3b:

$$Z_{sh} = \left[\sum_{n=3,5,7...}^{\infty} |Y_{a,n}| exp(j(\angle Y_{a,n} + \frac{n\pi}{2})) \right]^{-1} \tag{4.3}$$

$$= \frac{4\gamma}{1-4\gamma}(R_{sw} + Z_a) \approx 4.3(R_{sw} + Z_a) \tag{4.4}$$

When the source impedance is a frequency-invariant resistance, (4.3) can be expressed as (4.4). In (4.4), the shunting loss depends only on the switch resistance, R_{sw}, and source impedance, Z_a. The γ in (4.4) results from the 4-phase downconversion Fourier series approximation [135] and can be expressed as

$$\gamma = \frac{2}{\pi^2}. \tag{4.5}$$

The input impedance of the passive mixer receiver can now be expressed using a simple circuit model, shown in Fig. 4.3b, where the switches are described by a series resistor, R_{sw}, the conversion losses by the shunt impedance, Z_{sh}, and the baseband impedance by the γ-scaled Z_L. The simple circuit results in an input impedance that can be expressed as [134]:

$$Z_{in} = R_{sw} + \gamma Z_L || Z_{sh}. \tag{4.6}$$

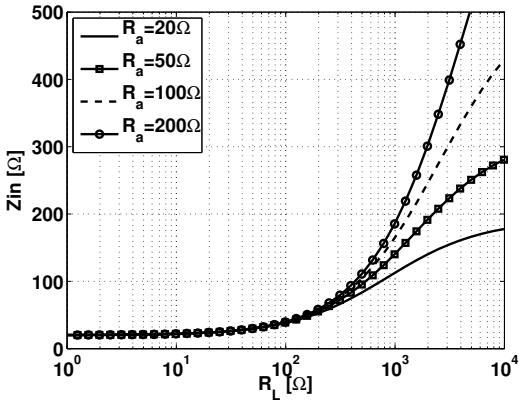


Figure 4.4. Input impedance of the passive mixer receiver analysis for different source impedances (R_a) and baseband input impedances (R_L).

For an intermediate frequency offset from the LO frequency, the impedance becomes

$$Z_{in}(\omega_{LO}+\omega_{IF}) = R_{sw} + \frac{\gamma R_L || R_{sh}}{1+j\omega_{IF}C_L(\gamma R_L||R_{sh})}, \tag{4.7}$$

where the reactive impedance caused by the baseband filtering capacitor, C_L, has been taken into account. The baseband input impedance at the zero frequency can be calculated with the help of the Miller-effect:

$$R_L = \frac{R_{fb}}{1+A}. \tag{4.8}$$

The input impedance of the receiver has been plotted in Fig. 4.4 for different source and baseband input impedance values. The switch resistance, R_{sw}, and the amplifier gain, A, have been set to 20 Ω and 40 dB, respectively, in these simulations. The figure shows that low feedback resistance, R_{fb}, determines the input impedance for this topology by shunting the parasitic impedance, Z_{sh}, according to (4.6). In this situation, the input impedance is solely determined by the switch resistance, (4.6). When the feedback resistance is increased up to 100 $k\Omega$, the input impedance is determined by the parallel connection of γR_L and Z_{sh}, since their values are of the same magnitude. According to (4.6), the shunt impedance, Z_{sh}, starts to dominate the input impedance for R_L values beyond 1 $k\Omega$. In this case, the level of the source impedance value plays an important role in the input impedance of the passive mixer receiver, as can be seen in Fig. 4.4. However, in practical cases the input impedance is limited to lower values by the parasitics of the input interface (e.g. bonding pad and input series inductance).

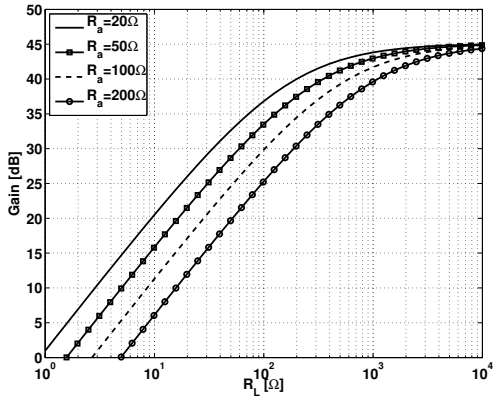


Figure 4.5. In-band gain of the passive mixer receiver for different source impedances (R_a) and baseband input impedances (R_L).

Next, we can determine the gain of the passive mixer-first receiver at the amplifier output. The current induced by the input impedance can be calculated by using (4.6). The frequency translation from RF to the baseband can be mapped from the Fourier-series of the LO signal, and it results in a coefficient of $\pi/2\sqrt{2}$ for a 25% duty cycle signal. The gain for a differential output at an IF frequency can now be expressed as

$$G_{IF}(\omega_{IF}) = \frac{\frac{-\pi}{\sqrt{2}}A}{1+\frac{Z_a+R_{sw}}{R_{sh}||\gamma Z_L}}, \tag{4.9}$$

where A is the open-loop gain of the amplifier. The behavior of the gain has been plotted in Fig. 4.5 against the source R_a and baseband R_L resistance values. Ideally, the gain obtained via this topology can be defined by $R_{fb}/(Z_a+R_{sw})$, which explains the behavior visible at lower R_L values. According to (4.9), with higher R_L values the gain saturation occurs at 45 dB instead of an ideal result of 46 dB due to the harmonic re-radiation. When these results are compared against steady-state circuit simulations, the equations prove numerically accurate as long as a sufficient number of harmonics are used in the simulations.

In order to calculate the noise performance of the receiver, the different noise sources must first be identified. When examining Fig. 4.3a, four sources of noise can be identified: The source impedance itself, the switch resistance, the feedback resistance, and the input-referred noise of the amplifier. Additionally, the noise caused by the virtual shunt impedance, Z_{sh}, needs to be added parallel to the baseband impedance noise sources in Fig. 4.3a. In this topology, the Miller effect allows the feedback resistance

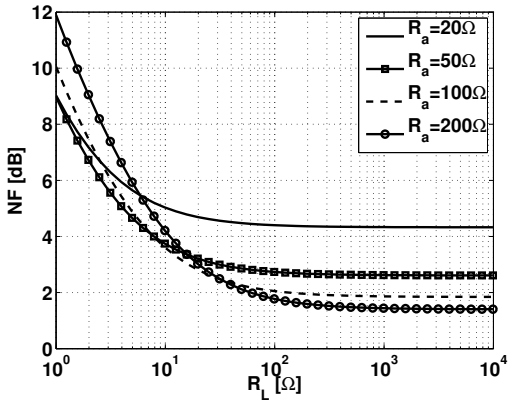


Figure 4.6. Noise figure of the passive mixer receiver analysis for different source impedances (R_a) and baseband input impedances (R_L).

to be made larger by a factor proportional to the gain of the amplifier, and simultaneously the noise from the feedback resistor is suppressed by the same factor. The noise figure of the receiver can now be expressed as follows [134]:

$$F = 1 + \frac{R_{sw}}{R_a} + \frac{Z_{sh}}{R_a}\left(\frac{R_a + R_{sw}}{Z_{sh}}\right)^2 + \gamma\frac{R_{fb}}{R_a}\left(\frac{R_a + R_{sw}}{\gamma R_{fb}}\right)^2 + \gamma\frac{\overline{v_{n,A}^2}}{4k_BTR_a}\left(\frac{R_a + R_{sw}}{\gamma R_{fb}} + \frac{R_a + R_{sw} + Z_{sh}}{Z_{sh}}\right)^2. \tag{4.10}$$

The second and third terms in (4.10) depict the noise contributions from the switch and shunt resistances. The fourth and fifth terms represent the noise contributions of the feedback resistance and the amplifier. The noise figure of the receiver compared to the different source and baseband resistance values is shown in Fig. 4.6. The switch resistance is 20 Ω, the gain is 40 dB, and the amplifier input-referred noise is 500 $pV/\sqrt{Hz}$ in these calculations. It is clear that choosing a low source and feedback resistance (low R_L) is detrimental to the noise performance of the receiver. On the other hand, increasing the feedback resistance beyond 10 $k\Omega$ ($R_L = 100\ \Omega$) has only a small impact on the NF. When the baseband input resistance, R_L, is sufficiently high, the noise figure is determined by the relationship between the source and switch resistances. Making the source resistance large (e.g. over 100 Ω) compared to the switch resistance has a beneficial effect on the noise performance, and the calculation suggests that a NF of less than 2 dB can be achieved with a high source impedance. However, the highest achievable source impedance is limited by the input parasitics, as was previously mentioned. Similarly, there is a limit of

a minimum switch resistance that improves the noise performance. Increasing the device's dimensions beyond this limit causes more parasitic losses than the decreasing series resistance can outweigh. This will be evident in the trade-off study in the next section.

4.3 Passive mixer-first receiver design trade-offs

In the previous section, the analysis revealed important aspects about designing a passive mixer in a receiver. However, the linearity of the receiver was not analyzed and the effect of the switch non-idealities was not addressed. In this section, a trade-off study from [V] is presented, where the ideal switches have been replaced by transistors using an RF large-signal model (PSP) from a 65-nm CMOS process. The study aims to show how the interface impedances and the switch size of the passive mixer should be chosen to give best performance in terms of noise, linearity, and die size. The simulation model used in the trade-off study consists of a balanced input, a quadrature passive mixer, and an ideal operational amplifier model. This model is identical to the analysis model presented in Fig. 4.3a except that it has a balanced input. However, the obtained results are valid for both the single-ended input and the balanced input. Values for the simulation are chosen such that they reflect an actual implementation and are identical to the values used in the analysis of Section 4.2. The input-referred noise source for the baseband amplifier has a value of 500 $pV/\sqrt{Hz}$, the amplifier gain is 40 dB, and the switch resistance in one simulation case is 20 Ω. The common-mode voltage (CM) of the switches is set to half of the supply voltage and the capacitor value, C_L, is scaled such that a –3-dB baseband bandwidth is maintained at 10 MHz in all simulation cases. To capture the variation in RF performance over a wide range, LO center frequencies of 1 and 3 GHz were used in all simulations.

Figure 4.7 shows how the minimum noise figure and the optimal source (antenna) resistance behave in relation to different design factors. The minimum noise figure simulation clearly confirms the analysis findings presented in Fig. 4.6: It is highly beneficial to select a baseband input resistance, R_L, that is sufficiently high (high R_{fb}). This partially results from the fact that less noise is being injected into the baseband amplifier input by the R_{fb} and partially from the fact that there are smaller losses inside the mixer. The smaller losses result from the switch resistance

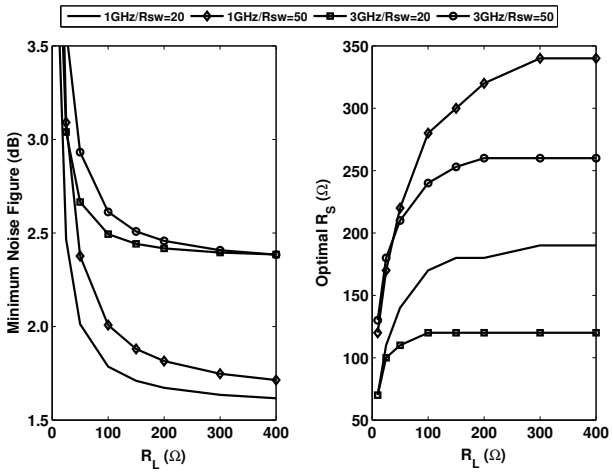


Figure 4.7. Minimum noise figure and the corresponding optimum source resistance, R_S, compared to the baseband input resistance, R_L. Four different switch resistance, R_{SW}, and LO frequency cases are shown in both figures [V].

being smaller in relation to a higher baseband input resistance R_L. Furthermore, the switch resistance (simulation with 20 and 50 Ω) has only a small effect on the noise at high R_L values, as depicted by the results. The RF frequency has a clear and expected effect on the noise, i.e. the capacitances of the switch degrade the high frequency noise performance. Compared to the analysis results, there is a clear discrepancy of 0.7 dB in the NF result at a higher frequency (3 GHz) due to switch capacitances, but otherwise the analysis and simulation results are in good agreement. In Fig. 4.7, the optimal source resistance, corresponding to each minimum noise figure value, suggests that the optimal source resistance follows the baseband input resistance value. However, there is significant variation in the optimal R_S value across the LO frequency and the switch size. Smaller switch sizes (higher R_{SW}) result in less parasitic capacitance and, thus, higher source values (250 and 340 Ω) can be obtained. For the larger switch sizes, the optimal value for the source resistance is 120 and 190 Ω at 1- and 3-GHz LO frequencies, respectively. In practical cases, package parasitics further load the mixer input and, therefore, a lower optimal source resistance value would be expected. Moreover, the choice of the R_S is always a compromise between the optimal resistance values over the operating frequency range.

The mixer linearity was studied via blocker input compression point (blocker ICP) simulations, where the power of the blocking signal was increased until the wanted small in-band signal gain decreased by 1 dB.

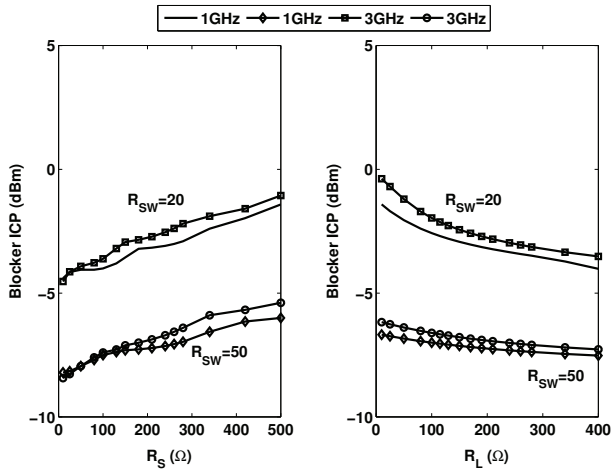


Figure 4.8. Blocker input compression point for varying R_S ($R_L = 200\Omega$) and R_L ($R_S = 200\Omega$) values at four different switch resistance and LO frequency combinations. The test blocker is located at a 50 MHz offset from the LO [V].

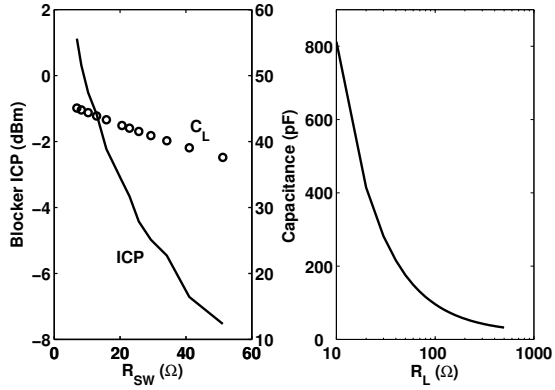


Figure 4.9. Blocker input compression and corresponding baseband filtering capacitor value for varying switch resistance. The test blocker is located at a 50 MHz offset from the LO (1 GHz). Additionally, to give perspective, baseband capacitor variation is shown agains the baseband input resistance. The –3 dB bandwidth at the baseband input is fixed at 10 MHz in all cases [V].

The results, performed for R_L=200 Ω and R_S= 200 Ω, are presented in Fig. 4.8. The simulation with fixed R_L=200 Ω shows that the linearity of the receiver is optimized by using large switches (R_{SW}=20 Ω). Choosing a higher source impedance also improves the linearity since the blocker power is rejected more effectively at the input. The simulation with fixed R_S=200 Ω shows again that large switches are beneficial. However, the linearity is degraded as the load impedance is increased. The increase in R_L results in a smaller capacitor to be seen by the source, which is due to the scaling of the filtering capacitor, C_L, to maintain a constant

bandwidth. The blocker power values depicted in the simulation results are the values that are actually inserted into the receiver, i.e., part of the power is also rejected by the mismatch between high source and low load impedance at the blocker frequency.

Finally, to demonstrate how the linearity and the filtering capacitor are related to the switch size, a simulation depicted in Fig. 4.9 was conducted. The result shows that the linearity is greatly affected by the switch resistance, while the change in the filtering capacitor, C_L, is under 10 pF. For comparison, the same dependency of the capacitor value is plotted against the baseband input impedance value on the right side of Fig. 4.9. Clearly, low R_L values result in an implementation where the die size is dictated by the capacitor.

As an original contribution of this thesis, we can draw the following conclusions from this trade-off study:

- The switch resistance, R_{SW}, should be as small as possible, given the limitations of the LO power consumption and operating frequency range.

- A high source impedance, R_S, level is preferable for the best noise and linearity performance. However, this is often limited by practical issues such as input parasitics and antenna implementation.

- A high load impedance, R_L, results in lower noise and a smaller layout size with a small penalty in linearity performance.

4.4 N-path filters

The N-path filtering concept, shown in Fig. 4.10, was first conceived in the 1960s by Franks and Sandberg [136]. They described a time-varying network utilizing linear filtering and modulators between the input and the output. With the N-path filter, the clock period is divided into N phases, which each have their own branch in the filter network, as is depicted in Fig. 4.10. These phases are summed together at the output to form the N-path filter. Although the targeted frequencies were relatively low at the time, Franks and Sandberg identified five key properties of N-path filters: 1) Periodic filtering properties occur around clock harmonics; 2) narrowband band-pass and band-stop filters can be synthesized without induc-

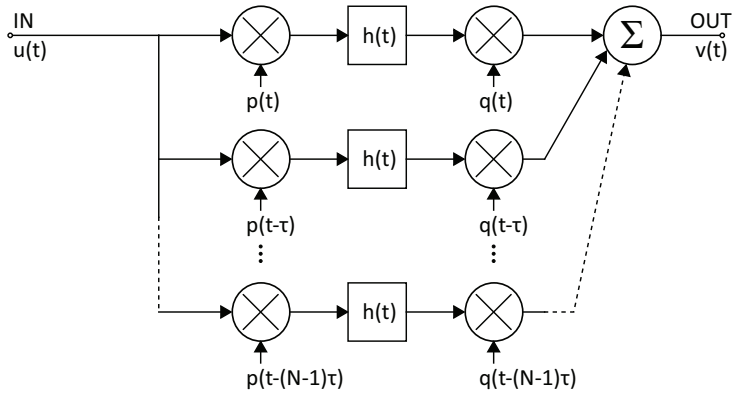


Figure 4.10. N-path filter configuration.

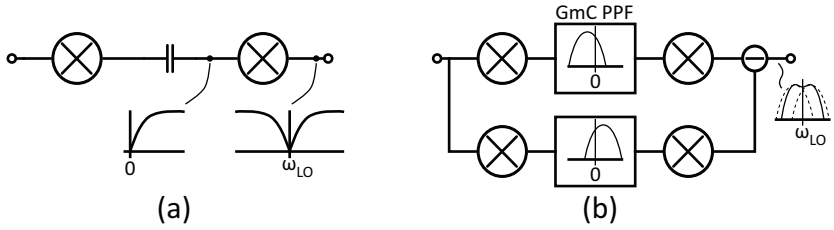


Figure 4.11. N-path filter with a notch (a) and bandpass (b). The bandpass filter has two parallel N-paths with a g_mC polyphase filter to increase the overall filter order to 4. The N-paths have been simplified to one visible path.

tors; 3. the filter frequency can be controlled with the clock frequency; 4. the frequency transform from the low-pass to band-pass is exact; and 5. the technique can also be applied to driving-point impedances [136]. These properties are utilized widely in modern RF implementations that make use of the N-path concept.

4.4.1 N-path filter application in RF receivers

The advent of high-speed, sub-micron CMOS process technology has spawned new possibilities for the N-path filter concept in RF receivers and other applications. The availability of RF-frequency switching has made it possible to synthesize high-Q filters at clock frequencies of multiple gigahertzes. Seven different N-path configurations are presented next.

The first topology is a straight notch filter, which is shown in Fig. 4.11a. The filter is formed by cascading N-path down-conversion mixers, high-pass filtering, and up-conversion mixers. The implementation uses eight clock phases and achieves a rejection of 21 dB, while the loss and NF on the pass-band are –2 and 2 dB, respectively [137]. The notch filter can be used, e.g., in an FDD system to suppress the TX from leaking into the

RX. The second topology, shown in Fig. 4.11b, realizes a more complex bandpass filter. Two N-paths with slightly different center frequencies are realized and their output is taken as a subtraction, as is shown in the figure. The results show that the two 2^{nd}-order filters form a 4^{th}-order band-pass filter [138]. The small frequency offsets from zero have been realized by using g_mC polyphase filters. The implementation results show a high rejection of 55 dB and an out-of-band IIP3 of +29 dBm over a center frequency of 0.3–1.2 GHz. However, due to the subtraction and the 1/f noise of the g_m stages, the NF of the filter is 9.5 dB, which is too high for the filter to be applied as a pre-select filter in a receiver.

The third topology is a feedforward N-path filter, shown in Fig. 4.12a, where the signal has two paths. One path is a normal RF path with an LNA and the other is a filtering path, where an N-path filter is used to create a notch around the LO frequency. Since the two paths are subtracted from each other, a narrow band-pass response results [139]. A stop-band rejection of 21 dB has been reported with a receiver NF of 6.8 dB. The feedforward cancellation is sensitive to the gain and phase mismatch of the two paths. Additionally, other non-idealities, such as component mismatch, cause a rapid degradation in the rejection performance. Of the different issues, the phase mismatch caused by the finite baseband bandwidth of the N-path downconversion mixers limits the rejection performance of this topology [139]. In contrast, the feedback topology, presented in Fig. 4.12b, does not suffer from rejection degradation caused by mismatched due to the inherent nature of the feedback. In the feedback topology, the output signal is down-converted and filtered by the high-pass filter. The remaining signal is subtracted at the RF, where it cancels the interfering signals that lie out-of-band. The resulting frequency response is again a band-pass response that tunes with the LO frequency. Additionally, compared to the feedforward cancellation, the feedback loop linearizes the RF amplifiers within the loop (see Fig. 4.12b) and thus their out-of-band linearity requirements are relaxed when compared to the feedforward topology. Furthermore, because the feedback loop samples the cancellation error signal at the output, it sees a smaller blocking signal and thus the distortion components produced in the feedback loop are also of a smaller magnitude. Reported rejections vary depending on the implementation being between 6 and 48 dB, while the IIP3 is between -5 and +12 dBm. The achieved NF with the feedback topology varies between 4 and 9 dB [140–142], [IV].

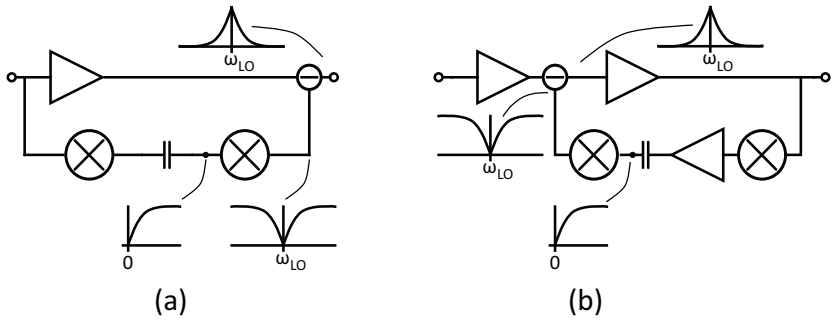


Figure 4.12. Receiver utilizing (a) a feedforward N-path notch filter and (b) a feedback N-path notch filter. The N-paths have been simplified to one visible path.

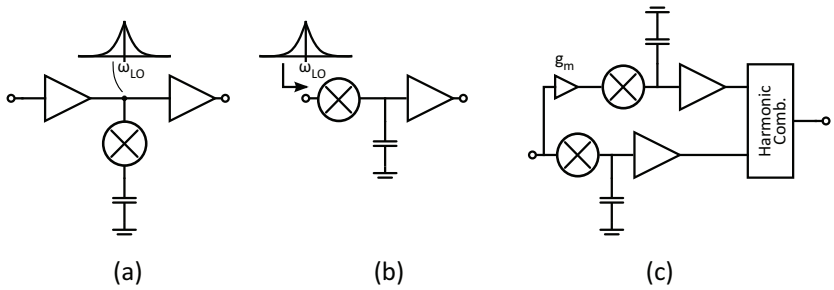


Figure 4.13. N-path application in (a) a high-Q load, (b) a passive mixer-first receiver, and (c) a noise-cancelling mixer-first receiver. The N-paths have been simplified to one visible path.

The last three N-path topologies are presented in Fig. 4.13. In Fig. 4.13a, the N-path filter is used as a high-Q, resonator-type load for the RF amplifiers. The filter operates on the passive mixer transparency property, i.e., the baseband impedance is visible on the RF side as an up-converted version of the low-pass response around the LO frequency [143, 144]. By using two separate LO frequencies and two N-path filters, an image-reject filter can be constructed for a superheterodyne architecture [6]. To maximize the rejection offered by this topology, the switch resistance should be made low ($< 20\ \Omega$) and the filter should be connected to a high-impedance load point, such as an LC-resonator load [145]. When connected to a wideband load, like a shunt-peaked load, the rejection is limited to approximately 10 dB [III]. The filter incurs a noise penalty, which limits its use in front of an LNA. The passive mixer topology, shown in Fig. 4.13b, is a special case of an N-path filter with only one down-conversion mixer. As in the previous topology, the passive mixer also takes advantage of the mixer transparency property to attenuate out-of-band blockers at the input, but in addition the down-converted baseband signal is amplified and processed further by a baseband chain. In the passive

mixer topology, the first amplifier stage plays an important role in the noise and linearity performance of the whole receiver. Therefore, large devices and sufficient bias current are needed in the first baseband stage [V]. The passive mixer-first receiver suffers from down-conversion of the input signal from around the LO harmonic frequencies. Instead of the normal 4-phase mixer, a higher number of phases can be used to improve the harmonic rejection at the expense of a higher LO frequency. However, even with higher number of phases, additional rejection is needed for the harmonics to avoid desensitization by interferers around the LO harmonics. The reported passive mixer-first receivers achieve an IIP3 of -7 to +25 dBm with a NF of 4 to 6.5 dB between reception frequencies of 0.1 to 2.7 GHz [112–114], [V]. An evolution version of the mixer-first receiver has been implemented by adding a noise-canceling auxiliary path, as shown in Fig. 4.13c. This is similar to the noise-canceling LNA topology that was introduced in Section 3.2. The g_m-stage samples the noise voltage generated in the primary down-conversion mixer switches and the inverted version of the signal is fed through a replica mixer and amplifier, as is depicted in Fig. 4.13c. At the output, a harmonic combination of the signal paths is performed for the 8-phase signaling to cancel the 3^{rd} and 5^{th} harmonics and to sum up the noise-canceling paths. The reported IIP3 and NF for this topology are +13.5 dBm and 1.9 dB, respectively [116]. However, the implementation of the noise-canceling path doubles the hardware on the signal path.

In addition to the passive mixer-first analysis and trade-off study presented in this chapter, further analysis of the N-path filter and the various topologies using it are provided in [7, 127, 134, 135, 138, 146–149], [IV-V].

5. Receivers utilizing N-path techniques

This Chapter covers three different receiver implementations using N-path techniques. The receivers also utilize the wideband LNA and buffer topologies that were covered in Section 3. The first receiver is an RF resonator receiver [III] that uses N-path resonators to enhance the selectivity and linearity of the LNA. The second receiver is based on a feedback N-path topology [IV], which is inherently more complex than the first realization. The third implementation is a mixer-first receiver that was implemented together with a wideband antenna [V]. The chapter collects the essential information from the publications [III-V], while the papers themselves provide further details. A comparison of the implemented receivers is provided at the end of the chapter. The author's original contributions in this chapter include the use of N-path resonators in a wideband LNA, a feedback N-path topology, and analysis of the design trade-offs. Finally, the mixer-first implementation together with the wideband antenna is the first of its kind.

5.1 N-path resonator receiver

The need for a wideband, interference-tolerant, RF front-end is due to the fact that highly selective pre-select filters cannot be used in large numbers because they are bulky and expensive off-chip components. While in a traditional radio system the receiver is preceded by a pre-select filter to suppress strong interferers, which relaxes the receiver IC linearity and desensitizing requirements, the wideband front-end in an SDR or a CR radio must have other ways to cope with the hostile interferer environment. One way is to make the receiver path hostile to certain frequencies by utilizing a notch filter at the front-end [74, 102], [I]. While this is effective for a limited number of problematic frequencies, e.g., the device's

own TX signal in a FDD system, the problem with this solution is that the frequencies of the large blockers have be to known a priori.

Another solution is to make the receiver path as selective as possible outside the reception frequency by utilizing structures that behave as LC resonators. This work focuses on using such structures in a wideband receiver. As was previously discussed, a structure called a transferred impedance filter (TIF[1]) relies on a passive mixer and capacitors to implement a selective impedance, which can be tuned by adjusting the passive mixer local oscillator (LO) frequency. A wide tuning range can be achieved with this technique, which makes it suitable for SDR and CR receivers. Such a concept has been demonstrated for a relatively narrowband solution in [141, 145, 150]. For a wideband receiver, the interferer suppression and the effect on the noise figure (NF) have been investigated in [III]. Other issues include the LO leakage to the antenna and the LNA design used with this type of structure [III].

The focus of this work has been on LNA design. The goal has been to gain knowledge about the effect of the TIF to the noise figure and selectivity. Therefore, the gain partition of the front-end has been selected such that the noise figure is determined by the LNA and TIF. This means that with the high gain in the LNA, the overall receiver linearity is dominated by the stages following LNA.

5.1.1 Low-noise amplifier with transferred impedance filters

The front-end of the receiver is composed of a two-stage LNA and two TIFs connected to the input and output of the first stage. The schematic for the two-stage LNA is presented in Fig. 5.1, where the TIFs act as resonator loads for the LNA. The load impedance of the first stage has to be designed as high as possible for the TIF to have good selectivity. Thus, the first stage uses a common-source (CS) amplifier stage with a high-impedance PMOS load. The second stage is a CS amplifier with a cascode stage to increase the overall gain. A shunt-peaked load has been used in the second stage to achieve a wide bandwidth by compensating for the gain response drooping in the first stage. An RC feedback from the second stage output to the first stage input has been used to achieve wideband matching (see Section 3.2). The feedback paths have been cross-connected to maintain correct signal polarity. However, the cross connection is not

[1]TIF naming is used here instead of N-path filter, because it was used in the author's publications [III, IV] at the time of the writing.

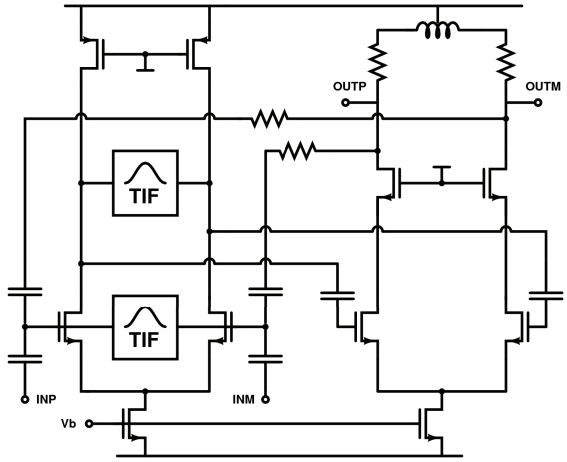


Figure 5.1. Two-stage LNA schematic with TIFs [III].

visible for common-mode signals and therefore this type of amplifier can oscillate. The current sources have been added to ensure that the amplifier stages have common-mode rejection. As depicted in Fig. 5.1, the stages utilize DC blocking capacitors to maintain independent bias levels for the two stages.

The impedance at the TIF's input can simply be approximated as (see Fig. 3 in [III] for the schematic)

$$Z_L \approx Z_{RF}||(R_{sw} + Z_{TIF}). \tag{5.1}$$

The overall impedance is determined as a parallel connection of the Z_{RF} and the TIF impedances. The Z_{RF} includes the impedances associated with the RF circuitry, i.e., the RF loads and parasitics. The TIF impedance is a series connection of the effective switch resistance, R_{sw}, and the frequency-transferred impedance, Z_{TIF}. The Z_{TIF} is large around the LO frequency and low far from the LO frequency. Therefore, the in-band impedance is set by the Z_{RF} and should be as large as possible, whereas the out-of-band impedance is determined by the R_{sw}, which should be as small as possible. The relationship between these two impedances sets the limit for the TIF selectivity. Clearly, using an LC resonator for the RF load will result in better selectivity since the resonator has a high Q-value and the TIF performance is enhanced. However, such a load is a narrowband load and cannot be used in a wideband design. Thus, a PMOS load was used in this design.

The placement of the TIFs plays an important role. For the filter to have a maximum effect on the linearity, it should be placed as close to

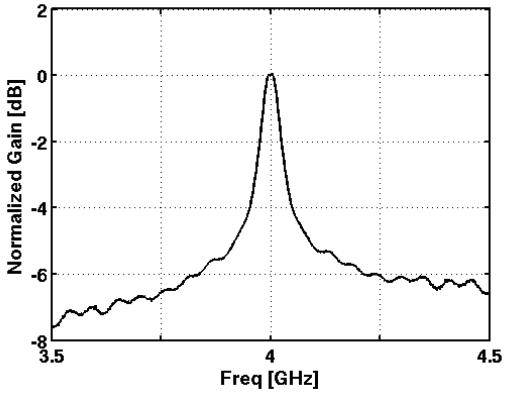


Figure 5.2. Receiver relative gain with TIF ON at 4 GHz LO frequency. [III]

the receiver's input as possible to decrease the out-of-band gain of the succeeding blocks. However, the increase in the noise figure and possible LO leakage can severely degrade the receiver performance if the TIF is placed too close to the input. In this case, it was seen to be beneficial to place one of the filters at the input so that the performance penalty in noise and LO leakage could be measured. The second filter was placed at the first stage load, where it is most effective. The isolation of the first CS stage is low, and thus the selective load impedance can also be seen at the amplifier input.

The LO drive inverters have been designed such that they can be individually powered down if needed. This makes it possible to study the performance of the front-end with the TIF either turned on or off. When turned off, the loading caused by the TIFs is minimal, and therefore, the LNA performance degradation is small. The inverter chains can cover a LO signal up to 5 GHz without using additional inductors, thus the die area penalty for using three separate chains is minimized.

5.1.2 Experimental results

The chip was processed using a 65-nm CMOS process, packaged in a quad-flat package, and assembled on a printed circuit board for measurements.

The selectivity of the receiver with TIFs ON is shown in Fig. 5.2 with an LO frequency of 4 GHz. A selectivity improvement of 6 dB is achieved at a 250 MHz offset. However, the 50 % duty cycle and the relatively low-impedance load at the LNA output limit the selectivity. The receiver input compression point for a blocker at a 500 MHz offset is presented in Fig.

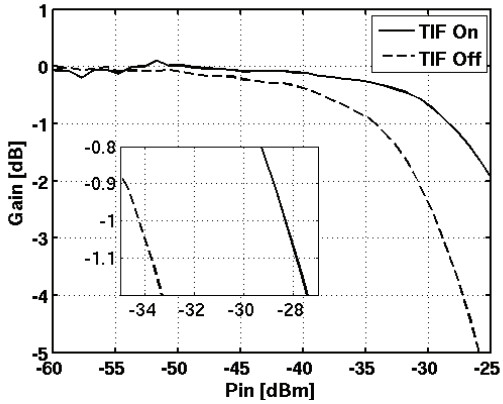


Figure 5.3. Receiver input compression point for a blocker at 500 MHz offset [III].

5.3. The result shows that a linearity improvement of 6 dB is achieved by turning on the filter. A summary of the measurement results is provided in Table I. The LO leakage of the receiver with the TIF turned on is -63 dBm. Additionally, the LNA gain, linearity, and noise have been estimated from the measurement results of the complete receiver in Table 5.1. The LNA results show that a wideband interference blocking scheme can be implemented with a noise degradation of 1.5 dB. However, the effectivity of the N-path filtering is much better for a resonator load [144, 145].

Table 5.1. Measurement results for a wideband receiver and LNA estimate with N-path resonators [III].

	Receiver		LNA Estimate	
TIF (OFF/ON)	OFF	ON	OFF	ON
Technology	65nm CMOS		65nm CMOS	
Area (um)	890 x 890		na	
Supply (V)	1.2		1.2	
Idc (mA)	41	46	14	19
Gain (dB)	44	40	24	20
S11< -6dB (GHz)	1-5	1-6	1-5	1-6
NF (dB)	4.4	5.9	3.4	4.9
Blocker ICP (dBm)	-34	-28	-21	-15
IIP3*(dBm)	-24	-20	-12	-8
LO leakage (dBm)	na	-63	-na	-63

* Test tones at 500 and 995 MHz offset.

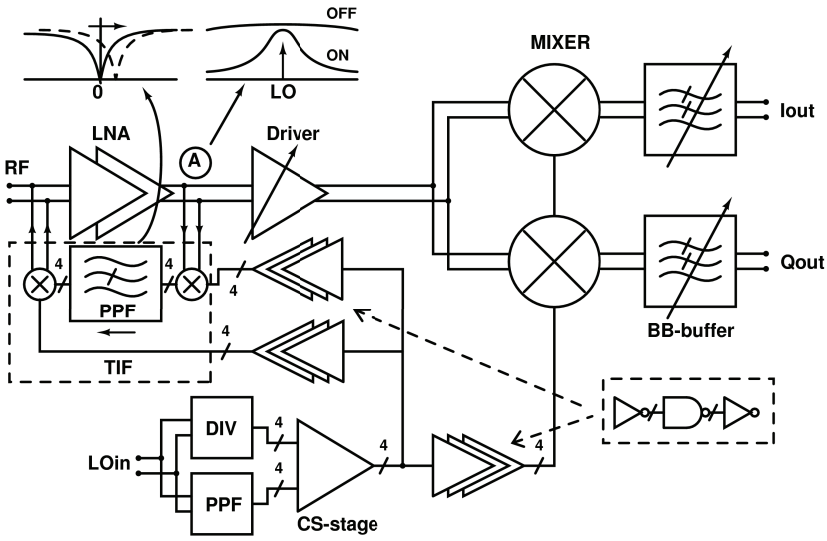


Figure 5.4. Wideband N-path feedback receiver architecture overview [IV].

5.2 N-path feedback receiver

5.2.1 Receiver

The focus of the second presented receiver was to introduce adjustable selectivity around the LNA, which linearizes the front-end [151]. The proposed feedback cancellation scheme is presented in Fig. 5.4. The feedback uses two passive mixers and an adjustable polyphase filter (PPF) to linearize the RF front-end. Effectively, the mixers upconvert the complex filter response around the LO frequency. When the feedback is turned off, the receiver operates as a normal direct-conversion receiver.

The operating principle of the transferred impedance filter is based on two separate phenomena that affect the behavior of the TIF (N-path filter) in a closed-loop system. First, the front-end contact points, A and RF input in Fig. 5.4, see a sharp resonator-type impedance at the LO frequency through the mixers due to the transparent behavior of the passive mixers. The achievable out-of-band attenuation with this upconverted impedance is limited by the ratio of the effective series resistance of the switches and the RF impedance where the mixer is connected. Second, when the mixers are connected in feedback through the PPF, the desired signal sees a notch, as depicted in Fig. 5.5a, and only the interference is fed back from the LNA output. As a result of subtraction, interference at the RF input is suppressed, thus improving the out-of-band linearity of the whole front-

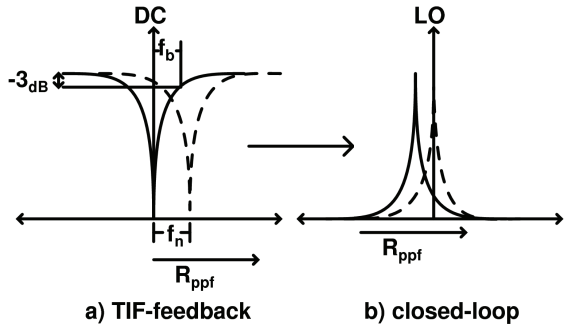


Figure 5.5. Behavior of the TIF feedback (a) and closed-loop system (b) for filter notch offset frequency tuning [IV].

end. The end result is the band-pass-type, closed-loop response shown in Fig. 5.5b. The function of the PPF notch filter is to compensate for the varying phase around the feedback so that maximum gain is maintained around the LO frequency, as depicted in Fig. 5.5. Therefore, the PPF notch frequency is made adjustable by tuning the filter resistor value (R_{ppf}). Note that the baseband frequency domain is complex, which translates normal low-pass and high-pass responses into band-pass and band-stop (notch) responses. The main advantage of this type of filtering scheme is that the corner frequency and frequency selectivity of the polyphase filter are up-converted to the LO frequency and are independent of the LO frequency. Thus, changing the LO frequency does not change the bandwidth of the up-converted, closed-loop system response.

5.2.2 Transferred impedance feedback analysis

An in-depth analysis of the feedback and the closed-loop system is described in [IV]. The target was to achieve better understanding of the complex dependencies of the frequency-translation feedback system. The analysis defines a TIF model and the parameters leading to a y-parameter, 2-port description, which is then frequency transferred to achieve an RF frequency model. After the frequency transformation, a closed-loop system transfer function is solved. The most relevant results of the analysis will be highlighted next and general design guidelines are provided as a conclusion to the analysis.

The analysis was performed for parameter values that were determined based on transistor-level simulations. Unless otherwise mentioned, the values were as follows. (Model shown in Fig. 4 of [IV]) in The gain of the LNA, A_{dc}, was 22 dB, the LNA transconductance, g_m, was 30 mS, the

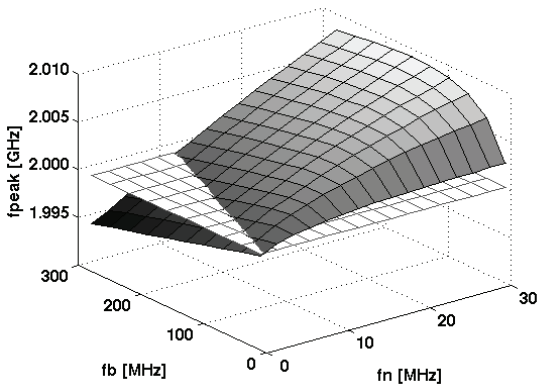


Figure 5.6. Frequency of maximum gain peak versus filter bandwidth and notch offset frequency in the TIF analysis. The targeted LO = 2 GHz is shown with a constant plane (white mesh) [IV].

mixer switch on-resistance, R_{on}, was 50 Ω, and the input resistance, R_s, was 50 Ω. The LNA input and output pole frequencies, f_i and f_{3dB}, were 5 and 2 GHz, respectively. The PPF filter notch bandwidth, f_b, and notch offset frequency, f_n, were 180 and 7 MHz, these are shown in Fig. 5.5.

In Fig. 5.6, the maximum gain frequency, f_{peak}, is plotted against the notch-offset and bandwidth frequencies. In this simulation, the LO frequency was 2 GHz and it is represented by a constant plane in the figure. The figure clearly shows that if a regular high-pass filter ($f_n = 0$) is used in the feedback, the resulting closed-loop gain peak will always be below the desired frequency due to the phase shift in the loop. For example, the necessary notch offset frequency compensation is 10 MHz for a TIF bandwidth of 200 MHz. The figure also implies that the required notch offset frequency compensation changes as the bandwidth of the system is altered. Furthermore, the figure shows that the necessary correction decreases with the filter bandwidth. Therefore, a programmable PPF should be used to shift the closed-loop maximum gain back to the LO frequency.

Figure 5.7 shows the selectivity of the close-loop system at a 50 MHz offset from the LO frequency in relation to the filter bandwidth and the filter notch offset frequency. The selectivity was observed at a 50 MHz offset since it serves to characterize the close-by selectivity better than the maximum selectivity far away from the LO frequency. The figure shows that if the system requires a high notch frequency compensation, then the maximum selectivity becomes small. For example, for a notch frequency compensation of 15 MHz, the achievable closed-loop maximum selectivity is below 15 dB regardless of the filter bandwidth. What is interesting is

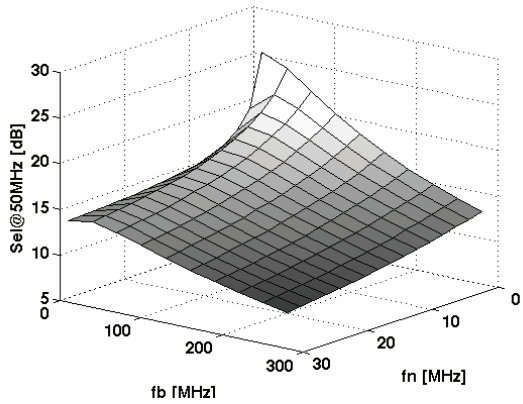


Figure 5.7. Selectivity at a 50 MHz offset from the LO frequency versus the filter bandwidth and notch offset frequency in TIF analysis [IV].

that the notch frequency has a much more severe impact on the selectivity when the filter bandwidth is small.

The other observations made based on the analysis will be discussed next. When the bandwidths of the LNA input and output, the f_i and f_{3db}, are decreased, the required notch frequency compensation increases and thus the selectivity degrades. However, the effect of the output, f_{3db}, is much more pronounced than for the input bandwidth since the input impedance level is nominally fixed and low. The LNA gain should be large to maximize the selectivity, which, together with a wideband resistive load, results in the need for a high g_m. Additionally, the switch series resistance, R_{on}, affects the system such that it should be minimized in order to maximize the selectivity because a large resistance value deteriorates the feedback signal level. However, having a small switch resistance leads to a larger TIF filter capacitance value for any given system bandwidth.

Based on the analysis, a design procedure for a feedback TIF LNA can be derived as follows:

- Design the LNA for high gain, high Z_{out}, and low C_{out}. A high g_m should be used to meet noise and linearity requirements.

- Determine the desired system bandwidth and, using the model, map it to the needed TIF bandwidth.

- Design the mixers with a small R_{on} and calculate the filtering capacitor size.

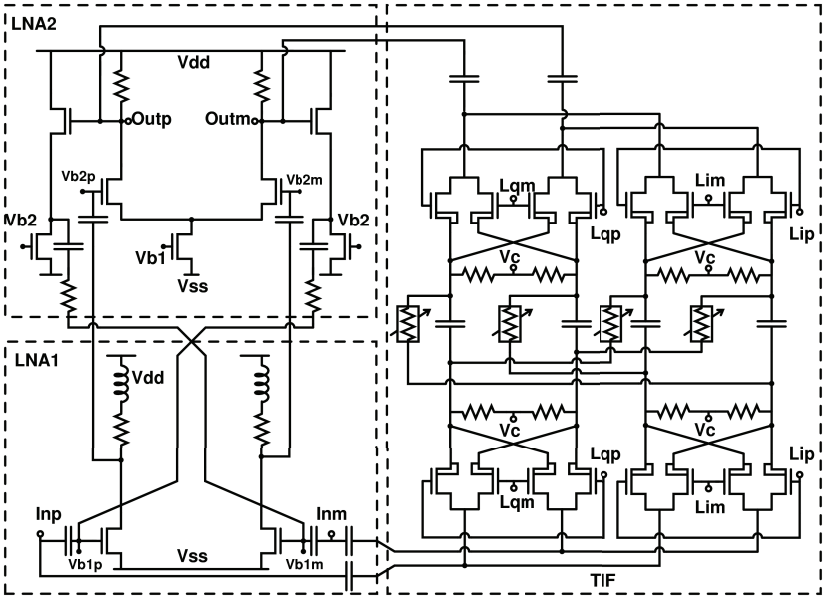


Figure 5.8. Schematic of 2-stage, wideband LNA and TIF feedback [IV].

- Using the model, define the required notch adjustment range in relation to the LO frequency range.

- Check for stability. Re-iterate if necessary.

In practical cases, the achievable gain and output impedance values are often limited to modest values, e.g. 25 dB and 200 Ω, especially in wideband systems, resulting in limited selectivity. All parasitic capacitances in the closed-loop system's nodes deteriorate the system performance by requiring the use of a higher notch offset frequency to compensate for the parasitics. The switch series resistance also has a practical lower limit, which can make it difficult to achieve a high enough feedback signal level for the cancellation to be effective. To boost the feedback signal, one can add an amplifier before the filter [152]; however, this solution severely degrades the bandwidth of the feedback and the stability of the system.

5.2.3 Circuit design

LNAs

A CS topology was chosen for both LNA stages to provide high gain for the feedforward path, as is depicted in the schematic of the LNA and TIF in

Fig. 5.8. The cascode stage, typically used together with a CS stage, has been omitted to maintain adequate voltage headroom in the LNAs. The first stage utilizes a shunt-peaked load to compensate for the RC roll-off over the wide reception bandwidth. The simulated -3dB bandwidth of the open-loop LNA is 6.3 GHz, with a maximum gain of 24 dB. The output of the second stage (TIF input (A) in Fig. 5.4) uses a wideband resistive load, which limits the maximum selectivity of the TIF system.

When the TIF feedback is not used, a voltage follower RC feedback is connected from the second-stage output to the RF inputs to provide wideband matching for the receiver input. The stability of a 2-stage LNA with feedback, like the one in Fig. 5.8, is generally of some concern. When differential signaling is used, the paths can always be crossed so that negative feedback is maintained. However, a positive feedback is created for common-mode (CM) signals since the signal path crossing does not invert the CM polarity. Therefore, we have added a current source to the second stage input to suppress the CM gain of the LNA. The simulated current consumption of the LNAs and the matching feedback is 21 mA.

Transferred impedance filter

The details of the TIF are presented in Fig. 5.8. As was explained in the analysis, when the TIF is used in a wideband configuration, the feedback loop exhibits a variable phase shift, which shifts the desired frequency response slightly below the LO frequency by various amounts. Hence, we propose to use an adjustable PPF to shift the feedback gain and phase responses so that a closed-loop system response is maintained around the LO frequency, as depicted in Fig. 5.4. When the PPF resistor values are decreased, the notch frequency of the filter increases and its phase response is correspondingly altered. Previous studies on transferred impedance resonator structures [139, 141, 145] do not provide evidence of this type of compensation.

5.2.4 Experimental results

All of the measurements of this receiver include the effects of the PCB, the RF lateral SMA connectors, the 44-pin QFN package, and standard process ESD protection. The RF and LO paths on the PCB were implemented as grounded co-planar waveguides (GCPW). Additionally, good continuity of the GCPWs was ensured by extending the ground lines with parallel bond wires into the chip.

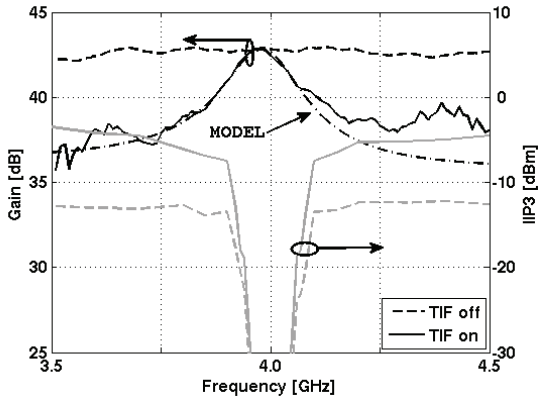


Figure 5.9. RF front-end gain, modeled response, and IIP3 with TIF on (solid) and off (dashed) when LO = 4 GHz [IV].

The measured gain, the modeled gain from the analysis, and the IIP3 responses at 4 GHz are shown in Fig. 5.9. As can be observed, the wideband frequency response is transformed into a band-pass frequency response when the TIF is turned on. The TIF response was measured as the difference between the BB output frequency responses in the on and off cases because a direct measurement of the TIF response was not possible. The attenuation at 500 MHz offset is 5 to 7 dB, which is limited by the gain, the switch R_{on} resistance, and the output impedance of the LNA. The IIP3 of the RF front-end is also shown as a function of the test-tone offset from the LO frequency. In the measurement, the IMD3 difference frequency is fixed at 3 MHz. At low offsets, the IIP3 is dominated by the BB buffer, while at out-of-band frequencies the IIP3 is dominated by the front-end. The IIP3 improvement at a 500 MHz offset is 8 to 9 dB. Analysis of the experimental results show them to be in agreement with the theory, as depicted by the model response shown in the figure. During the design of the circuit not all trade-offs were known at that time, which lead to a sub-optimal implementation and limited selectivity. According to the theory, there is still room for improvement in the selectivity by increasing the LNA gain and decreasing the switch R_{on} resistance and bandwidth. A practical limitation of the performance is set by the trade-off of power consumption and layout size with these parameters.

The blocker input compression point of the front-end was measured by increasing the blocker power at the 500 MHz offset from the LO signal and simultaneously measuring the gain of a weak in-band signal. The measured results are shown in Fig. 5.10, where it can be seen that the

Table 5.2. Measurement results for a wideband N-path feedback receiver [IV].

	TIF OFF/ON	TIF OFF/ON	TIF OFF/ON
LO Freq (GHz)	2.4	4.0	5.3
Gain (dB)	42/40	43/41	42/40
IIP3 (dBm)	-11/-5	-13/-5	-11/-7
IIP2 (dBm)	>45/>45	>30/>35	>28/>31
Blocker ICP (dBm)	-20/-15	-23/-16	-23/-18
NF (dB)	4.3/5.8	3.2/5.7	3.9/5.9
S11< -10dB (GHz)	2.5-5.5		
LO leak (dBm)	-85/-63	-56/-54	-58/-56
Idc (mA)	45/53	44/56	46/58
Gain Adjustment (dB)	15		
BB bandwidth (MHz)	3-50		
Active area (mm^2)	0.25		
Technology	1.2V 65nm CMOS		

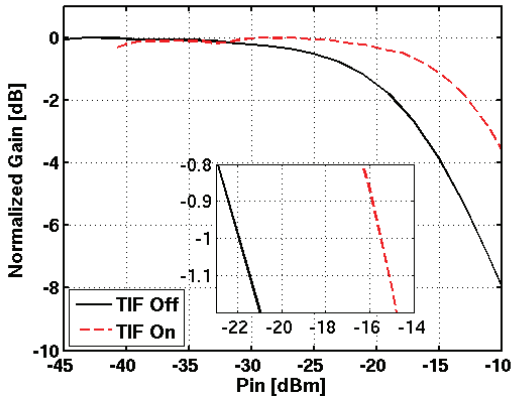


Figure 5.10. Blocker ICP with TIF on (solid) and off (dashed) when the LO = 4 GHz and f_b = 4.5 GHz [IV].

blocker ICP improves by more than 6 dB from -22 dBm to more than -16 dBm for the TIF off and on cases, respectively.

Table 5.2 summarizes the performance of the TIF RF front-end at frequencies of 2.4, 4.0, and 5.3 GHz. The results demonstrate the feasibility of the wideband feedback architecture. Table 5.2 shows the measured LO

Table 5.3. Comparison table for blocker-tolerant narrowband and wideband receivers [IV].

	Narrowband			**Wideband**	
Circuit	LNA+Mix	LNA+Mix+LO	Receiver	LNA+Mix+BB+(SX)	**LNA+Mix+LO+(BB)**
Cancellation method	Feedforward OFF / ON	Feedback OFF / ON	ΣΔ Feedback OFF / ON	Feedforward	**Feedback OFF / ON**
Freq (GHz)	1.96	1.9	0.9	0.4-3**	**2-6**
Gain (dB)	23.4 / 20.9	24.7 / 22.5	40	70	**43 / 41**
ICP (dBm)	-12 / 0*	-28*/ -17.5*	na / -18	-8	**-23 / -16**
IIP3 (dBm)	2.6 / na	na	-4*/ +4	+10	**-13 / -5**
NF (dB)	3.9 / 6.8	8.8 / 8.9	2.3 / 6.2	3	**3.2 / 5.7**
Idc (mA)	8 / 29	150	66.5	30-55mW	**44 / 56**
Supply (V)	2.5 & 1.2	2.5	1.2	2.5 & 1.1	**1.2**
Technology	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	**65nm CMOS**
Ref	[139]	[141]	[145]	[87]	**[IV]**

* Estimated ** Estimated -3dB bandwidth

leakage levels at the input of the receiver, which can be a potential problem with this kind of receiver architecture. However, as can be seen from the table, the leakage is more than 25 dB lower for the case in which the TIF is off and when the divider is used, which suggests that the leakage is in fact limited by the off-chip coupling when the LO PPF is used. Table 5.3 shows a comparison of this work with recent publications. As can be observed, various N-path filtering techniques have been implemented on narrowband systems. For a wideband implementation [87], good linearity results have been achieved; however, in this case a high supply voltage has been used to improve the linearity of the LNA. It turns out that when an ideal SDR receiver is sought, the linearity of the LNA is the bottleneck that is difficult to fulfill, even with filtering. Therefore, the mixer-first receiver topology is a better candidate for SDR implementations.

5.3 Mixer-first receiver with a compact-size, wideband antenna

Mixer-first receivers have recently demonstrated potential to become a true SDR solution with good flexibility, linearity, and noise performance [113, 114, 127]. While there are still unresolved issues, such as that concerning the harmonic mixing, the topology has gained momentum. Furthermore, similar to digital transmitters [153] and synthesizers [154], mixer-first receivers are fundamentally performing a sampling operation at the input and, thus, will benefit from the continuously decreasing line width by making their switches faster and more efficient. Simultaneously, inherently non-resonant antennas with a capability for very wide and continuous frequency tuning ranges have been introduced [155, 156]. Capacitive coupling element (CCE) antennas are a viable candidate for mobile SDR with operation across a broad frequency range. Unlike most resonant antennas, the geometrical structure of CCE antennas does not exhibit inherent frequency selectivity, which makes it easy to tune. In this implementation, we utilize these two advances in a single-antenna SDR receiver capable of operating over a wide frequency range. The implemented system can operate on LTE bands ranging from 0.7 to 2.7 GHz while using a single antenna and a single RF input. To the author's knowledge, this is the first demonstration of a mixer-first receiver with a CCE antenna.

This section covers the system considerations of the receiver and the antenna and highlights the receiver implementation and experimental

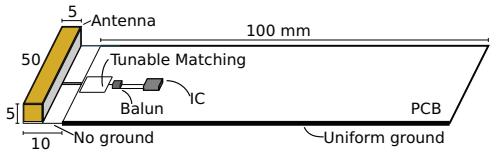


Figure 5.11. System diagram showing the physical dimensions of the antenna and the board together with the component placements. The thicker line on the side reflects the fact that the bottom ground plane is used as a radiating element together with the CCE. The dimensions are in millimeters [V].

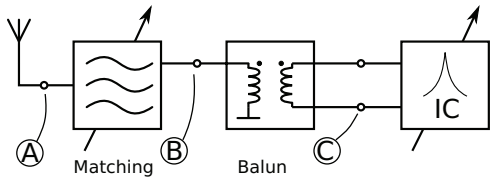


Figure 5.12. Block diagram of the system input configuration [V].

results of both, the IC and the system. Further details are provided in [V]. The antenna implementation has been presented in more detail in [157]. Analysis of the passive, mixer-first receiver interface impedance was presented in Section 4.3, while the LO circuitry used in the receiver is covered in Section 6.3.

5.3.1 System considerations

Interfacing a wideband receiver with an antenna that is capable of a large tuning range poses different kinds of requirements on matching than in a conventional case, where the input is matched at frequency points defined by the supported systems. The antenna and receiver input reactances vary over frequency, and handling this behavior is one key to wideband matching.

A physical description of the system and a block diagram of the key interfaces are shown in Fig. 5.11 and Fig. 5.12, respectively. Figure 5.11 depicts the relative locations of the interface key components, namely the antenna element, the tunable matching, the balun, and the integrated receiver circuit (IC). All of the components are placed on a printed circuit board (PCB) that is 110x50x5 mm in size, which makes it suitable for mobile handset integration.

There are certain requirements and limitations in the IC interface (node C, Fig. 5.12). First, the performance of a mixer-first receiver is optimized when it is presented with a sufficiently large antenna impedance, as was shown in Section 4.3. On the other hand, the single-ended CCE

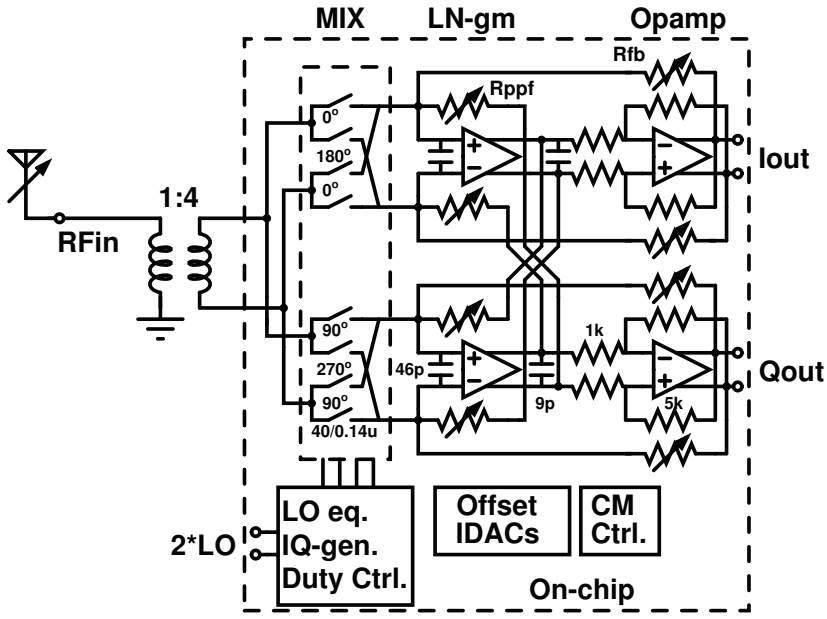


Figure 5.13. Wideband mixer-first receiver architecture overview with a quadrature passive mixer, a 2-stage baseband filter, and an LO chain [V].

antenna impedance is inherently low, which interfaces poorly with the desired high IC input impedance. Second, LO noise and receiver linearity issues are alleviated by using balanced input signaling, but compact-size, balanced antennas do not reach low-band ($<$1 GHz) operation in mobile handsets [158]. These problems have been addressed by using a balun, depicted in Fig. 5.12, which accomplishes unbalanced-balanced and impedance transformations simultaneously (from node B to C in Fig. 5.12). Due to the fundamental limitations of small antennas, the CCE antenna cannot be instantaneously matched across all frequencies without separate matching circuitry. Hence, reconfigurable matching is still needed, as is shown in Fig. 5.12.

5.3.2 Mixer-first receiver implementation

Figure 5.13 shows the complete receiver architecture, including the transformer, the quadrature passive mixer, the low-noise transconductance stages (LN-gm), the output operational amplifiers (Opamp), and the LO path with a duty-cycle control. The input transformer is a commercial 1:4 balun, which limits the receiver's operating frequency to 0.7–2.7 GHz.

A 4-phase mixer is used to limit the required input LO frequency range and to minimize the LO power consumption. Using an 8-phase mixer

would provide additional harmonic rejection and a lower noise figure with increased power consumption, circuit complexity, and synthesizer requirements. The passive mixer is implemented with low-V_t devices to maximize the overdrive voltage and to minimize the switch resistance (20 Ω). It was concluded that the choice of the switch size was an effective compromise between the noise, the linearity, the operating bandwidth, and the power consumption, as was previously discussed in Section 4.3. A triple-well configuration was used to tie the transistor bulk to the same potential with the source, which provides a lower V_t, and to isolate the mixer from the substrate.

Low noise performance has been achieved with a differential LN-gm that uses a PMOS differential pair with a W/L-ratio of 1200, a 100-kHz 1/f-noise corner, and a 7 mA current consumption. A local CM feedback with a 1 pF capacitor provides additional rejection for high-frequency interference. The cross-connected 3-bit polyphase resistors (R_{ppf}) over the first stage perform complex input impedance tuning. According to simulations, the capacitance at the input of the mixer shifts the input impedance to the capacitive side of the Smith's chart and, to perform matching, complex impedance tuning is only needed in the inductive direction.

The Opamp stage uses a lead-compensated, 2-stage amplifier with the driver stages drawing a 22 mA current due to the 50 Ω measurement interface. The input stage of the opamp utilizes a W/L-ratio of 2000 to achieve low noise and high linearity. By controlling the values of the adjustable 3-bit feedback resistance (R_{fb} in Fig. 5.13) and mixer switch series resistance (through duty-cycle or overdrive voltage), the input matching impedance at the transformer input can be tuned to between 28 and 330 Ω to accommodate for the antenna interface. Furthermore, the feedback resistor enables bandwidth and gain control by adjusting the filtering RC product and by adjusting the switch resistance to feedback resistance ratio that controls the gain.

5.3.3 IC experimental results

The receiver was fabricated using a 65-nm CMOS technology and it occupies an active area of 0.3 mm^2. Figure 5.14 shows the measured gain, the noise figure, and the third-order input intercept point (IIP3) of the receiver with the balun from 0.7 to 2.7 GHz. The gain of the receiver varies from 41 to 43 dB, while the IIP3 is between +17 and +20 dBm (50 and 98 MHz offset test tones). The NF of the receiver varies from 4.2 to 6.0

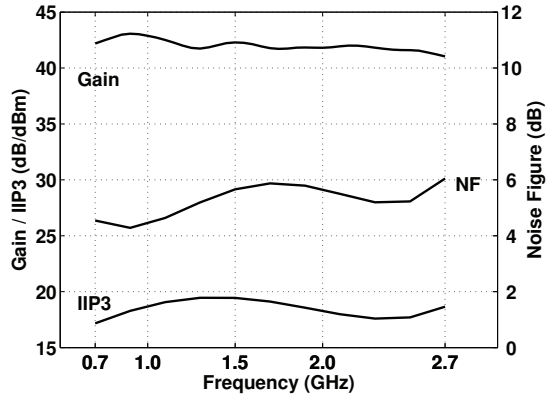


Figure 5.14. Receiver gain, noise figure, and third-order intercept point over the reception band [V].

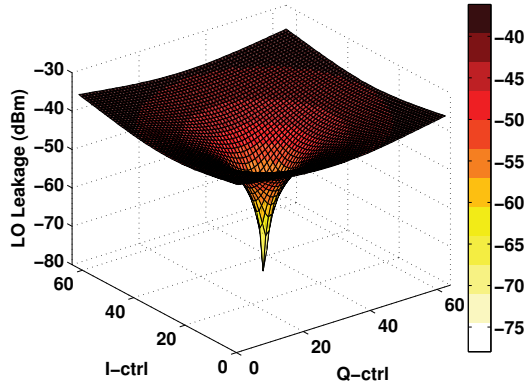


Figure 5.15. LO leakage at 1 GHz compared to the I- and Q-branch offset IDAC codes.

dB. The balun has approximately a 1-dB impact on the NF. The results in Fig. 5.14 show that with the duty-cycle control, the gain droop and the NF degradation can be mitigated at high frequencies. The blocker NF for a –15-dBm blocker was 5 dB, while the rejection for 3^{rd} and 5^{th} harmonics were 10 and 33 dB, respectively.

Using the optimal DC-offset codes from an IIP2 measurement, the LO leakage was less than –60 dBm over the entire frequency band. A sample measurement from the RF input is presented in Fig. 5.15, where values below -70 dBm can be observed. The IQ amplitude and phase imbalance from the baseband output with a 1 MHz test signal (LO = 1 GHz) were less than 0.5 dB and 0.5 degrees, respectively.

Table 5.4 shows the RFIC measurement results compared to recent similar IC implementations and simulations. The interface optimization al-

Table 5.4. RFIC results and comparison table [V].

	Simulated	**Measured**	[114]	[127]	[113]	[87]
Architecture	**MX+BB+ LO**	**MX+BB+ LO**	MX+BB+ LO	2xMX+ BB+LO	MX+BB +LO	LNA+MX+ BB+LO+SX
Freq. (GHz)	**0.7-2.7**	**0.7-2.7**	0.1-2.4	0.08-2.7	0.2-2.0	0.4-3[2]
Req LO range (GHz)	**1.4-5.4**	**1.4-5.4**	0.4-4.8	0.32-10.8	0.8-8	0.8-6
Gain (dB)	**41**	**40**	40-70	70	19	70
NF (dB)	**3.0-4.5**[1]	**3.2-5**[1]	3-10	1.5-2.4	6.5	3
OB-IIP3 (dBm)	**+17**	**+17**	+25	+13.5	+11	+10
IIP2 (dBm)	**na**	**+60**	+56	+54	+65	+70
Blocker ICP (dBm)	**+10**	**+5**	+5	-1	na	-8
IQ imbal. (dB/°)	**na**	**0.5/0.5**	na	na	na	na
Power (mW)	**30-40**[3]	**31-42**[3]	37-70	35-78	67	30-55
Supply (V)	**1.2**	**1.2**	1.2/2.5	1.3	1.2	1.1/2.5
Active area (mm^2)	**0.27**	**0.27**	0.75	1.2	0.13	2
CMOS Technology	**65 nm**	**65 nm**	65 nm	40 nm	65 nm	40 nm

[1] Without 1-dB balun loss [2] Estimated -3-dB bandwidth [3] Excluding 50-Ω BB drivers

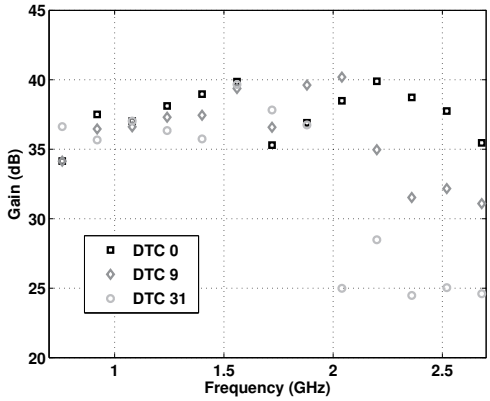


Figure 5.16. System frequency response with the reception antenna [V].

lowed the reduction of the active area of the design while maintaining state-of-the-art performance. As can be seen in Table 5.4, adding the duty-cycle control to the receiver has no adverse effects on the performance, while it still adds a trade-off possibility to our design. The duty cycle performance trade-off for the mixer-first receiver is presented in Section 6.3.2.

5.3.4 System experimental results

The system experiments were executed in four parts: First, the system interface was co-designed prior to implementing the RFIC; second, characterization measurements were conducted to verify the antenna and RFIC functionality; third, the interface was verified with simulated and measured data; and fourth, system measurements were performed. Compared to conventional antenna or RFIC measurements, the system validation process involved making some non-trivial measurements. Many of these measurements were performed to normalize the input power at the antenna and, thus, to avoid making approximative link-budget calculations.

To verify the functionality of the interface arrangement, the inherently low-impedance CCE antenna with a discrete tunable capacitor (DTC), and the mixer-first receiver were assembled on a 4-layer Rogers (4350B/4403) PCB substrate and measured over the air with the help of a transmitting, dual-polarized Vivaldi antenna. The measured frequency response of the system is presented in Fig. 5.16 for three different DTC tuning codes. The measurement includes all of the dissipative and reflective losses of the system and, thus, the measured gain is lower than for the IC charac-

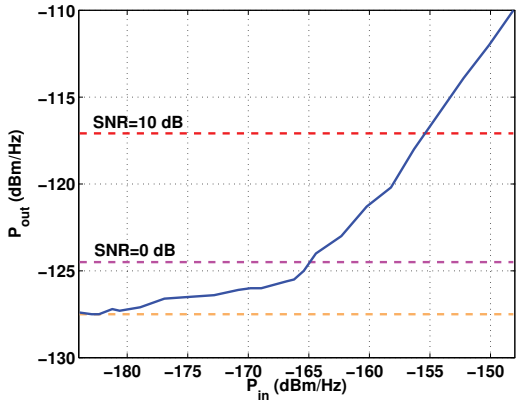


Figure 5.17. System sensitivity measurement with the reception antenna [V].

terization measurement in Fig. 5.14. Compared to the default (DTC 0) code, we were able to achieve up to a 3-dB improvement in system gain at certain frequencies by tuning the DTC codes.

The sensitivity measurement of the receiver at 1 GHz is shown in Fig. 5.17, where the signal-to-noise ratio (SNR) levels of 0 and 10 dB are also depicted. The noise figure of the system can be approximated using

$$NF = 174 - 10log(BW) - SNR_{out} + P_{in}, \tag{5.2}$$

where BW is the bandwidth, SNR_{out} is the desired SNR, and P_{in} is the input power level where the SNR level is met. The approximation gives an overall system NF of 9 dB, including all losses. We approximated the 9-dB NF to consist of the following contributions: An antenna loss of 2-3 dB, a matching and balun loss of 2-3 dB, and an IC NF of 4 dB.

Providing the antenna with a sufficient amount of power during linearity measurements was challenging. With a very linear RFIC and a total path loss of more than 40 dB to the antenna, the power at the receiving antenna is too small and the intermodulation products easily fall under the noise floor. For this reason, blocker ICP measurements could not be performed. However, with test tones of 1.050 and 1.098 GHz we measured an IIP3 of +17 dBm, which is in line with the RFIC results.

During the measurements, the tuning of the receiver feedback resistor (R_{fb} in Fig. 5.13) was found to contribute very small changes to the actual frequency response shape of the system. There are a number of possible reasons for this. First, the transformer efficiently suppresses all impedance changes visible at the balanced side to the unbalanced side, due to both the transforming ratio and the internal matching of the com-

ponent. Second, any transmission line between the receiver and the balun will shift the impedance on the Smith's chart and, thus, affect the intended matching impedance. To optimize performance, it would be beneficial to implement the transformer on-chip to circumvent this interface dilemma. In a more general case, a wideband SDR interface needs to minimize the lengths of all RF traces since it is difficult to guarantee an ideal matching impedance over a wide bandwidth. This fact will be emphasized in future multiple-input-multiple-output (MIMO) and carrier aggregation systems, such as LTE-A, where separation between the antennas is needed and, therefore, the PCB traces will also end up being longer than what is ideal.

5.4 Summary of the implemented N-path receivers

Three different receiver implementations utilizing an N-path filter were presented in this chapter. The first N-path resonator receiver was the first N-path implementation by the author. This receiver achieved a wide RF band (2–6 GHz), but it suffered from limited selectivity due to the low impedance RF load and the 50% duty cycle that was used in the LO drive. The feedback N-path receiver demonstrated a complex architecture, which, based on the simulations, could achieve a selectivity of more than 20 dB. This receiver used a more linearity-oriented gain partitioning and achieved an IIP3 improvement of 15 dB compared to the previous receiver. In part, this was also due to the 25% duty cycle that was generated with a NAND-based logic circuitry. The noise performance was comparable to the resonator-based, N-path receiver. The mixer-first receiver was a concept circuit for studying the interface impedance design together with a wideband CCE antenna. Compared to the two previous implementations, in this receiver the baseband and the LO chain design gained an increased focus. As a result, a tunable duty-cycle circuit was developed for the LO drive and the baseband stages achieved a robust, high-linearity, and low-noise performance. The mixer-first receiver demonstrated an IIP3 of +17 dBm with a similar noise figure as the first two receivers. The implemented RF band was targeted for the LTE frequencies (0.7–2.7 GHz) and the instantaneous bandwidth was also narrower than the previous N-path receivers by the author. All three receivers suffer from LO leakage and harmonic folding issues, as was discussed previously. The LO leakage can be reduced by a calibration routine, as was shown in Fig.

5.15 for the mixer-first receiver. For the harmonic folding issue, a higher number of phases (e.g., 8) can be utilized in the mixer for additional rejection, but additional pre-select filtering is still needed for the 3^{rd} and 5^{th} harmonics to achieve sufficient suppression. In conclusion, it can be said that the mixer-first topology fulfills many requirements of the SDR radio concept, while the feedback and the resonator topologies are more suited for conventional receiver operation with a linearity boost mechanism.

6. Local oscillator drive and quadrature generation

This chapter presents the design aspects of a local oscillator drive and quadrature generation for down-conversion mixers. The chapter is organized as follows. First, the conventional passive polyphase filters and dividers are introduced. Then, the active polyphase filter is presented and the analysis results and the experimental implementation results of [VI, VII] are highlighted. Next, duty cycle manipulation methods are presented and a more detailed description of a feedback control method from [V] is presented. Finally, the quadrature generation methods are qualitatively compared to each other and other LO drive requirements are discussed. The chapter's main points of emphasis include the original contribution of the author to the active polyphase filter and the duty-cycle control circuitry.

6.1 Dividers and polyphase filters

Quadrature generation is needed in modern radio communication systems to separate the frequency or phase modulated data [9], and it is therefore an essential part of a wireless communication hardware. Quadrature generation is typically performed on the LO path where it can be generated with an RC network, a frequency divider, or a cross-coupled, voltage-controlled oscillator [159]. The appropriate choice depends on the architecture and the targeted system.

An example topology of an LO chain is shown in Fig. 6.1, where typical locations of different LO chain blocks are depicted. A parallel quadrature generation topology can be utilized to reduce the required synthesizer frequency range, as is shown in this example. Due to mismatches of the active and passive components, the quadrature signals are not in perfect balance, which in turn degrades the image rejection of the system.

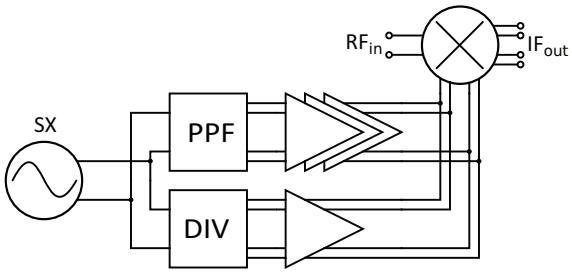


Figure 6.1. LO chain consisting of a synthesizer, a polyphase filter, a divider, buffers, and a mixer.

The amplitude and phase imbalance of the quadrature signal is measured with the image rejection ratio (IRR), which can be expressed as [160]

$$IRR = \frac{1 - 2\epsilon \cdot cos(\phi) + \epsilon^2}{1 + 2\epsilon \cdot cos(\phi) + \epsilon^2}, \tag{6.1}$$

where

$$\epsilon = \frac{|I|}{|Q|}, \tag{6.2}$$

$$\phi = \pi/2 - Arg(I) - Arg(Q), \tag{6.3}$$

where I and Q are the complex LO or baseband voltage waveforms.

6.1.1 Dividers

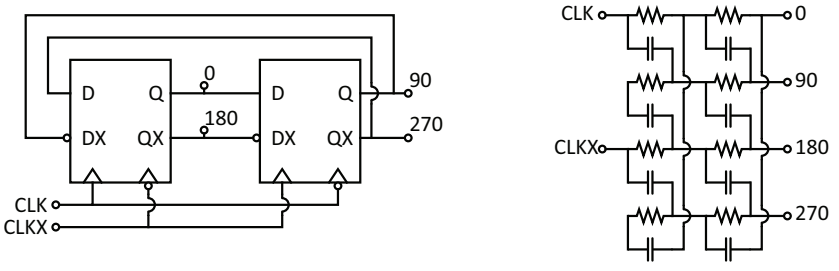


Figure 6.2. Quadrature signal generation with (a) a divider and (b) a type-I, 2-stage polyphase filter.

A static, divide-by-2 frequency divider in a cross-connected, master-slave D-latch configuration can be used for quadrature generation, which is shown in Fig. 6.2a. When the input signal has a 50% duty cycle, the differential output signals (0,180 and 90,270) are in a 90 degree phase shift. The properties that make the divider an attractive choice for quadrature generation are the wide operating bandwidth, the robust operation, and the large output signal swing. The divider can be designed to operate from DC to very high frequencies and the large output swing reduces the

buffering needs in the LO chain and, thus, the power consumption. Additionally, due to the fact that the input and output frequencies of the divider are at different frequencies, the divider exhibits less LO pulling and LO leakage [15]. The divider also has drawbacks. If the divider needs to drive a substantial capacitive load (e.g., mixer gate), the current consumption can become large. Furthermore, the fast toggle speed of the divider requires the use of small transistor dimensions, which incurs a penalty in the form of increased mismatch and, hence, reduced IRR performance. Despite its drawbacks, the divider is used widely to generate quadrature signals. Further details on dividers and D-latch implementations can be found, for example, in [161–167]. In this thesis dividers were used in the receivers reported in publications [I-V].

6.1.2 Passive polyphase filters

First-order passive RC networks can be used for quadrature generation, but their use in practical applications is difficult due to their limited amplitude and phase accuracy. Instead, multiple passive RC filters can be cascaded in a passive polyphase filter to improve the amplitude and phase accuracy. Figure 6.2b shows a 2-stage passive polyphase filter as an example. The inputs of the I branches (CLK,CLKX) are connected to a balanced sinusoidal signal input, while the inputs of the Q branches are floating. This type of input configuration, which is referred to as type-I PPF [168], results in a 90 degree phase balance at the output, but it has perfect magnitude balance only at certain frequencies. The type-II topology, which is presented in Fig. 6.3, feeds the input signals to both the I and Q branches, which results in a unity magnitude balance across frequency, but a 90 degree phase difference only at specific frequencies. The relative matching of capacitors and resistors in an IC process is good, and thus PPFs can provide very high IRRs. However, the absolute value of the passives varies greatly so the RC product can be, e.g., 30% higher than intended. The frequency range where a specific IRR value is achieved is limited by this variation. To broaden the IRR range, the number of cascaded stages can be increased, but it is typically limited to 2–4 due to the additional loss, which is added by the PPF stage. Component tuning can also be used to improve the operating bandwidth at the cost of additional hardware and losses associated with the switches used in the tuning banks. In this thesis, passive polyphase filters were implemented in the receivers reported in [III, IV]. Further examples of PPFs are found, for instance,

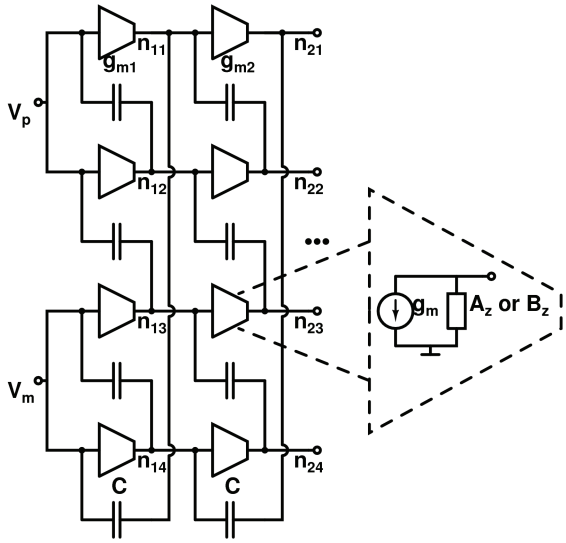


Figure 6.3. Active polyphase filter schematic (type-II) [VI].

in [169–173].

6.2 Active polyphase filter design

Passive polyphase filter implementation is known to require passives of a good quality, which is no longer self-evident with modern CMOS processes. Furthermore, the tuning of the passive polyphase filters results in additional losses in the filter, as was previously mentioned. Therefore, with the high-speed transistors and simple g_m elements available [174, 175], active polyphase filters (APPF) have become an attractive possibility [176, 177]. The benefits of APPF include the possibility for filter calibration, tuning, and signal amplification. However, due to the nature of the APPFs, they have a tendency to become unstable. This issue has been analyzed in [VI]. This section will discuss the most important results from the APPF analysis. Additionally, the filter implementation in [VII] is discussed and the experimental results are shown at the end of the section. Further details are presented in [VI, VII].

6.2.1 Active polyphase filter analysis

The classical polyphase filter has already been analyzed thoroughly, e.g., in [168]. Many of the details presented in the analysis hold true for APPFs as well. However, there are also several differences with the APPF com-

pared to the passive polyphase filter, which are analyzed in [VI]. Figure 6.3 illustrates a two-stage topology of an active polyphase filter that was used for the analysis and implementation. For this analysis, we used input signaling, shown in Fig. 6.3, which has an equivalent magnitude response for the I and Q branches. The input signaling can also be modified to type-I topology (Fig. 6.2b) to provide an equal phase response [168].

In Fig. 6.3, g_m is used to denote the transconductance of the element instead of the passive polyphase filter resistance. In addition, the g_m element's non-idealities are included and denoted with A_z and B_z for stages 1 and 2, respectively. They can be expressed as

$$A_z = sC_1 + G_1 = \frac{g_{m1}}{A_{DC}}(\frac{s}{\omega_{-3dB}} + 1), \tag{6.4}$$

$$B_z = sC_2 + G_2 = \frac{g_{m2}}{A_{DC}}(\frac{s}{\omega_{-3dB}} + 1), \tag{6.5}$$

where C_1 and C_2 are the intrinsic output capacitances and G_1 and G_2 are the finite output conductances of the elements. They have been expressed with the help of the element transconductance (g_m), the DC gain (A_{DC}), and the intrinsic –3-dB pole frequency (ω_{-3dB}).

Based on the analysis of the 1-stage filter [VI], it can be concluded that the maximum gain of the filter is 3 dB when the non-idealities are removed. To avoid excessive gain degradation, the results suggest that the intrinsic pole of an element should be designed to be higher than the filter pole frequency. Additionally, the analysis provided in [VI] demonstrated that the 1-stage filter is always stable if the input configuration is connected in the manner shown in Fig. 6.3.

For the 2-stage filter, the closed form transfer function for the differential signal is always stable, i.e., the poles of the transfer function always remain in the left half-plane. However, by solving the single-ended transfer function concerning, e.g., node n21, the instability of the APPF becomes evident. The stability is determined by the denominator poles, i.e., when the poles move to the right half-plane, the transfer function becomes unstable. The relative stability factor S is therefore determined as the denominator imaginary part divided by the real part, or as the Q-factor of the denominator. Publication [VI] demonstrates that the stability condition of the 2-stage filter can be expressed as

$$S = \frac{(3-k)A_{DC} - (1-k)A_{DC}^2 + 2(1-k^2)/p}{A_{DC}^2 + (1-k^2) + A_{DC}(3-k)/p + (1-k^2)/p^2}, \tag{6.6}$$

where k is the pole-splitting factor of the two filter poles relative to the

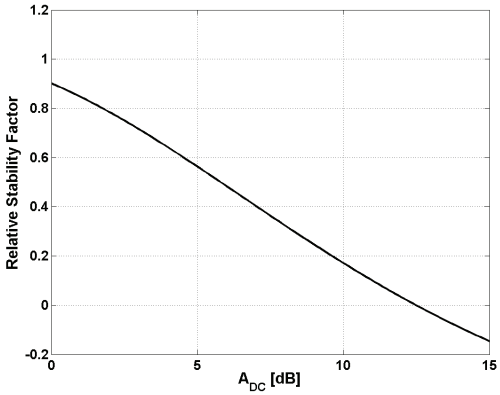


Figure 6.4. Stability of the 2-stage filter compared to the g_m element DC gain [VI].

filter center frequency [168]:

$$\omega_{1/2} = \omega_c(1 \pm k). \tag{6.7}$$

The variable p is the intrinsic pole factor ($\omega_{-3dB} = p\omega_c$) of an element relative to the filter center frequency.

The condition for stability is that S must remain positive. By studying (6.6), we see that the term determining whether or not the numerator becomes negative is formed by the pole-splitting factor, k, and g_m element DC gain, A_{DC}. In theory a large pole-splitting factor k could make the denominator negative, but in practice the pole splitting factor is near zero and thus the numerator determines the stability condition.

The key results of the stability analysis are the stability compared to the g_m element's DC gain and the stability compared to the filter's pole-splitting factor, k. The relative stability factor as a function of the g_m element's DC gain is presented in Fig. 6.4, where it can be seen that the stability decreases as the DC gain is increased, which was to be expected. The stability threshold is approximately 12 dB in this case. In Fig. 6.5, the stability, S, is shown as a function of the pole-splitting factor, k. The figure clearly shows that choosing the first filter pole at a higher frequency (positive k) results in a more stable design.

6.2.2 Active polyphase filter implementation

The implemented filter uses the same topology as was used in the analysis (Fig. 6.3). The transconductances in the filter are tunable via a bias current, while the filter capacitors are unity capacitors denoted by the variable C. The targeted operating frequency of this filter was 0.5 to 5 GHz

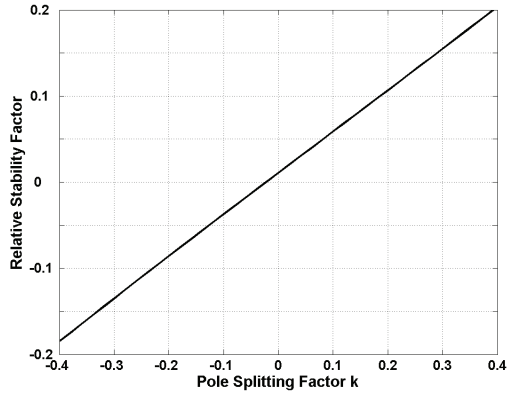


Figure 6.5. Stability of the 2-stage filter compared to the pole-splitting factor k [VI].

with an IRR of 40 dB, which makes it suitable for the majority of wireless applications in the frequency range. Implementing the same frequency range with a passive filter would render either an impractical number of filtering stages or a large tuning matrix whose performance would be limited by the parasitics. If a divider was used instead, then the synthesizer would have to be able to provide an LO signal from 1 to 10 GHz with a high signal level.

The designer has the freedom to choose the g_m element sizes and the order of the filter stages. If a larger transconductance is used as the first stage, then the filter gain will be higher, but if it is used as the last stage, then the frequency response will be flatter. Moreover, a larger transconductance is capable of driving a larger capacitive load, which is usually desired. The highest transconductances were designed at 3.1 and 5.8 mS for the two filter stages, g_{m1} and g_{m2}, respectively. With the filter capacitance set at 205 fF, these transconductances translate to filter poles at 2.4 and 4.5 GHz, respectively. The minimum g_m values were designed at 0.9 and 1.5 mS, which translate to filter poles at 0.7 and 1.2 GHz, respectively. With these transconductance values, the filter is able to cover the entire targeted frequency band with an IRR better than 40 dB.

The schematic of the g_m element is presented in Fig. 6.6. The element consists of a differential inverter, stabilizing feedback, current mirrors, and a common-mode feedback (CMFB) circuitry. The effective transconductance of the element is set by the g_m of transistors M_1 and M_3. The resistive feedback between the input and the output serves two purposes: It provides a bias voltage to the gate of the amplifying transistors and it reduces the DC gain of the element. The transconductance value of

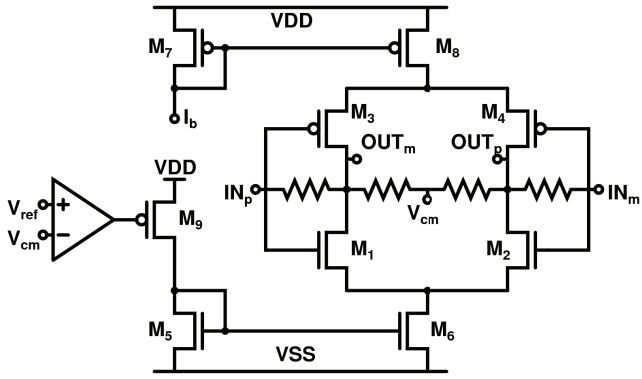


Figure 6.6. Active polyphase filter g_m-element schematic [VII].

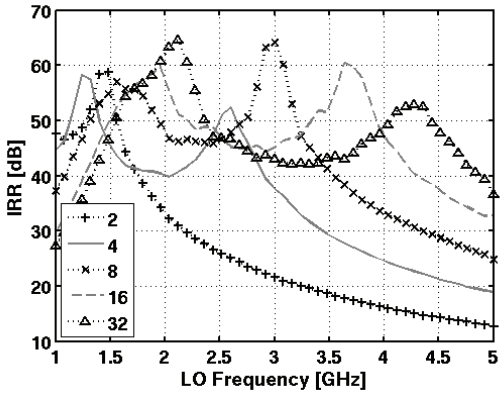


Figure 6.7. Compensated IRR responses with different APPF biasing codes [VII].

the element can be adjusted by varying the input bias current, I_b, to the PMOS current mirror. The current can be adjusted with a 5-bit current-steering current-mirror, which provides 32 current levels. Additionally, the current-mirrors provide common-mode rejection (CMR) for the g_m element. CMFB and CMR also allow for the use of a higher DC gain without violating the stability of the filter. Large resistors at the output are used to sense the common-mode voltage of the element. This voltage is supplied to the operational amplifier, which adjusts the current source, M_9, such that the correct output voltage level is maintained. This is necessary to maintain correct biasing when the input bias current is adjusted. Moreover, the APPF exhibits DC pulling of the I and Q branches in opposite directions, which must be compensated for with the CMFB in order to avoid g_m mismatch and thus a degrading of the IRR.

6.2.3 Experimental results

The circuit was fabricated using a 1.2-V, 65-nm CMOS process. The measurement setup included a 1–12-GHz hybrid at the LO input. This limited the lowest input frequency in the measurements to 1 GHz. The measurements were conducted on a test receiver with an LNA, a mixer, a baseband section, and an LO chain containing the APPF (see Fig. 1 in VII for a block diagram). The four baseband output signals of the receiver (differential I and Q branches) at 1 MHz were measured simultaneously with a 20 GHz oscilloscope after being down-converted by the mixer. Because it was not possible to directly measure the I and Q errors of the APPF from the input of the mixer in the receiver, we have compensated for the static errors of the baseband and the mixer in the measured results to show a more insightful result for the tuning characteristics of the APPF filter. Figure 6.7 shows the IRR frequency responses when the average static error for the amplitude and phase imbalance is compensated for based on the measured results. The results clearly show that the APPF IRR response tunes from 1 to 5 GHz with an IRR better than 40 dB when the bias code is adjusted. The current consumption of the APPF between the minimum and maximum bias codes is 0.7 and 4.4 mA, respectively. To the author's knowledge, this is the first demonstration of an active polyphase filter tuning for a LO quadrature drive.

6.3 Duty-cycle generation

6.3.1 Logic and division based approaches

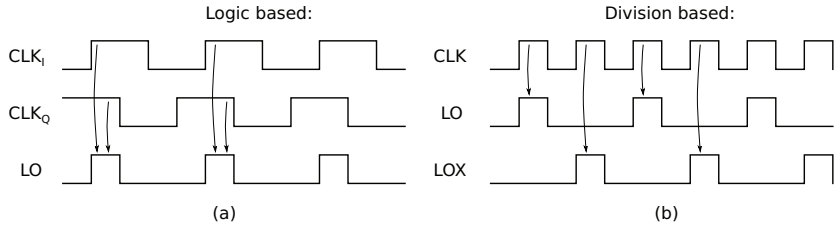


Figure 6.8. 25% duty-cycle generation principle via a (a) logic combination and (b) clock division.

As has been previously stated in this thesis, the passive mixer and N-path filters benefit from using a 25% duty-cycle LO signal. Such a signal can be generated by a logic combination approach where two clock signals

in quadrature are combined using an AND logic to produce a 25% duty cycle, as shown in Fig. 6.8a [134, 135], [IV]. The quadrature signals can be generated by a PPF or a divide-by-2 circuit. In the former case, the input clock frequency will be same as the LO frequency and can potentially lead to LO-pulling problems when used in conjunction with a PA. In the latter case, the input frequency will be twice the LO frequency and will thus avoid LO-pulling phenomena, but according to [134], the flicker noise of the dividers tends to degrade the mixer noise figure. To resolve this problem, the quadrature signal from the divider can be combined with the original double frequency input clock signal [134].

Another method for generating a 25% duty cycle is by frequency division, as depicted in Fig. 6.8b. With this approach, a shift-register-based Johnson divider can be used to select the individual high states from the original clock waveform, as shown in Fig. 6.8b. As was mentioned, divider circuits suffer from flicker noise and any further buffering before the mixer contributes additional uncorrelated LO noise. In the case of a single-ended passive mixer, this uncorrelated noise couples to the RF input and down-converts onto the signal band. In a differential mixer, a single LO phase drives two mixer switches, thereby coupling the noise as a common-mode signal that can be rejected by the differential baseband. In the single-ended case, the divider can be modified such that there is only one transistor that contributes additional uncorrelated noise [127]. However, buffers cannot be used before the mixer, which increases the drive-strength requirements and power consumption of the divider.

6.3.2 Analog feedback approach

With the mixer-first receiver topology, the LO signal chain waveform is emphasized, since it directly affects the noise, linearity, and bandwidth performance of the receiver. Therefore, it is desirable to be able to fine-tune the LO signal duty cycle, which is not possible with the logic- or division-based approaches.

The implementation and operating principle of the duty-cycle control with the analog feedback approach is presented in Fig. 6.9a. The DC component of the LO signal is linearly related to the duty cycle, as depicted in Fig. 6.9b. Therefore, by sampling the DC voltage of the output LO signal and comparing it to a reference voltage, we can offset the inverter chain bias points (Vb1 to Vb4) such that the resulting signal has the desired duty cycle. The bias network schematic is presented in Fig. 6.10, where it

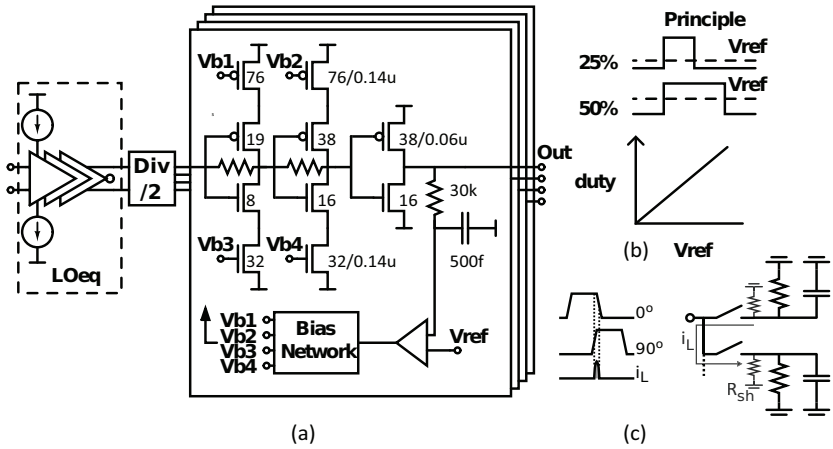


Figure 6.9. (a) LO path block diagram with a duty-cycle control, (b) operating principle, and (c) leakage mechanism with overlapping LO pulses [V].

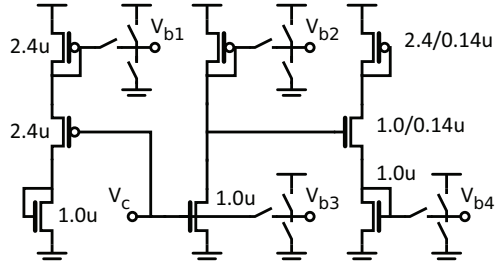


Figure 6.10. LO duty cycle control bias circuitry. All NMOS transistors are $1.0/0.14\mu m$ and PMOS transistors are $2.4/0.14\mu m$.

can seen how the input V_c is mirrored to the bias voltages Vb1 to Vb4. For example, for duty cycle of 25% the bias voltages Vb1 and Vb3 are adjusted up to bring down voltage at the inverter output. Likewise, the voltages Vb2 and Vb4 are adjusted down to raise the output voltage of the second controlled inverter. The net result is that the output DC level of the last inverter drops to equal that of the set duty cycle signal. Each of the inverter chains has a separate feedback that equalizes differences in the gain and offsets. However, phase differences between the input signals are not equalized. Additionally, the duty-cycle control helps to maintain signal waveform integrity at higher frequencies, where the LO clock signal is less ideal, by compensating for the inverter bias points in order to boost the gain as the frequency increases.

The feedback operational amplifier together with the inverter chain introduce a significant amount of DC gain to the loop. To ensure stability, the loop has been designed with a phase margin of 57° in [V]. The reference voltage for the operational amplifier is generated with a 3-bit resis-

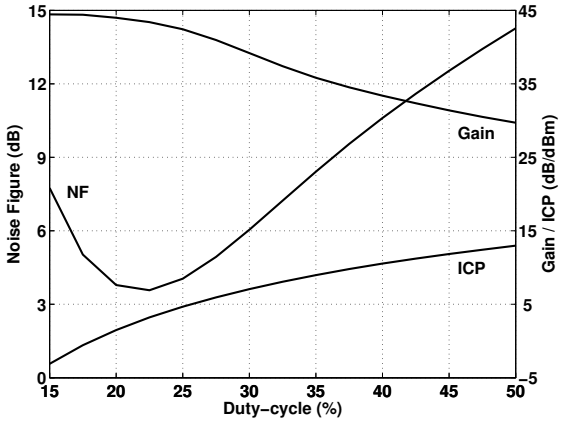


Figure 6.11. Mixer-first receiver gain, noise figure, and blocker input compression point as a function of the LO duty-cycle control [V].

tor network, which allows us to control the duty cycle from 15 to 52.5% in 2.5-% steps. When the duty-cycle code exceeds 25%, the switches in the passive mixer start to conduct simultaneously. This creates a leakage current, i_L, from one baseband branch to another through the mixer switches, as is depicted in Fig. 6.9c. The gain and the noise figure of the mixer-first receiver degrade as a direct consequence of this leakage, but simultaneously the linearity is also improved.

To demonstrate the effectiveness of the feedback duty-cycle control, it was implemented in the LO chain of a mixer-first receiver presented in V. Figure 6.11 presents the performance of the receiver with different duty-cycle values at an RF frequency of 1 GHz. There is a clear optimal point for the receiver NF (3.5 dB) between duty cycles of 20 and 25%, which is where minimum switch resistance and signal leakage can simultaneously be achieved. Increasing the duty cycle further decreases the effective series resistance of the mixer switches and causes the LO phases to overlap, which results in the signal leaking from one branch to another, as was explained earlier. This decreases the signal gain, degrades the NF, and improves the –1-dB blocker input compression point from –3 to +13 dBm, as depicted in Fig. 6.11. This result demonstrates that noise and linearity performance can be exchanged by 10 dB by adjusting the duty cycle from 25 to 50%.

6.4 Requirements of wideband LO drive and quadrature generation

When designing LO quadrature generation for a receiver, there are several design factors that affect the choice of the quadrature implementation technique. First and foremost are the implementation frequency and the range that it must cover. While dividers are inherently wideband, they suffer from two limiting properties. Since the divider halves the input frequency (divide-by-2), it doubles the required input frequency and tuning range for any given application, and higher order division ratios exacerbate the requirements even further. For wideband and high-frequency applications, this property increases the requirements of the frequency synthesizer considerably.

Passive and active polyphase filters operate at the same frequency as the synthesizer, which, in contrast to the dividers, can cause LO leakage and pulling issues. With PPFs, a single filter stage can cover only a narrow band and thus the bandwidth of the LO chain is increased by cascading filter stages designed for different frequencies. With passive PPFs, this also increases the attenuation of the filter, which has to be compensated for by means of buffering; this comes at the expense of die area and power. The number of filter stages needed depends on the IRR requirement and bandwidth [168]. Typically, the number of stages in the PPF is limited to 2-4 and the only way to increase the bandwidth of the filter further for a certain IRR level is to make the filter stages tunable. For the passive PPF, this means that either the resistors or capacitors are made tunable by using switches or varactors. This introduces additional capacitance, resistance, and non-linearity that degrade the filter performance. For the active PPF, realized with g_m elements, the tuning of the filtering stages can be done simply by adjusting the g_m values. With proper g_m element design, this can be achieved by adjusting the bias current of the element, thus removing the need for switches and passive component matrixes in the filter itself, as was discussed in Section 6.2. However, the APPF must incorporate some form of calibration to properly tune the amplitude and phase balance when it is used in a larger system.

Of the three implementation techniques, the divider typically has the smallest layout size. When the supply stabilization capacitors that are needed with the divider are also considered, the difference between the topologies becomes smaller. The layout area for non-tunable passive and active PPFs is relatively equal, but for a tunable implementation, the

active filter consumes clearly less die area than the passive filter.

While the passive PPF consumes no power, it attenuates the input signal and thus it needs the most buffering of the three to achieve a given signal level at the mixer, which increases its power budget. The power consumption of the divider and the active PPF depends on the implementation frequency, but for typical wireless applications it is in the same order of magnitude for both implementations. However, the divider produces a near full-scale signal and thus the buffering needs are lower than for an active PPF. On the other hand, the divider requires a relatively large input signal to operate, while the active and passive PPFs can operate across a wider input signal power range. The mixer type also affects the amount of buffering needed since active mixers operate typically with smaller LO signal amplitudes than their passive counterparts. When the overall power consumption is considered, there is no clear rule as to which method leads to an optimal result and the correct choice depends on the system.

Spectral purity is another issue that needs to be considered in the LO chain design. While the system blockers and transmission spectral mask define the required phase noise and spurious tones requirements that mainly affect the synthesizer design, the quadrature generation scheme also has an impact. Of the three, the passive PPF has the cleanest output waveform due to the linear passive components used in it. The active PPF on the other hand can produce LO harmonics that depend on the input signal level because of the non-linear g_m element used in it. The divider, when locked, produces an output signal that has high a harmonic content and, in wideband applications, this may cause unwanted harmonic folding or emissions.

7. Conclusions

In this thesis the design of wideband receiver circuits for future mobile communications systems has been studied. The circuit structures presented in this thesis are based on flexible wideband solutions that are not bound to a specific system or frequency band. This work contributes to the mobile receiver research field by providing circuit solutions that will make it possible to develop better flexible wideband receivers in the future.

The multisystem, multiband problem in mobile terminals drives up the cost and complexity of radios by requiring separate dedicated signal paths with discrete filtering. By removing the filters, the radios could be made more cost-efficient and flexible and the signal path design would be simplified. However, with receivers this demands that the front-end is capable of withstanding an extremely harsh interference environment while still providing good sensitivity. This thesis concentrates on improving and developing receiver circuits that provide a wide reception bandwidth and selectivity against blockers. The properties of fast CMOS transistors have been successfully utilized, while at the same time novel solutions have been develop for the research problems.

The presented work includes a WiMedia UWB receiver with an active baseband filter and a synthesizer, which was described in [I]. The front-end consisted of a 2-stage LNA, a wideband buffer, and an active mixer. The challenge in this work was to achieve a 1.6-GHz gain and matching bandwidth simultaneously with a minimal amount of inductors and competitive performance. The work proposed the use of a dual-feedback topology for the LNA, which provides wideband matching with only one inductor in the shunt-peaked load. The receiver achieved a 60-dB maximum gain and an NF better than 6.2 dB in BG1 mode. Additionally, in [II] a 60-GHz receiver utilizing the UWB front-end as an IF stage was implemented. The proof-of-concept demonstrates the feasibility of a 60-

GHz broadband receiver with an ADC in deep-submicron CMOS. Despite the high level of integration, the receiver compares favorably with other state-of-the-art millimeter-wave receivers published at the same time.

One major topic in this thesis has been the use of an N-path filter in receiver applications. The first of the N-path works explored the effectiveness of N-path filtering in a wideband LNA [III]. It was found that the low load impedance presented by the wideband amplifier limited the selectivity achievable with the N-path filter to 6 dB. The use of the 50-% duty cycle also limited the selectivity in this case. When the filter was turned on, a 1.5-dB NF increase was measured and the LO leakage due to the N-path filter at the input was -63 dBm.

The second N-path receiver studied the effectiveness of the N-path filter used in a feedback configuration around a 2–6-GHz LNA [IV]. An adjustable PPF structure was proposed to compensate for the frequency response shift in the feedback loop and thus to shift the closed-loop response to the desired frequency. A model for the closed-loop system was derived using frequency transformation and parameterization. The analysis results showed that in order to maximize selectivity, the forward gain should be maximized and the N-path bandwidth and the notch frequency offset minimized while fulfilling stability conditions. The measured results showed a 7-dB improvement in the blocker input compression point, while the increase in NF was 1.5 dB at a 4.0-GHz reception frequency.

The third N-path work was a concept demonstrator of a wideband, mobile-handset sized, single-antenna, mixer-first receiver [V]. The work included the system considerations for the antenna-IC interface. Special attention in the design was paid to the interface impedances between the antenna and the IC. From the trade-off study presented in this thesis, it was concluded that in terms of the noise, linearity, power, and operating bandwidth of the receiver, it is desirable to choose a high interface impedance. On the other hand, the CCE antenna has an inherently low unbalanced radiation resistance, so a reasonable compromise was needed. We used a 1:4 impedance transforming balun to satisfy the higher input impedance requirement. The mixer-first receiver IC demonstrated a NF of 3.2 to 5 dB, without 1-dB balun loss, and a blocker ICP of +5 dBm, while occupying only 0.3 mm^2 of active die area. Additionally, an LO duty-cycle adjustment was proposed as a means to regulate the LO signal and trade-off the receiver performance by 10 dB. The performance of the IC was comparable to that in other state-of-the-art, linear receivers pub-

lished recently. The system measurements with the CCE antenna showed that we were able to maintain the performance of the receiver with only a slight degradation. The interface arrangement proved that the low-resistance CCE antenna and the high-input impedance receiver can successfully be made interoperable. To the author's knowledge, this was the first demonstration of a compact-size, single-antenna, single-input, mixer-first receiver covering the LTE bands from 0.7 to 2.7 GHz.

Finally, wideband LO circuitry was also studied in this thesis. In addition to the duty-cycle control circuitry presented in [V], an active polyphase filter for wideband quadrature signal generation was studied in [VI, VII]. The gain and stability of 1- and 2-stage active polyphase filters were analyzed. An analytical equation for the 2-stage stability condition was derived. The results showed that, for the APPF to remain stable, there is a predictable limit for the gain, pole frequencies, and intrinsic capacitance of the g_m element. The analysis provides a means for designing APPFs with optimal gain, IRR, and bandwidth while still remaining stable. This was demonstrated in [VII], where a 1-to-5-GHz APPF was implemented. The filter achieved an IRR better than 40 dB over the operating band.

The results presented in each publication in this thesis take the mobile receiver closer to the ideal receiver mentioned in Section 1.2. With the solutions presented here, the receiver can be made more flexible and linear so that some of the costly pre-select filters may be simplified or removed. Based on the work presented in this thesis, the research in our group will continue to focus on flexible and interference-tolerant receiver circuits. Important topics include improving the selectivity and linearity, the harmonic mixing dilemma, the reciprocal mixing of the LO phase noise, and the use of digitally-intensive circuit structures in receivers. Since the mobile communication industry is evolving rapidly, even completely new approaches that revolutionize the receiver can emerge. What the exact solutions will be in the future remains a mystery, but it can be expected that they will take advantage of the ever-decreasing feature size of the CMOS technology.

Bibliography

[1] J. Crols and M. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 3, pp. 269–282, 1998.

[2] J. Rudell, J.-J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, "A 1.9 GHz wide-band IF double conversion CMOS integrated receiver for cordless telephone applications," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 1997, pp. 304–305.

[3] E. Armstrong, "The super-heterodyne - its origin, development, and some recent improvements," *Proceedings of the IRE*, vol. 12, no. 5, pp. 539–552, Oct. 1924.

[4] R. Hartley, "Modulation system," U.S. Patent 1,666,206, April 17, 1928.

[5] D. Weaver, "A third method of generation and detection of single-sideband signals," *Proceedings of the IRE*, vol. 44, no. 12, pp. 1703–1705, 1956.

[6] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, 2011.

[7] ——, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 52–65, 2012.

[8] F. M. Colebrook, "Homodyne," *Wireless World and Radio Review*, vol. 13, pp. 645–648, 1924.

[9] A. A. Abidi, "Direct-conversion radio tranceivers for digital communications," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1399–1410, 1995.

[10] J. F. Wilson, R. Youell, T. H. Richards, G. Luff, and R. Pilaski, "A single-chip VHF and UHF receiver for radio paging," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 12, pp. 1944–1950, 1991.

[11] J. Ryynänen, S. Lindfors, K. Stadius, and K. A. I. Halonen, "Integrated circuits for multiband multimode receivers," *IEEE Circuits and Systems Magazine*, vol. 6, no. 2, pp. 5–16, 2006.

[12] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, pp. 428–435, 1997.

[13] K. Kivekäs, A. Pärssinen, J. Ryynänen, J. Jussila, and K. Halonen, "Calibration techniques of active BiCMOS mixers," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 766–769, 2002.

[14] J. Jussila, "Analog baseband circuits for WCDMA direct conversion receivers," Ph.D. dissertation, Helsinki University of Technology, Espoo, Finland, 2003, p. 247.

[15] B. Razavi, *RF Microelectronics*. Prentice-Hall, 1998, p. 335.

[16] V. Saari, "Continous-time low-pass filters for integrated wideband radio receivers," Ph.D. dissertation, Aalto University, Espoo, Finland, 2011, p. 230.

[17] (2013, June) A short history of radio. [Online]. Available: www.fcc.gov/omd/history/radio

[18] T. Cover and J. Thomas, *Elements of Information Theory*. John Wiley & Sons, 2006, p. 576.

[19] C. E. Shannon, "A mathematical theory of communications," *Bell System Technical Journal*, vol. 27, pp. 379–423 and 623–656, July and Oct. 1948.

[20] B. Razavi, T. Aytur, C. Lam, F. R. Yang, R. H. Yan, H. C. Kang, C. C. Hsu, and C. C. Lee, "Multiband UWB tranceivers," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, USA, Sept. 2005, pp. 141 – 148.

[21] A. Batra, G. Balakrishnan, G. R. Aiello, F. J. R., and A. Dabak, "Design of a multiband OFDM systems for realistic UWB channel environments," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 2123–2138, 2004.

[22] M. Hämäläinen, V. Hovinen, R. Tesi, J. Iinatti, and M. Latva-aho, "On the UWB system coexistence with GSM900, UMTS/WCDMA, and GPS," *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 9, pp. 1712–1721, 2002.

[23] A. Molisch, J. Foerster, and M. Pendergrass, "Channel models for ultrawideband personal area networks," *IEEE Wireless Communications*, vol. 10, no. 6, pp. 14–21, 2003.

[24] K. Mandke, H. Nam, L. Yerramneni, C. Zuniga, and T. Rappaport, "The evolution of ultra wide band radio for wireless personal area networks," *High Frequency Electronics*, vol. 2, no. 5, pp. 22–32, Sept. 2003.

[25] C. Mishra, A. Valdes-Garcia, F. Bahmani, A. Batra, E. Sanchez-Sinencio, and J. Silva-Martinez, "Frequency planning and synthesizer architectures for multiband OFDM UWB radios," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 12, pp. 3744–3756, 2005.

[26] R. Harjani, J. Harvey, and R. Sainati, "Analog/RF physical layer issues for UWB systems," in *IEEE Proceedings of VLSI Design*, Mumbai, India, Jan. 2004, pp. 941–948.

[27] (2013, June) High rate ultra wideband PHY and MAC standard, ECMA standard 368,. [Online]. Available: http://www.ecma-international.org/publications/standards/Ecma-368.htm

[28] (2009, Dec.) WiMedia PHY Specification, Release 1.5. [Online]. Available: http://www.wimedia.org/en/docs/10003r02WM_CRB-WiMedia_PHY_Spec_1.5.pdf

[29] *3GPP Technical Specification 45.005 Release 10*, 3GPP Std., Mar. 2013. [Online]. Available: www.3gpp.org/ftp/Specs/html-info/45005.htm

[30] *3GPP Technical Specification 25.101 Release 10*, 3GPP Std., July 2013. [Online]. Available: www.3gpp.org/ftp/Specs/html-info/25101.htm

[31] *ETSI TS 136 101 V10.10.0 LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception*, ETSI/3GPP Std., July 2013. [Online]. Available: www.3gpp.org/ftp/Specs/html-info/36101.htm

[32] *802.11 IEEE Standard for Infromation technology - Telecommunications and infromation exchange between systems - Local and metropolitan area networks - Specific requirements, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications.*, IEEE Std., 2007. [Online]. Available: http://standards.ieee.org/getieee802/download/802.11-2007.pdf

[33] *Global Positioning System Standard Positioning Service Performance Standard.*, Gps.gov Std., Sept. 2008. [Online]. Available: http://www.pnt.gov/public/docs/2008/spsps2008.pdf

[34] A. Pärssinen, "Multimode-multiband transceivers for next generation of wireless communications," in *Proceedings of the European Solid-State Circuits Conference*, Helsinki, Finland, Sept. 2011, pp. 25–36.

[35] J. Mitola, "The software radio architecture," *IEEE Communications Magazine*, vol. 33, no. 5, pp. 26–38, 1995.

[36] F. Rivet, Y. Deval, J. Begueret, D. Dallet, P. Cathelin, and D. Belot, "The experimental demonstration of a SASP-based full software radio receivers," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 979–988, 2010.

[37] R. Schiphorst, F. Hoeksema, and C. Slump, "The front end of software-defined radio: Possibilities and challenges," in *Annual CTIT Workshop on Mobile Communications*, Enschede, The Netherlands, Feb. 2001, pp. 1–4.

[38] R. Walden, "Performance trends for analog to digital converters," *IEEE Communications Magazine*, vol. 37, no. 2, pp. 96–101, 1999.

[39] W. H. W. Tuttlebee, "Software-defined radio: facets of a developing technology," *IEEE Personal Communications*, vol. 6, no. 2, pp. 38–44, 1999.

[40] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. Abidi, "An 800-MHz – 6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, 2006.

[41] Z. Ru, N. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, 2009.

[42] J. Craninckx, "CMOS software-defined radio transceivers: Analog design in digital technology," *IEEE Communications Magazine*, vol. 50, no. 4, pp. 136–144, 2012.

[43] H. Holma and A. Toskala, *WCDMA for UMTS: HSPA Evolution and LTE*. John Wiley & Sons, 2010, p. 576.

[44] H. Darabi, P. Chang, H. Jensen, A. Zolfaghari, P. Lettieri, J. Leete, B. Mohammadi, J. Chiu, Q. Li, S.-L. Chen, Z. Zhou, M. Vadipour, C. Chen, Y. Chang, A. Mirzaei, A. Yazdi, M. Nariman, A. Hadji-Abdolhamid, E. Chang, B. Zhao, K. Juan, P. Suri, C. Guan, L. Serrano, J. Leung, J. Shin, J. Kim, H. Tran, P. Kilcoyne, H. Vinh, E. Raith, M. Koscal, A. Hukkoo, C. Hayek, V. Rakhshani, C. Wilcoxson, M. Rofougaran, and A. Rofougaran, "A Quad-Band GSM/GPRS/EDGE SoC in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 870–882, 2011.

[45] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly integrated and tunable RF front ends for reconfigurable multiband transceivers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 9, pp. 2038–2050, 2011.

[46] S. Abdelhalem, P. Gudem, and L. Larson, "Hybrid transformer-based tunable differential duplexer in a 90-nm CMOS process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1316–1326, 2013.

[47] J. Mitola and J. Maguire, G.Q., "Cognitive radio: making software radios more personal," *IEEE Personal Communications*, vol. 6, no. 4, pp. 13–18, 1999.

[48] D. Cabric, I. O'Donnell, M.-W. Chen, and R. Brodersen, "Spectrum sharing radios," *IEEE Circuits and Systems Magazine*, vol. 6, no. 2, pp. 30–45, 2006.

[49] D. Cabric and R. Brodersen, "Physical layer design issues unique to cognitive radio systems," in *IEEE 16th International Symposium on Personal, Indoor and Mobile Radio Communications*, Berlin, Germany, Sept. 2005, pp. 759–763.

[50] D. Cabric, S. Mishra, and R. Brodersen, "Implementation issues in spectrum sensing for cognitive radios," in *Conference Record of the Thirty-Eighth Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, USA, Nov. 2004, pp. 772–776.

[51] V. Turunen, M. Kosunen, M. Vääräkangas, and J. Ryynänen, "Correlation-based detection of OFDM signals in the angular domain," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 3, pp. 951–958, 2012.

[52] M. Sahin and H. Arslan, "System design for cognitive radio communications," in *1st International Conference on Cognitive Radio Oriented Wireless Networks and Communications*, Mykonos Island, Greece, June 2006, pp. 1–5.

[53] B. Razavi, "Challenges in the design of cognitive radios," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, USA, Sept. 2009, pp. 391–398.

[54] ——, “Cognitive radio design challenges and techniques,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1542–1553, 2010.

[55] P. Orsatti, F. Piazza, and Q. Huang, “A 20-mA-receive, 55-mA-transmit, single-chip GSM transceiver in 0.25-μm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, pp. 1869–1880, 1999.

[56] A. Pärssinen, “Direct conversion receivers in wide-band systems,” Ph.D. dissertation, Helsinki University of Technology, Espoo, 2000, p. 235.

[57] A. Loke and F. Ali, “Direct conversion radio for digital mobile phones-design issues, status, and trends,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 11, pp. 2422–2435, 2002.

[58] J. Ryynänen, “Low-noise amplifiers for integrated multi-mode direct-conversion receivers,” Ph.D. dissertation, Helsinki University of Technology, Espoo, 2004, p. 138.

[59] J. Kaukovuori, “CMOS radio frequency circuits for short-range direct-conversion receivers,” Ph.D. dissertation, Helsinki University of Technology, 2007, p. 201.

[60] D. Leenaerts, J. Tang, and C. Vaucher, *Circuit Design for RF Transceivers*. Kluwer Academic Publishers, 2002, p. 323.

[61] G. Girlando and G. Palmisano, “Noise figure and impedance matching in RF cascode amplifiers,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 11, pp. 1388–1396, 1999.

[62] R. Valkonen, “Impedance matching and tuning of non-resonant mobile terminal antennas,” Ph.D. dissertation, Aalto University, Espoo, 2013, p. 149.

[63] A. Rofougaran, G. Chang, J. Rael, J.-C. Chang, M. Rofougaran, P. Chang, M. Djafari, M.-K. Ku, E. Roth, A. Abidi, and H. Samueli, “A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS. I. Architecture and transmitter design,” *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 515–534, 1998.

[64] K. Simons, “The decibel relationships between amplifier distortion products,” *Proceedings of the IEEE*, vol. 58, no. 7, pp. 1071–1086, 1970.

[65] R. Meyer and A. Wong, “Blocking and desensitization in RF amplifiers,” *IEEE Journal of Solid-State Circuits*, vol. 30, no. 8, pp. 944–946, 1995.

[66] A. Springer, L. Maurer, and R. Weigel, “RF system concepts for highly integrated RFICs for W-CDMA mobile radio terminals,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 254–267, 2002.

[67] C. Iversen and T. E. Kolding, “Noise and intercept point calculation for modern radio receiver planning,” *IEE Proceedings Communications*, vol. 148, no. 4, pp. 255–259, 2001.

[68] R. Magoon, A. Molnar, J. Zachan, G. Hatcher, and W. Rhee, “A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-n synthesizer,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1710–1720, 2002.

[69] A. Ismail and A. Abidi, "A 3.1- to 8.2-GHz zero-IF receiver and direct frequency synthesizer in 0.18-μm SiGe BiCMOS for mode-2 MB-OFDM UWB communication," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2573–2582, 2005.

[70] A. Bevilacqua and A. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, 2004.

[71] F. Lee and A. Chandrakasan, "A BiCMOS Ultra-Wideband 3.1-10.6-GHz Front-End," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1784–1791, 2006.

[72] R. Kaunisto, "Monolithic active resonator filters for high frequencies," Ph.D. dissertation, Helsinki University of Technology, Espoo, 2000, p. 125.

[73] B. Razavi, T. Aytur, C. Lam, F.-R. Yang, K.-Y. Li, R.-H. Yan, H.-C. Kang, C.-C. Hsu, and C.-C. Lee, "A UWB CMOS transceiver," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2555–2562, 2005.

[74] J. Kaukovuori, J. Ryynänen, and K. A. I. Halonen, "A dual-band direct-conversion RF front-end for WiMedia UWB receiver," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, Honolulu, HI, USA, June 2007, pp. 211–214.

[75] M. Reiha and J. Long, "A 1.2 V Reactive-Feedback 3.1 – 10.6 GHz Low-Noise Amplifier in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1023–1033, 2007.

[76] C. Sandner, S. Derksen, D. Draxelmayr, S. Ek, V. Filimon, G. Leach, S. Marsili, D. Matveev, K. L. R. Mertens, F. Michl, H. Paule, M. Punzenberger, C. Reindl, R. Salerno, M. Tiebout, A. Wiesbauer, I. Winter, and Z. Zhang, "A WiMedia/MBOA-compliant CMOS RF transceiver for UWB," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2787–2794, 2006.

[77] S. Mohan, M. Hershenson, S. Boyd, and T. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, 2000.

[78] S. Shekhar, J. Walling, and D. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, 2006.

[79] F.-T. Chien and Y.-J. Chan, "Bandwidth enhancement of transimpedance amplifier by a capacitive-peaking design," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 8, pp. 1167–1170, 1999.

[80] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, 2004.

[81] E. Klumperink, F. Bruccoleri, and B. Nauta, "Finding all elementary circuits exploiting transconductance," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 11, pp. 1039–1053, 2001.

[82] A. Tanaka, H. Okada, H. Kodama, and H. Ishikawa, "A 1.1V 3.1-to-9.5GHz MB-OFDM UWB transceiver in 90nm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2006, pp. 398–407.

[83] D. Estreich, "A monolithic wide-band GaAs IC amplifier," *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, pp. 1166–1173, 1982.

[84] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto, "An interference robust 0.18 μm CMOS 3.1-8GHz receiver front-end for UWB radio," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, USA, Sept. 2005, pp. 157–160.

[85] D. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *IEEE Radio Frequency Integrated Circuits Symposium*, Forth Worth, TX, USA, June 2004, pp. 97–100.

[86] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. de Gyvez, D. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 12, pp. 875–879, 2005.

[87] J. Borremans, G. Mandal, V. Giannini, T. Sano, M. Ingels, B. Verbruggen, and J. Craninckx, "A 40nm CMOS highly linear 0.4-to-6GHz receiver resilient to 0dBm out-of-band blockers," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2011, pp. 62–64.

[88] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, 2004.

[89] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wide-band balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, 2008.

[90] C.-F. Liao and S.-I. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, 2007.

[91] J. Jussila and P. Sivonen, "A 1.2-V highly linear balanced noise-cancelling LNA in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 579–587, 2008.

[92] J.-H. Zhan and S. Taylor, "A 5GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2006, pp. 721–730.

[93] R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4V 25mW Inductorless Wideband LNA in 0.13μm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2007, pp. 424–613.

[94] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, "Low-area active-feedback low-noise amplifier design in scaled digital CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2422–2433, 2008.

[95] S. Lee, J. Bergervoet, K. Harish, D. Leenaerts, R. Roovers, R. van de Beek, and G. Van Der Weide, "A broadband receive chain in 65nm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2007, pp. 418–612.

[96] R. Van de Beek, J. Bergervoet, H. Kundur, D. Leenaerts, and G. Van Der Weide, "A 0.6-to-10GHz receiver front-end in 45nm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2008, pp. 128–601.

[97] M. Kaltiokallio, J. Kaukovuori, and J. Ryynanen, "Analysis of different feedback topologies to LNA input matching," in *IEEE European Conference on Circuit Theory and Design*, Sevilla, Spain, Aug. 2007, pp. 68–71.

[98] J. Bergervoet, K. Harish, S. Lee, D. Leenaerts, R. Van de Beek, G. Van Der Weide, and R. Roovers, "A WiMedia-compliant UWB transceiver in 65nm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2007, pp. 112–590.

[99] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 4, pp. 365–373, 1968.

[100] H. Zheng, S. Lou, D. Lu, C. Shen, T. Chan, and H. Luong, "A 3.1-8.0 GHz MB-OFDM UWB tranceiver in 0.18μm CMOS," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, USA, Sept. 2007, pp. 651–654.

[101] R. Roovers, D. Leenaerts, J. Bergervoet, K. Harish, R. van de Beek, G. Van Der Weide, H. Waite, Y. Zhang, S. Aggarwal, and C. Razzell, "An interference-robust receiver for ultra-wideband radio in SiGe BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2563–2572, 2005.

[102] A. Valdes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez, and E. Sanchez-Sinencio, "An 11-band 3–10 GHz receiver in SiGe BiCMOS for multiband OFDM UWB communication," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 935–948, 2007.

[103] M. Kaltiokallio, S. Lindfors, V. Saari, and J. Ryynänen, "Design of precise gain GmC-leapfrog filters," in *IEEE International Symposium on Circuits and Systems*, New Orleans, LA, USA, May 2007, pp. 3534–3537.

[104] S. Reynolds, B. Floyd, U. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, 2006.

[105] A. Parsa and B. Razavi, "A 60GHz CMOS receiver using a 30GHz LO," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2008, pp. 190–606.

[106] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60-GHz CMOS receiver front-end with frequency synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, 2008.

[107] B. Afshar, Y. Wang, and A. Niknejad, "A robust 24mW 60GHz receiver in 90nm standard CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2008, pp. 182–605.

[108] S. Pinel, S. Sarkar, P. Sen, B. Perumana, D. Yeh, D. Dawn, and J. Laskar, "A 90nm CMOS 60GHz radio," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2008, pp. 130–601.

[109] J. Lee, Y. Huang, Y. Chen, H. Lu, and C. Chang, "A low-power fully integrated 60GHz transceiver system with OOK modulation and on-board antenna assembly," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2009, pp. 316–317,317a.

[110] A. Tomkins, R. Aroca, T. Yamamoto, S. Nicolson, Y. Doi, and S. Voinigescu, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2085–2099, 2009.

[111] F. Vecchi, S. Bozzola, E. Temporiti, D. Guermandi, M. Pozzoni, M. Repossi, M. Cusmai, U. Decanis, A. Mazzanti, and F. Svelto, "A wideband receiver for multi-Gbit/s communications in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 551–561, 2011.

[112] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.

[113] M. Soer, E. A. M. Klumperink, Z. Ru, F. Van Vliet, and B. Nauta, "A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving >11dBm IIP3 and <6.5 dB NF," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2009, pp. 222–223,223a.

[114] C. Andrews and A. Molnar, "A passive-mixer-first receiver with baseband-controlled RF impedance matching, < 6dB NF, and > 27dBm wideband IIP3," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2010, pp. 46 –47.

[115] J. Borremans, G. Mandal, V. Giannini, T. Sano, M. Ingels, B. Verbruggen, and J. Craninckx, "A 40nm CMOS highly linear 0.4-to-6GHz receiver resilient to 0dBm out-of-band blockers," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2011, pp. 62–64.

[116] D. Murphy, A. Hafez, M. Mikhemar, H. Darabi, M. Chang, and A. Abidi, "A blocker-tolerant wideband noise-cancelling receiver with a 2dB noise figure," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2012, pp. 74–75.

[117] S. Chehrazi, A. Mirzaei, and A. Abidi, "Noise in current-commutating passive FET mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 2, pp. 332–344, 2010.

[118] S. Zhou and M.-C. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, 2005.

[119] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz 1/f noise corner," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, 2005.

[120] W. Liu, X. Jin, J. Chen, M.-C. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P. Ko, and C. Hu, "Bsim 3v3.2 mosfet model users' manual," EECS Department, University of California, Berkeley, Tech. Rep. UCB/ERL M98/51, 1998. [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/1998/3486.html

[121] N. Poobuapheun, W.-H. Chen, Z. Boos, and A. Niknejad, "A 1.5-V 0.7–2.5-GHz CMOS quadrature demodulator for multiband direct-conversion receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1669–1677, 2007.

[122] H. Darabi and A. Abidi, "Noise in RF-CMOS mixers: a simple physical models," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, 2000.

[123] W. Redman-White and D. Leenaerts, "1/f noise in passive CMOS mixers for low and zero IF integrated receivers," in *European Solid-State Circuits Conference*, Villach, Austria, Sept. 2001, pp. 41–44.

[124] H. Khatri, P. Gudem, and L. Larson, "Distortion in current commutating passive CMOS downconversion mixers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 11, pp. 2671–2681, 2009.

[125] A. Shahani, D. Shaeffer, and T. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receivers," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, 1997.

[126] K. Kivekäs, A. Pärssinen, and K. A. I. Halonen, "Characterization of IIP2 and DC-offsets in transconductance mixers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 11, pp. 1028–1038, 2001.

[127] D. Murphy, H. Darabi, A. Abidi, A. Hafez, A. Mirzaei, M. Mikhemar, and M.-C. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.

[128] K. L. Fong and R. Meyer, "Monolithic RF active mixer design," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 231–239, 1999.

[129] J. Weldon, R. Narayanaswami, J. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. Gray, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 2003–2015, 2001.

[130] E. Klumperink, R. Shrestha, E. Mensink, G. Wienk, Z. Ru, and B. Nauta, "Multipath polyphase circuits and their application to RF transceivers," in *IEEE International Symposium on Circuits and Systems*, New Orleans, LA, USA, May 2007, pp. 273–276.

[131] Z. Ru, E. Klumperink, and B. Nauta, "Discrete-time mixing receiver architecture for RF-sampling software-defined radio," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1732–1745, 2010.

[132] Z. Ru, E. Klumperink, C. Saavedra, and B. Nauta, "A 300–800 MHz tunable filter and linearized LNA applied in a low-noise harmonic-rejection RF-sampling receiver," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 967–978, 2010.

[133] T. Choke, H. Zhang, S. Tan, W. Yang, Y. Tan, S. Karri, Y. Sun, D. Li, Z. Lee, T. Gao, W. Shu, and O. Shana'a, "A multiband mobile analog TV tuner SoC with 78-dB harmonic rejection and GSM blocker detection in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1174–1187, 2013.

[134] C. Andrews and A. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.

[135] A. Mirzaei, H. Darabi, J. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2353–2366, 2010.

[136] L. E. Franks and I. W. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path filters," *Bell Systems Technical Journal*, vol. 39, pp. 1321–1350, Sep. 1960.

[137] A. Ghaffari, E. Klumperink, and B. Nauta, "8-path tunable RF notch filters for blocker suppression," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2012, pp. 76–78.

[138] M. Darvishi, R. van der Zee, E. Klumperink, and B. Nauta, "Widely tunable 4th order switched Gm-C band-pass filter based on N-path filters," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3105–3119, Dec. 2012.

[139] H. Darabi, "A blocker filtering technique for SAW-less wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2766–2773, Dec. 2007.

[140] A. Safarian, A. Shameli, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "Integrated blocker filtering RF front ends," in *IEEE Radio Frequency Integrated Circuits Symposium*, 2007, pp. 13–16.

[141] T. Werth, C. Schmits, and S. Heinen, "Active feedback interference cancellation in RF receiver front-ends," in *IEEE Radio Frequency Integrated Circuits Symposium*, June 2009, pp. 379 –382.

[142] S. Youssef, R. van der Zee, and B. Nauta, "Active feedback receiver with integrated tunable RF channel selectivity, distortion cancelling, 48dB stopband rejection and >+12dBm wideband IIP3, occupying $<0.06\text{mm}^2$ in 65nm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2012, pp. 166 –167.

[143] A. Ghaffari, E. Klumperink, and B. Nauta, "A differential 4-path highly linear widely tunable on-chip band-pass filter," in *IEEE Radio Frequency Integrated Circuits Symposium*, Anaheim, CA, USA, May 2010, pp. 299 –302.

[144] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.

[145] K. Koli, S. Kallioinen, J. Jussila, P. Sivonen, and A. Pärssinen, "A 900-MHz direct delta-sigma receiver in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2807 –2818, Dec. 2010.

[146] T. Ström and S. Signell, "Analysis of periodically switched linear circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 24, no. 10, pp. 531–541, Oct. 1977.

[147] M. Soer, E. Klumperink, P.-T. de Boer, F. van Vliet, and B. Nauta, "Unified frequency-domain analysis of switched-series-RC passive mixers and samplers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 10, pp. 2618–2631, Oct. 2010.

[148] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 5, pp. 879–892, May 2011.

[149] A. Ghaffari, E. Klumperink, M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

[150] A. Mirzaei, H. Darabi, J. Leete, X. Chen, K. Juan, and A. Yazdi, "Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2678–2688, 2009.

[151] M. Kaltiokallio, V. Saari, J. Ryynänen, S. Kallioinen, and A. Pärssinen, "Wideband 2 to 6 GHz RF front-end with blocker filtering," in *IEEE Proceedings of the European Solid-State Circuits Conference.*, Helsinki, Finland, Sept. 2011, pp. 539 –542.

[152] T. Werth, C. Schmits, R. Wunderlich, and S. Heinen, "An active feedback interference cancellation technique for blocker filtering in RF receiver front-ends," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 989–997, 2010.

[153] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Pärssinen, "A multimode transmitter in 0.13 um CMOS using direct-digital RF modulator," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2774–2784, Dec. 2007.

[154] T. Rapinoja, K. Stadius, L. Xu, S. Lindfors, R. Kaunisto, A. Pärssinen, and J. Ryynänen, "A digital frequency synthesizer for cognitive radio spectrum sensing applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1339–1348, May 2010.

[155] J. Villanen, J. Ollikainen, O. Kivekäs, O, and P. Vainikainen, "Coupling element based mobile terminal antenna structures," *IEEE Transactions on Antennas and Propagation*, vol. 54, no. 7, pp. 2142–2153, Jul. 2006.

[156] D. Manteuffel and M. Arnold, "Considerations for reconfigurable multi-standard antennas for mobile terminals," in *Proceedings of International Workshop Antenna Technology*, Chiba, Japan, Mar. 2008, pp. 231–234.

[157] R. Valkonen, M. Kaltiokallio, and C. Icheln, "Capacitive coupling element antennas for multi-standard mobile handsets," *IEEE Transactions on Antennas and Propagation*, vol. 61, no. 5, pp. 2783–2791, May 2013.

[158] D. Zhou, R. Abd-Alhameed, C. See, A. G. Alhaddad, and P. Excell, "Compact wideband balanced antenna for mobile handsets," *IET Microwaves, Antennas and Propagation*, vol. 4, no. 5, pp. 600–608, 2010.

[159] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 1996, pp. 392–393.

[160] J. Cavers and M. Liao, "Adaptive compensation for imbalance and offset losses in direct conversion transceivers," *IEEE Transactions on Vehicular Technology*, vol. 42, no. 4, pp. 581–588, 1993.

[161] M. Suzuki, K. Hagimoto, H. Ichino, and S. Konaka, "A 9-GHz frequency divider using Si bipolar super self-aligned process technology," *IEEE Electron Device Letters*, vol. 6, no. 4, pp. 181–183, 1985.

[162] W. Fang, A. Brunnschweiler, and P. Ashburn, "An analytical maximum toggle frequency expression and its application to optimizing high-speed ECL frequency dividers," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 920–931, 1990.

[163] B. Razavi, K. Lee, and R. Yan, "Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 2, pp. 101–109, 1995.

[164] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, 2000.

[165] H. Wang, "A 1.8 V 3 mW 16.8 GHz frequency divider in 0.25μm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, Feb. 2000, pp. 196–197.

[166] H. D. Wohlmuth, D. Kehrer, and W. Simburger, "A high sensitivity static 2:1 frequency divider up to 19 GHz in 120 nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium*, Seattle, WA, USA, July 2002, pp. 231–234.

[167] P. Heydari and R. Mohanavelu, "Design of ultrahigh-speed low-voltage CMOS CML buffers and latches," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 12, no. 10, pp. 1081–1093, 2004.

[168] J. Kaukovuori, K. Stadius, J. Ryynänen, and K. A. I. Halonen, "Analysis and design of passive polyphase filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 3023–3037, 2008.

[169] M. J. Gingell, "Single sideband modulation using sequence asymmetric polyphase networks," *Electrical Communication*, vol. 48, no. 1 and 2, pp. 21–25, 1973.

[170] J. Archer, J. Granlund, and R. Mauzy, "A broad-band VHF mixer exhibiting high image rejection over a multidecade baseband frequency range," *IEEE Journal of Solid-State Circuits*, vol. 16, no. 4, pp. 385–392, 1981.

[171] S. Galal, H. Ragaie, and M. Tawfik, "RC sequence asymmetric polyphase networks for RF integrated transceivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 1, pp. 18–27, 2000.

[172] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, 2001.

[173] K. Wada and Y. Tadokoro, "RC polyphase filter with flat gain characteristic," in *International Symposium on Circuits and Systems*, Bangkok, Thailand, May 2003, pp. I–537–540.

[174] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, 1992.

[175] E. Klumperink and B. Nauta, "Systematic comparison of HF CMOS transconductors," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 10, pp. 728–741, 2003.

[176] F. Tillman and H. Sjöland, "A polyphase filter based on CMOS inverters," in *23rd NORCHIP Conference*, Oulu, Finland, Nov. 2005, pp. 12–15.

[177] M. Törmanen, A. Axholt, J. Lindstrand, and H. Sjöland, "A 2GHz Tx LO generation circuit with active PPF and 3/2 divider in 65nm CMOS," in *International Symposium on Integrated Circuits*, Singapore, Dec. 2011, pp. 208–211.

This work contributes to the mobile receiver research field by providing circuit solutions that enable the flexible and wideband receivers of the future. The multisystem multiband problem in mobile terminals requires new type of receiver solutions to minimize the cost and complexity.
One such solution developed in this thesis is the N-path filter, which utilizes the fast switching speed of modern CMOS technology. Other topics investigated in this thesis include wideband LNAs, mixer-first receivers, and LO-drive circuits. The circuits presented in this work represent novel circuit solutions and ideas, reaching state-of-the-art performance with respect to wideband and linear receivers.

Aalto-DD 36/2014

ISBN 978-952-60-5615-9
ISBN 978-952-60-5616-6 (pdf)
ISSN-L 1799-4934
ISSN 1799-4934
ISSN 1799-4942 (pdf)

Aalto University
School of Electrical Engineering
Department of Micro- and Nanosciences
www.aalto.fi

BUSINESS + ECONOMY

ART + DESIGN + ARCHITECTURE

SCIENCE + TECHNOLOGY

CROSSOVER

DOCTORAL DISSERTATIONS