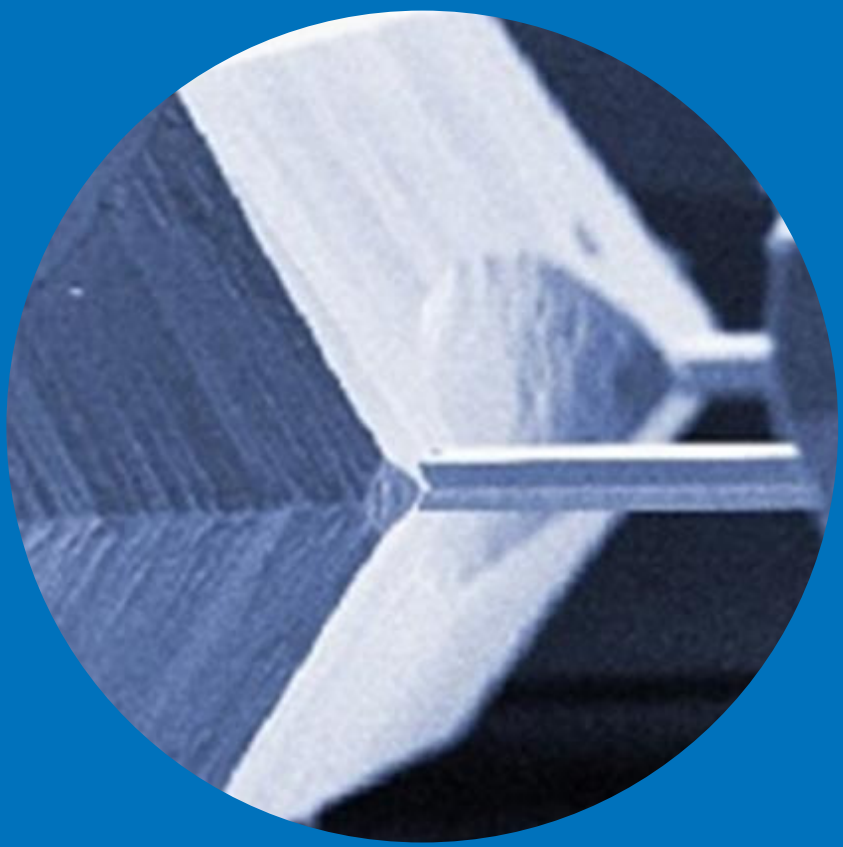
Department of Materials Science and Engineering

KOH anisotropic silicon etching for MEMS accelerometer fabrication

Petteri Kilpinen



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KOH anisotropic silicon etching for MEMS accelerometer fabrication

Petteri Kilpinen

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Abstract

This dissertation is intended as a guidebook for processing crystalline silicon by anisotropic potassium hydroxide (KOH) wet etching. In low cost bulk micromachining of silicon for MEMS (Micro Electro Mechanical Systems), anisotropic wet etching of single crystalline silicon in aqueous KOH solutions is a technically important process. Anisotropic etching of silicon is used to create mechanical microstructures in silicon. Differences in etch rates between the different crystal planes are utilized in the process.

The present dissertation explores six different aspects of silicon anisotropic etching using an accelerometer as a test device. The first part of the thesis concentrates on liquid phase phenomena, and the latter part with the interactions of the silicon crystal with the etching process. It is shown that etch rates and anisotropy are extremely sensitive to the process conditions and equipment, for example rotational flow in the etch bath is shown to be superior to laminar flow. It is also shown that the etch rate and the resulting surface quality are sensitive to very small changes in Pb concentrations in the range of 200 to 300 ppb.

The effects of wafer oxygen levels have been studied from etching point of view and were found to have a marked effect especially on etching the (111) crystal plane. A novel method for eliminating the effects of grinding damage on etching has been introduced. Ultra Poligrind wafers were used as substrate material for MEMS accelerometer structures. These wafers eliminate the need for double side polished wafers and are expected to reduce the cost of starting material considerably.

Taken together, the thesis provides an extensive set of guidelines for silicon anisotropic KOH etching. By careful optimization of both the etchant composition and equipment, and matching the design to wafer specifications, it is shown that a very high degree of control can be achieved by KOH wet etching. These guidelines will be useful for further MEMS and NEMS (Nano Electro Mechanical Systems) development in cases where critical structures are defined by KOH etching.

Keywords KOH, Silicon, Anisotropic Etching, MEMS, accelerometer

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Tiivistelmä

Tämä työ on tarkoitettu kaiken kattavaksi oppaaksi kiteisen piin anisotrooppiseen syövyttämiseen kaliumhydroksidilla eli KOH:lla. Piikiekkojen anisotrooppinen KOH-syövytys on edelleen teknisesti tärkeä prosessi, jolla valmistetaan halpoja mikroelektromekaanisia antureita ja systeemejä, joiden lyhenne on MEMS. Anisotrooppisella KOH-syövytyksellä valmistetaan MEMS-antureiden/-systeemien mekaaniset ja fysikaaliset rakenteet käyttämällä hyväksi piikiekon kidetasojen 100 ja 111 syöpymisnopeuseroja. Myös muiden kidetasojen syöpymisnopeuseroja voidaan hyödyntää.

Tässä työssä esitellään kuusi eri ilmiötä, jotka vaikuttavat piin anisotrooppiseen syöpymiseen KOH-vesiliuoksessa.Kahdessa ensimmäisessä osoitetaan, että syöpymisnopeudet ja anisotropiat ovat erityisen herkkiä syövytysprosessin olosuhteille sekä laitekonfiguraatiolle. Esimerkiksi KOH-vesiliuoksen virtauksessa pyörteinen virtaus on parempi kuin laminaarinen virtaus. Kolmannessa ilmiössä osoitetaan, että piin syöpymisnopeus on erittäin herkkä hyvin pienille lyijypitoisuuksien vaihteluille KOH-vesiliuoksessa. Lyjypitoisuuden muutos 200 ppb:sta 300 ppb:aan pienentää kidetasojen 100 ja 110 syöpymisnopeutta yli 7%. Neljännessä ilmiössä tutkitaan anisotropian ja syövytystuloksen vaihtelua piikiekon sisältämän hapen funktiona. Tulokset osoittavat, että kidetason 111 syöpymisnopeus on erityisen herkkä piikiekon happitasolle, ja siksi myös syövytystulos ja anisotropia ovat erityisen herkkiä. Kahdessa viimeisessä ilmiössä tutkitaan hienohiottuja piikiekkoja. Näistä ensimmäisessä esitellään uusi menetelmä hiontavaurioiden poistamiseksi ja osoitetaan, että hienohiotun ja vauriopoistosyövytetyn piikiekon KOH-syövytystulos on vastaava tai parempi kuin kiillotetun piikiekon syövytystulos. Jälkimmäisessä esitellään molemmin puolin Ultra Poligrind- hiotuista piikiekoista prossesoidut MEMS-kiihtyvyysanturin seismiset massat ja jouset. Tulokset osoittavat, että kiillotettujen kiekkojen asemesta Ultra Poligrind- hiottuja kiekkoja voidaan käyttää lähtömateriaalina vaativille MEMS-rakenteille ja että nämä kiekot voidaan anodisesti bondata eli liittää ilmatiiviiksi.

Kaikki tässä työssä esitellyt ilmiöt ja tutkimustulokset yhdessä antavat suuntaviivat mahdollisimman tasalaatuiselle piin anisotrooppiselle KOH-syövytysprosessille. Vain ottamalla huomioon kaikki syövytystulokseen vaikuttavat tekijät on mahdollista minimoida syövyttämällä tehtyjen MEMS-rakenteiden vaihtelu ja prosessoida nanoelektromekaanisia antureita/systeemejä (NEMS).

Avainsanat KOH, Pii, Anisotrooppinen märkäsyövytys, MEMS, Kiihtyvyysanturi

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Preface

The experimental research work of this thesis was carried out in Laboratory of Physical Metallurgy and Materials Science, Helsinki University of Technology, during the years 1998 - 2000 and in VTI Technologies Oy (present Murata Electronics Oy), during the years 2003 - 2013.

Warmest thanks to my supervisor professor Sami Franssila for his encouragement, comments and interest in my work. I am also very pleased and indebted to Ph.D. Ari Hirvonen who challenged and encouraged me in early stage to start this thesis in 2008 after my divorce. Ph.D. Risto Mutikainen, I would like to thank for the initial data from different projects and helpful comments and ideas which were invaluable.

For all the support and the opportunity to do this thesis, I would like to thank Murata Electronics Oy (former VTI Technologies Oy) and my manager M.Sc. Anni-Helena Hakola. I would also like to thank Aalto University Department of Materials Science and Engineering for the opportunity to do this thesis. For additional funding I would like to thank Henry Ford foundation.

I am also truly thankful to all my colleagues and friends in Murata Electronics Oy (former VTI Technologies Oy) for the pleasant working atmosphere. Especially, I am truly thankful to Ms. Suvi Keinänen, Mrs Tuire Lahti, M.Sc. Sanna Mäkelä, Mrs Elise Lindgren and M.Sc. Jami Nieminen for their assistance and support in performing the experiments and measurements. Furthermore, I am truly thankful to Ph.D. Xuwen Liu of Aalto University Department of Materials Science and Engineering for performing the Nanoindentation measurements.

My mother and my father as well as my sister and her family deserve lots of thanks for their trust and support. Lots of thanks also to all my friends and relatives for their support. And, special thanks go to my best friends: Jani, Jukka and Ilkka for all the support and joy they have given me during the past 25 years.

Finally, my truly loving thanks to my wife, Kia, for being with me and for supporting, trusting and loving me during the past five years. I also thank my ex-wife, Tiina, and my mother-in-law, Marja-Liisa, for their support. And, last but not least, I thank my dear daughter, Roosa, and my dear son, Carl, as well as my wife's son, Jan, for enriching my life and for just being there.

Espoo, April 27, 2014

Petteri Kilpinen

List of acronyms and symbols

a-Si	Amorphous silicon
ABS	Anti-lock breaking system
AFM	Atomic force microscopy
ASIC	Application-specific integrated circuit
ASTM	American Society for Testing and Materials
BHF	Buffered hydrofluoric acid
BioMEMS	Biological micro electro mechanical systems
Bow	The concave or convex deformation of a wafer
c-Si	Crystalline silicon
CMOS	Complementary metal oxide silicon field effect transistor technology
CMP	Chemical mechanical planarization
CZ	Czochralski crystal growth method
DI water	De-ionized water
DRIE	Deep reactive-ion etching
DSG	Double side grinded (wafer)
DSP	Double side polished (wafer)
EDP	Ethylene diamine pyrocathecol
ESC	Electronic stability control system
EPI	Epitaxial growth (wafer)
F3dB	The frequency where the gain is 3 dB lower than the gain at a specified reference frequency
FG	Fine grinding
FZ	Float-zone crystal growth method
FPD	Focal plane deviation
IC	Integrated circuits
IPC-AES	Coupled plasma atomic emission spectrometry
IPA	Isopropyl alcohol
LOCOS	Local oxidation of silicon; older isolation/separation technology
LPCVD	Low pressure chemical vapor deposition
MCZ	Magnetic Czochralski crystal growth method
MEMS	Micro electro mechanical systems
NEMS	Nano electro mechanical systems

NHE	Normal hydrogen electrode
PECVD	Plasma enhanced chemical vapor deposition
PTFE	Polytetrafluoroethylene
PGA	Photoacid generator
PMMA	Poly(methyl methacrylate)
Ra	Profile roughness parameter; arithmetic average
RF	Radio frequency
RG	Rough grinding
RMS	Root mean square (averaging factor)
Rq	Profile roughness parameter; root mean square
Sa	Area roughness parameter; arithmetic average
SC	Standard clean
SEM	Scanning electron microscope
SEM EDS	Scanning Electron Microscopy with X-ray microanalysis
SIMS	Secondary ion mass spectrometry
SOI	Silicon on insulator
SPM	Scanning probe microscopy
Sq	Area roughness parameter; root mean square
TEM	Transmission electron microscopy
TIR	Total indicating reading
TTV	Total thickness variation
TMAH	Tetra methyl ammonium hydroxide
Warp	The difference between the maximum and minimum distances of the median surface of the wafer from a reference plane encountered during the scanning pattern
WOX	Wet oxidation

Author's contribution

The author has had an active role in all phases of the research reported in this Thesis. He has been involved in planning and performing the tests, and in the interpretation of the results. He has had a major role in the conceptualization of low cost non-polished MEMS wafers and optimizing oxygen concentration in silicon wafers for MEMS. The conceptualization of Ultra Poligrind wafer as MEMS starting material is still in progress. The author has written the Thesis.

Additionally, the results of the etch rate variations of p+ silicon wafers have been presented by the author at the 1999 MRS fall meeting in Boston, USA, in 1999. The results of MEMS beam length control by optimizing silicon oxygen concentration for wet etching and low cost non-polished MEMS wafers have been presented by the author at the MME 2013 24th Micromechanics and Microsystems Europe Conference, Espoo, Finland, in 2013. Part of the writing and contribution to the experiments and experiment design as well as a good portion of the result analysis were contributed to [Gosálvez 2001]. Below a list of author presentations and author contributed publications:

- Kilpinen, P., Haimi, E., Lindroos, V.K., The Etch Rate Variations of p+ Silicon Wafers in Aqueous KOH Solutions as a Function of Processing Conditions, MRS Proceedings. 1999. 605: p. 293-298.
- Kilpinen, P., Mutikainen, R., Hirvonen, A., Franssila, S., Grinding damage removal results in low cost non-polished MEMS wafer. MME 2013 24th Micromechanics and Microsystems Europe Conference, Espoo, Finland, September 1-4, 2013. P8.
- Kilpinen, P., Hirvonen, A., Franssila, S., MEMS beam length control by optimizing silicon oxygen concentration for wet etching. MME 2013 24th Micromechanics and Microsystems Europe Conference, Espoo, Finland, September 1-4, 2013. P21.
- Gosálvez, M.A., Nieminen, R.M., Kilpinen, P., Haimi E., Lindroos, V., Anisotropic wet chemical etching of crystalline silicon: atomistic Monte-Carlo simulations and experiments. Applied Surface Science. 2001. 178: p. 7-26.

Contents

1. Introduction

1.1 What are microsystems?

Microsystems technology refers to products that have structures whose dimensions are measured in the micrometre (10^{-6} m) range and technical functions provided by the shape of the micro structure. They combine several micro-scale features, optimized as an entire system, to provide one or several specific functions, in some cases including microelectronics. Microsystems are synonymous with micro electro mechanical systems (MEMS). Typical microsystems have mechanical parts, like micro bridges in RF switches or bending cantilevers in atomic force microscopes (AFMs); electrical parts like piezoresistors in airbag sensors or capacitors in pressure sensors or accelerometer sensors; thermal and fluidic structures like heaters and nozzles in inkjet printers or in flow sensors. In biomicrosystems (BioMEMS), cells or microbeads are handled by fluidic streams, magnetic and electric fields, thermal gradients, etc. In chemical microsystems, operations like sample pre-treatment, separation and detection are built on microchips. Microsystems can be classified by their fabrication technologies. Devices are made with bulk micromachining technologies, surface micromachining, and silicon on insulator (SOI), and metal or polymer technologies. In bulk micromachining, the structures are etched through the wafer. The same is often true of SOI MEMS. In surface and metal microsystems, the devices are made in thin film layers deposited on (silicon) wafers.

A prototypical structure in bulk microsystems is a double-side etched (100) wafer. One example is the silicon spring beam and seismic mass of an accelerometer, Fig 1.

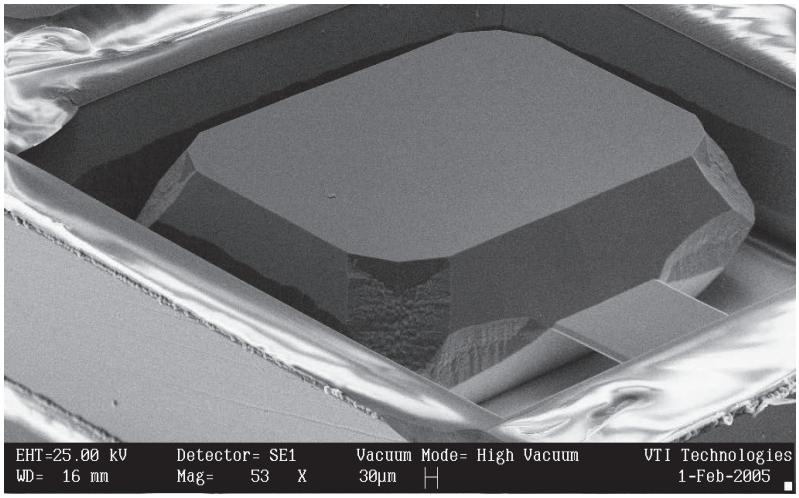


Fig 1. SEM figure of anisotropic KOH wet etched single crystalline silicon seismic mass and spring beam (cantilever) of bulk MEMS accelometer sensor.

1.2 How are microsystems made?

Microsystems are made by applying microfabrication technologies to silicon wafers. Integrated circuit (IC) technology uses only the electrical properties of silicon but microfabrication also uses the physical properties of silicon, such as ideal elasticity and chemical stability. Furthermore, silicon wafers are by default compatible with microfabrication equipment because most of the machinery for microfabrication was originally developed for silicon ICs [Franssila 2004].

Microfabrication processes consist of four basic operations:

1. Patterning (e.g. lithography...)
2. Additive (e.g. deposition, oxidation, epi...)
3. Subtractive (e.g. etching, polishing...)
4. Modification (e.g. doping, annealing...)

Surface preparation and wafer cleaning can be classed as the fifth basic operation. However, surface preparation and wafer cleaning are never done alone nor are permanent structures made in these processes. These steps are always closely

connected with both the preceding and the following process steps. Within each basic operation, there are many specific technologies suitable for certain substrates, certain line widths or certain cost levels [Franssila 2010].

1.3 Silicon

Bulk silicon wafers are made of single-crystal pieces cut and polished from larger single-crystal ingots. Silicon is extremely strong, on a par with steel, and it also retains its elasticity at much higher temperatures than metals. However, single-crystalline silicon wafers are fragile: once a fracture starts, it immediately develops across the wafer because covalent bonds do not allow dislocation movements [Franssila 2010]. The resistivity of silicon wafers ranges from 0.001 to 20 000 ohm-cm and the most used dopants are boron for p-type silicon and phosphorus, antimony and arsenic for n-type silicon. Silicon wafers are nowadays available with diameters of 100, 125, 150, 200, 300 and even 450 mm. In addition to size, resistivity and dopant type, wafer specifications include thickness and variation of thickness, crystal orientation, particle counts and many other parameters.

The crystal structure of silicon is similar to that of diamond. In other words, it has a double surface central cubical crystal structure, as shown in Fig 2. Every atom is connected in the form of a tetrahedron to four other atoms, forming a three-dimensional network lattice. The lattice constant (a) of silicon is about 5.43 Å.

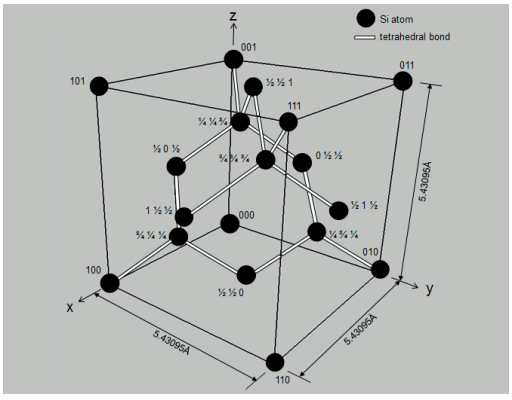


Fig 2. The unit cubical structure of the diamond lattice of silicon.

Fig 3 shows the crystallographic planes of the silicon crystal. Plane (100) is parallel with the normal of the cubic surface and it has a four-fold symmetry. Plane (110) is parallel with the normal of the diagonal of the cubic surface and it has a double symmetry. Plane (111) is parallel with the normal of the cubic volume diagonal and it has a three-fold symmetry.

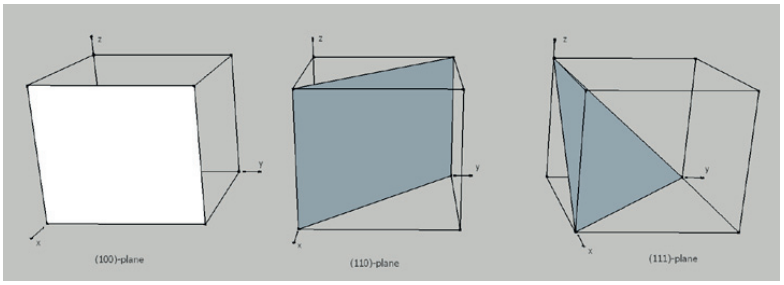


Fig 3. The most important crystallographic planes of the silicon.

1.4 Anisotropic wet etching of silicon

Anisotropic wet etching is used to create the mechanical parts, optical parts, fluidic structures or thermal structures of microsystems. With anisotropic etching it is only possible to make such structures as the shapes of (111) planes restrict. This radically reduces the degree of freedom of planning the structures. The simplest structures that can be etched to the (100) wafer are presented in Fig 4.

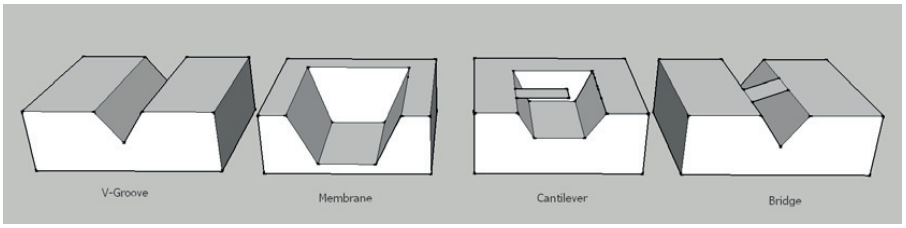


Fig 4. Structures accomplished by anisotropic etching to silicon wafer.

Anisotropically wet etched mechanical parts are used, for example, in; bending cantilevers [Elwenspoek 1989, Brugger 1997, Jovic 2007], membranes [Venstra 2003, Soin 2006], resonators [Vlaminck 2006], arrays [Hines 2003], sharp silicon tips

[Sarajlic 2007, Han 2009], nanowires [Namatsu 1997, Sheu 2001, Lee K-N. 2007, Bischoff 2009, Pennelli 2009], nanopillars/nanostructures [Manimaran 2001, Choi 2008], nanoribbons [Tolmachev 2005, Cho Ko 2006].

Optical parts are, for example, micro mirrors [Strandman 1995, Yun 2006, Jia 2008, and Xu 2009] or vertical taper structures [Holly 2006]. Fluidic structures are, for example, nozzles in inkjet printers [US5131978 1992, US5277755 1994, Nayve 2003] or porous silicon in fuel cells [Kelly 2005]. Thermal structures are, for example, heaters [Fonseca 2008] and fuel cells [Pichonat 2006, Hasran 2011].

DNA purification microchip [Chen X. 2007], microneedle arrays for drug delivery [Tan P.Y.J. 2002], CMOS infrared sensor arrays [Münch 1997] and single-electron transistors [Pennelli 2006] are all examples of microsystems in which fabrication anisotropic wet etching is used.

There are many etchants that behave anisoptopically in silicon etching. They are all caustic solutions but their main components can be organic or inorganic. The most common solutions are KOH (potassium hydroxide) and TMAH (tetra methyl ammonium hydroxide). Other anisotropic etchants are EDP (ethylene diamine pyrocathecol), (N_2H_2), NaOH, LiOH, and NH_4OH. The first studies with anisotropic etchants were made in 1962 with EDP solution [Lang 1996]. EDP is ideal for silicon anisotropic etching but it is very toxic and, therefore, its use is now prohibited. KOH remains the most popular anisotropic etching solution. However, TMAH is becoming more and more popular because it is nontoxic and it is compatible with CMOS technology. K^+ ions pose a contamination hazard in CMOS devices.

When a V-groove (Fig 4) is totally congruent with the direction <110>, under-etching will not take place. The walls of the etched V-groove are restricted by the (111) planes. The angle between the surface of the wafer and the walls is 54.74°. Fig 5 and Fig 6a show a V-groove which has been directed according to the (111) planes in the <110> direction.

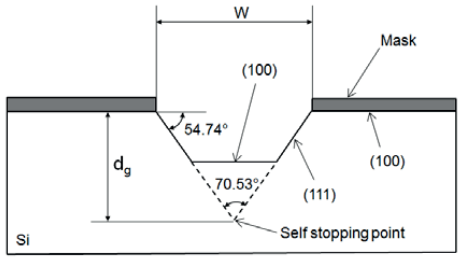


Fig 5. Anisotropically etched V-groove to (100) wafer, cross section.

At the bottom of a V-groove, when totally etched, is the self-stopping point at the intersection of the (111) planes in depth d_g. If the opening of the V-groove is W, the depth of self-stopping point is:

$$d_g = (W/2) * \tan 54.74° \quad (1)$$

If the right-angled opening in the mask oxide is not carefully set in the <110> direction, it will etch under the mask oxide (Fig 6b). This under-etching will continue until a (111) plane is reached and the figure has turned in the direction <110>. This means that the openings etched will be wider than the dimensions intended if the openings have been inaccurately orientated in the direction <110> or if the direction of the identification level of the wafer is not accurate. Under-etching takes place also in round structures (Fig 6c). When there is a convex corner of the (111) plane in the structure, as shown in Fig 6d, it will always etch to be the concave corner of the (111) plane.

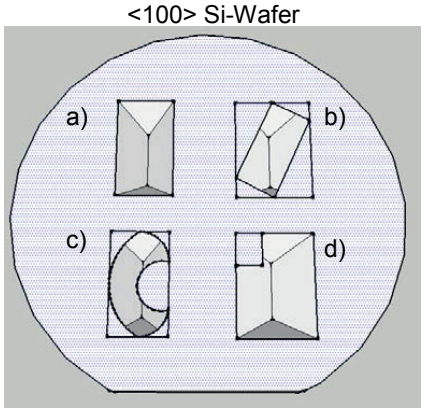


Fig 6. Figures anisotropically etched on the surface of the (100) wafer. Dotted area: figures made on the mask. Black line: figures accomplished with etching.

Finally, the etched structures can only contain convex corners if they have been protected with special protection figures (convex corner compensation figures) beforehand. The etching of the convex corner finds an explanation in the physical mechanism of the anisotropy. At the convex corner, the three bonds of the (111) plane are forced to be under the effect of the etchant. The atom at the corner is surrounded by etchant at a 270° angle, while the lattice atom sees etchant only at a 90° angle. Etching that has started from the convex corner continues until the concave corner is reached.

1.5 Motivation for the thesis

Over its fifty-year history, the semiconductor industry has sought to make devices ever smaller and at ever cheaper prices. The MEMS industry follows the same trends. This means that the manufacturing process must develop and the quality of the products must remain high. One obstacle on this road is anisotropy wet etching, which is still a very common method for the fabrication of the structures of MEMS devices on single-crystal silicon. Anisotropy wet etching is a much cheaper process than the newer dry etching method. In some applications also a larger size is

beneficial, for example, the bigger size of seismic mass of an accelerometer is needed to guarantee the highest possible accuracy of measurement.

Anisotropically etched silicon spring beams and seismic masses of accelerometers have been studied for decades [Li 1996, Schröpfer 1997, Puers 1998, Takao 2000, Sankar 2011]. Other methods to etch accelerometer mechanical structures onto silicon are DRIE etching [Xie 2011, Fujiyoshi 2011] and a combination of DRIE and anisotropic wet etching [Chae 2005, Xiao 2008, Zhou X 2010, Wang 2011]. A completely alternative method to produce accelerometer mechanical structures is, for example, with surface micromachining [Haris Md Khir 2007, Lee I 2005, Liu Y-C 2011, Aoyagi 2011]. Accelerometers are used in many consumer and automotive applications, for instance in video games, digital cameras, airbag launchers and anti-lock breaking (ABS) systems in motor vehicles, and electronic stability control (ESC) systems [Fleming 2001].

In order to achieve the highest possible accuracy of accelerometer measurement, it is necessary to etch the device structures with the highest possible precision. For example, the variation in accelerometer beam dimension and seismic mass size must be as low as possible. This demand is achieved only when etch rates are stable and etched surfaces are smooth. This dissertation explains the interactions between design rules, silicon wafer properties, process conditions and device performance. Central to the work is the study of batch etching of silicon wafers in KOH. This work gives guidelines for a highly uniform (across wafer, across batch and batch-to-batch) KOH etching process that is able to achieve the most identical MEMS structures in high volume manufacturing and even to approach the scale of NEMS structures (Nano Electro Mechanical Systems). In order to succeed in that kind of process development or enhancement, it is crucial to be familiar with all aspects of the process; materials, equipment and costs.

The present dissertation introduces six different phenomena that influence the anisotropic etching of silicon in aqueous KOH solution. They are:

1) Etching temperature and KOH concentration - chapter 6.1
2) Etching equipment and agitation - chapter 6.2
3) Impurities in etching solution - chapter 6.3

4) Impurities in Si wafer - chapter 7.1
5) Surface finish of Si wafer and removal of defects (KOH dip) - chapter 7.2
6) Surface finish of Si wafer and removal of defects (Ultra Poligrind) - chapter 7.3

The first two phenomena shows that etch rates and anisotropy are extremely sensitive to process conditions, process equipment and aqueous KOH flow (rotational flow is better than laminar flow). The third phenomenon shows that the etching rate and etching result are very sensitive to very small changes in Pb concentration (200 ppb to 300 ppb). The variation in anisotropy and etching results was studied as a function of oxygen level in crystalline silicon wafer in the fourth phenomenon. A novel method for removal of grinding damage was presented and variation in etching results studied as a function of crystalline silicon surface finish in the fifth phenomenon. In the final study, in the sixth phenomenon, double sided Ultra Poligrind ground wafers were processed to MEMS accelerometer seismic masses and spring beams.

2. Mechanism of anisotropic etching

The process of anisotropic etching of single crystalline silicon in aqueous KOH solutions utilizes the differences in etch rates between the (100) plane and other silicon crystal planes [Lang 1996]. KOH etching is based on the reaction presented in equation 2. In the etching reaction, the main reagents are OH^- ions and H_2O molecules. Palik *et al.* [Palik 1983] perceived this in 1983, when they followed the etching of silicon in KOH in situ with Raman-spectroscopy [Palik 1983]. In these tests, they noticed that the head reaction was restricted by OH^- ions and that $SiO_2(OH)_2^{--}$ is the primary reaction product which is followed by polymerization.

$$\mathbf{Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{--} + 2H_2} \qquad (2)$$

In the second test, [Palik 1983] added isopropyl alcohol to the KOH solution, the result was that alcohol did not take part chemically in the reaction. In later tests, Palik *et al.* [Palik 1985] suggested that the etching reaction transports electrons from the OH^- ion to the energy band of the silicon and from there back to the reaction product.

2.1 Chemical model

In 1990, more specific findings of reactions were published [Seidel 1990 1]. According to Seidel *et al*., the etching of the silicon begins when OH^- ions achieve connection with silicon atoms. In that case, the Fermi levels in both the electrolyte and the silicon will settle on the same level and the electrons flow from the electrolyte to the silicon. Consequently, the valence band and conductivity band curve downwards in both n- and p-type silicon (Fig 7). The stronger the curve of the bands, the bigger is the difference between the Fermi level in the electrolyte and the Fermi level in the silicon. Correspondingly, the more strongly the silicon is doped, the greater is the deviation of the Fermi level in the silicon. This phenomenon has been the subject of further studies [Chen L. 1995, Liu W. 2006].

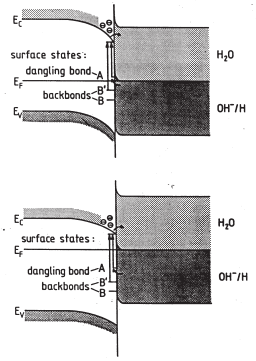


Fig 7. Energy band structure of silicon and KOH electrolyte in contact with each other. Upper: Si that has been doped p-type. Lower: Si that has been doped n-type [Seidel 1990 1].

The structure of the energy band of the silicon is shown in Fig 7 with the space between a valence band and a conductivity band being 1.12 eV. The position of the Fermi level depends on the doping level of the silicon. In n-type silicon, the Fermi level is above the middle of the valence band and the conductivity band. In p-type silicon, the Fermi level is below the middle of the valence band and the conductivity band. The silicon electron affinity is 4.05 eV, which corresponds to the distance from the vacuum to the lowest section of the conductivity band. Fig 8 shows the structure of the silicon and KOH electrolyte energy band. The distance from the vacuum to the Fermi level is 3.7 eV when the pH of KOH is 14.

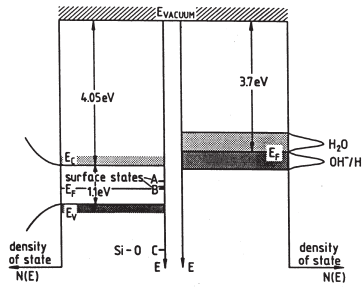


Fig 8. Silicon and KOH electrolyte energy band structure and electron affinity before contact [Seidel 1990 1].

Due to the crystalline structure of silicon, the crystal planes of the silicon differ depending on their surface structure. This means that OH^- ions which contact at the surface react at a separate rate with different crystal planes (Fig 9).

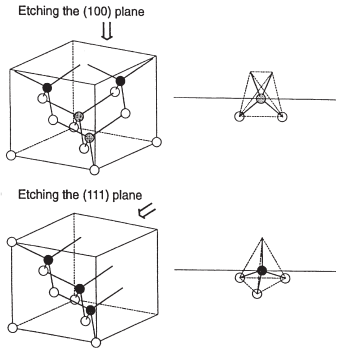
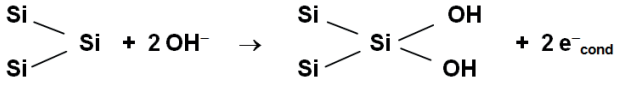


Fig 9. Difference of surface structure between plane (100) and plane (111) is shown. Etchant is in contact only with the atoms shown in black [Lang 1996].

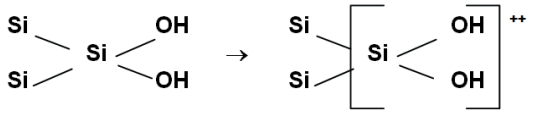
In the case of plane (100) (see Fig 9 upper), when silicon atoms are in contact with OH^- ions, the four bonds of the reacting atom have been divided so that there will be two bound bonds and two free bonds. The free bonds were created by the two atoms etched away at the previous etching stage. Etchant cut these two bound bonds and reacting atom etched away.

Etching takes place step by step. The first two OH^- ions connect to the two free bonds and two electrons are released:



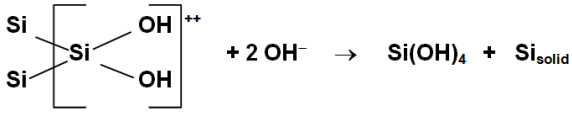
(3)

The electrons released in the reaction are carried by gap tunnelling to the conductivity band of the silicon, as shown in Fig 7 above. At the second stage, $Si(OH)_2$ ionizes. This will take place when the electrons of the two bound bonds of the silicon receive sufficient thermal energy for them to be transferred to the conductivity band:



(4)

At the third stage, positively charged $Si(OH)_2^{++}$ reacts with two new OH^- ions:



(5)

The $Si(OH)_4$ that has materialized in the reaction is soluble in the KOH solution and is able to loosen from the surface of the silicon crystal. In more than 12 pH solutions, $Si(OH)_4$ is not stable and reacts according to the reaction equations (6) and (7):

$$Si(OH)_4 \rightarrow SiO_2(OH)_2^{--} + 2\ H^+ \quad (6)$$

$$2\ H^+ + 2\ OH^- \rightarrow 2\ H2O \quad (7)$$

The gap-tunnelled electrons (equations (3) and (4)) remain in the conductivity band of silicon. If silicon is low-doped, in other words, if it behaves as a semiconductor, it has few recombination centres and the electrons will stay for some time in the conductivity band. When the electrons come free from the lattice, they will react with the water molecules of the KOH solution. First the water molecules ionize, then they break into OH^- ions and hydrogen molecules, which are released from the surface of the silicon crystal, and rise as bubbles to the surface of the KOH solution.

$$4\ H2O + 4\ e^- \rightarrow 4\ H2O^- \quad (8)$$

$$4\ H2O^- \rightarrow 4\ OH^- + 2\ H^+ \quad (9)$$

Based on reactions (8) and (9), silicon remains electrically neutral and the new OH^- ions formed in the reaction keep the etching process going. When reactions (3), (4) and (9) are examined, one can notice that the dissolving of the silicon is in fact an

electrochemical process which does not move net current. The etching of the silicon can thus be changed if the electric properties of the surface of the silicon are changed. The stopping techniques of the etching are based on this phenomenon. In the p+ etch stopping technique, the silicon has been highly boron doped and the electrons which have been carried in the valence band recombine with holes and are not able to continue reactions (8) and (9). In the electrochemical stopping technique, the electrons which have formed in reaction (4) are conducted off the surface of the silicon and the etching, by reactions (3) and (8), is prevented by an external electric field.

The OH^- ions formed in reactions (8) and (9) are the ones that react with silicon. This was supposed by Seidel *et al.* [Seidel 1990 1]. Four H_2O molecules are needed for the etching of one Si atom. This assumption accords well with the practice because the maximum etching rate is at a KOH concentration of 20 wt-% (Fig 10). Chapter 6.1 presents a study of silicon etch rate as a function of the KOH concentration for highly boron doped silicon.

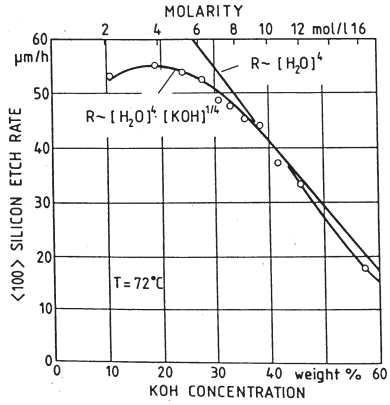


Fig 10. Etch rate of silicon (100) as function of the concentration of KOH etchant at 72 °C [Seidel 1990 1].

The total reaction from these part reactions is:

$$\mathbf{Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{--} + 2H_2} \qquad (10)$$

The difference in the surface structure of the different crystal planes explains the etching anisotropy. As shown in Fig 11, the numbers of the free bonds of silicon depend on the orientation. The fewest free bonds are in the (110) and (111) planes (Figs 11b and 11c), both having only one free bond per one Si atom. Most free bonds are at the (100) plane (Fig 11a) where two free bonds exist.

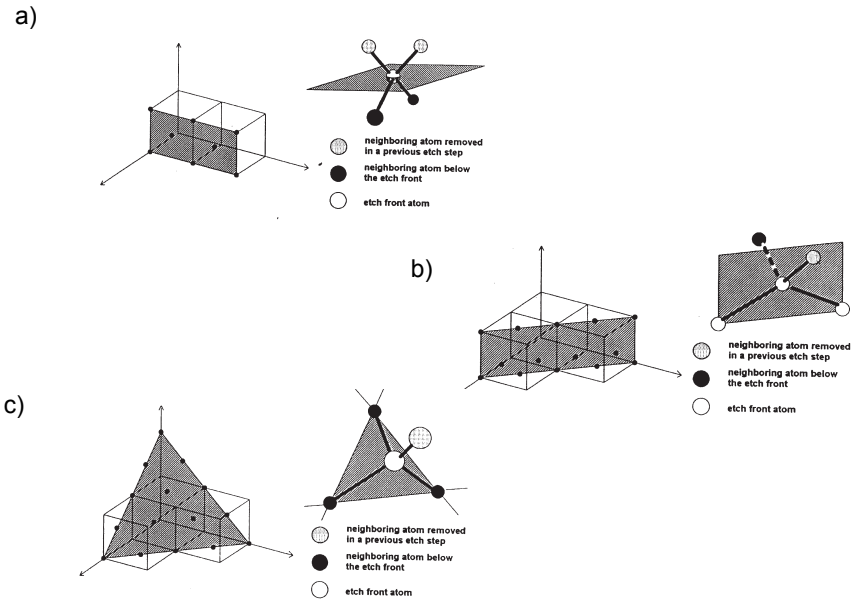


Fig 11. Positions of surface atoms, bound bonds and free bonds, in relation to the etch front. a. (100) b. (110) and c. (111) planes [Than 1994].

The absence of one free bond from the atoms of planes (111) and (110) slows down the etching reaction in these directions because only one OH^- the ion can be connected to one Si atom:

$$\begin{matrix}\mathrm{Si}\\ \mathrm{Si}\\ \mathrm{Si}\end{matrix}\!\!\diagdown\!\!\diagup\!\!\mathrm{Si} + \mathrm{OH}^- \rightarrow \begin{matrix}\mathrm{Si}\\ \mathrm{Si}\\ \mathrm{Si}\end{matrix}\!\!\diagdown\!\!\diagup\!\!\mathrm{Si}\,\mathrm{OH} + \mathrm{e}^-_{\mathrm{cond}} \qquad (11)$$

In the reaction, one electron is gap tunnelling to the conductivity band of silicon. The breaking of the bonds of the ones that have been bound is a precondition for the

continuing of the etching. At planes (111) and (110) there are three bound bonds on both. The breaking of these bonds requires more thermal energy than the breaking of the two bonds of the level (100). Furthermore, the amount of thermal energy needed to break the (100) plane bonds is reduced by OH^- ion fastening to free bonds. When an OH^- ion fastens on the free bonds of the silicon atom, it will reduce the binding energy of bound bonds. Two OH^- ions fastening on the two free bonds of the plane (100) change the form of the electron bond of the silicon atom by electrostatic interaction. The bound bonds weaken and break easily and thus the plane is etched fast. The effect of the one OH^- ion on three bound bonds is much smaller and the bound bonds do not weaken, thus the plane is etched slowly.

If the atoms of plane (111) get the bound electrons of moving to the conductivity band and the SiOH complex ionizes with enough energy, then:

$$\begin{matrix}\mathbf{Si}\\ \mathbf{Si}\\ \mathbf{Si}\end{matrix} \gt \mathbf{Si} \text{ — } \mathbf{OH} \rightarrow \begin{matrix}\mathbf{Si}\\ \mathbf{Si}\\ \mathbf{Si}\end{matrix} \quad [\mathbf{Si} \text{ — } \mathbf{OH}]^{+++} + 3\,\mathbf{e}^{-}_{\mathbf{cond}} \qquad (12)$$

The complex which has ionized reacts with three OH^- ions and forms Si(OH) which is soluble:

$$[\mathbf{Si} \text{ — } \mathbf{OH}]^{+++} + 3\,\mathbf{OH}^{-} \rightarrow \mathbf{Si(OH)_4} \qquad (13)$$

The $Si(OH)_4$ etching reaction will continue in the same way as described earlier in the (100) plane etching in equations (6 - 10).

In spite of having three bonds, the etching rate of the (110) plane is about the same as that of the (100) plane. By comparing Figs 11a and 11b, one can state that at the (110) plane the atoms of bound bonds come into contact with the etchant at the same time as the atoms to be etched and the binding energy of bound bonds becomes smaller. The plane is etched fast. At the (111) plane the atoms of bound bonds do not come into contact with the etchant (Fig 11c) and the bound bonds do not weaken.

From these conclusions the following rules are derived for the etching of silicon atoms:

1. An atom that is in contact with the etchant comes loose if it has:
    - Two bound bonds.
    - Three bound bonds, at least one of which is in contact with the etchant.
2. An atom that is in contact with the etchant does not come loose if it has three bound bonds, none of which is in contact with the etchant.
3. An atom which does not fulfil the 1st and 2nd rules comes loose.

2.2 Physical model

The theory of silicon wet etching, which is based on the understanding of the growth of single-crystal silicon, was presented by Elwenspoek [1998]. According to him, in the etching, the starting points may be either smooth or uneven crystal surfaces. The kinetics of smooth surfaces is controlled by the nucleation energy wall. There is no corresponding wall on the uneven surfaces. For this reason, the uneven surfaces etch at a rate one order higher than the even surfaces. Studies have shown that in the crystal structure of silicon the (111) plane is the only plane with a smooth surface. Other planes can be smooth only if their surface is rearranged. On rearranged surfaces, bonds are connected together and form a smooth plane where there are no free bonds.

In the kinetic model of crystal growth, the most important position is the active sections of the silicon lattice (called: kink site). In these sections, the atom has equal numbers of bound and open. Fig 12 describes the atoms in cubical figures. The atom (darkened) in an active section has three walls close to the lattice and there are three walls open to a fluid atmosphere or a gas atmosphere. In the etching, the etchant reacts with the atom in an active section where the case atom comes off the lattice and diffuses along the surface (Fig 12b). The atom that has come loose diffuses until it finds a new active position or is desorbed, in other words, the atom comes totally loose to the etchant from the surface of the crystal (Fig 12c). In the growth of a crystal, the process proceeds in the opposite direction. An atom in the melt is

absorbed into the surface of the crystal and it diffuses until it finds an active position or comes loose once more in the melt.

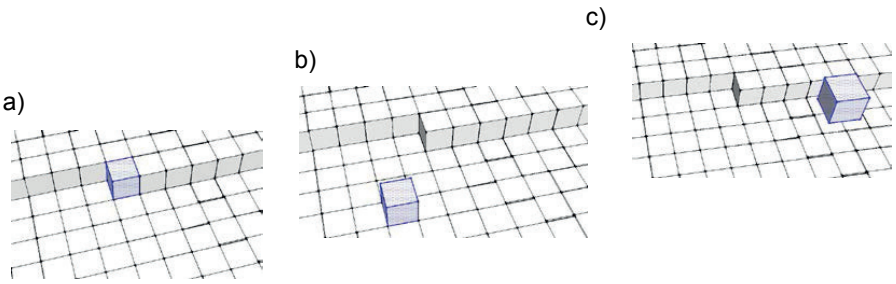


Fig 12. Behaviour of the atom in an active position in the etching (a $\rightarrow$ b $\rightarrow$c) and in the growth of the crystal (c $\rightarrow$ b $\rightarrow$ a) [redrawn from Elwenspoek 1998].

The kinetic value of the growth and etching of the crystal depends on the number of active positions. The number of active positions varies greatly between the crystallographic directions. There are no active positions in a smooth (111) plane because its atoms have three bound bonds and one free bond. In the (100) plane atoms have two bound bonds and two free bonds, in other words every (100) plane atom is in one active position. The difference between the separate crystals' directions will become clear in view of the different energy level required to loosen one atom or to bind it back (ΔE). To loosen one atom in the (111) plane, three strong bonds must be cut from the plane (3*ϕ). The energy of one bond is obtained from the back binding (ϕ) (Fig 13). In other words, the difference of these energies (ΔE) is 2 ϕ. At the (100) plane the situation is different because both the energy required to loosen the atom and the energy required for binding the atom back is equal, in other words 2ϕ, and the difference of energies (ΔE) is 0.

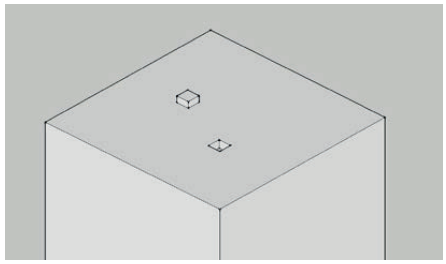


Fig 13. To loosen one atom in the (111) plane, three strong bonds must be cut from the plane (3*ϕ). The energy of one bond is obtained from the back binding (ϕ) [redrawn from Elwenspoek 1998].

When the difference of energies (ΔE) is divided by the absolute temperature (T) and the Boltsman constant (k), the factor of Jackson is obtained (α= ΔE / kT). When the temperatures are low enough $\Delta E = \kappa T\alpha$ is proportional to the step free energy (ΔE = γ). Step free energy (γ) is a reversible process, which is required for the creation of the plane 'step'. The essential difference between (111) and (100) planes is the fact that, in the balance, plane (111) is smooth at a relatively low temperature whereas plane (100) is uneven. Step free energy (γ) is finite on (111) plane and zero on (100) plane. When the number of the atom pairs that come loose or bind is proportional exp $-\alpha$, the probability of occurrence of this atom pair is extremely small at the (111) plane at a low temperature, but at the (100) plane the probability is 1 at all temperatures. The (110) plane is a so-called stepped face, which contains parallel chains of (110) plane which are not connected laterally. In that case, it will be possible to loosen the chain from the surface and to attach it to some other section of the surface without input of energy. In other words, the (110) plane is uneven.

The silicon crystal will etch or grow only when there is imbalance in the system, in other words, there must be a difference in the chemical potential between melt and solid silicon ($\Delta(\mu) \neq 0$). The etching and growth of the crystal depends on the value of $\Delta\mu$ and the amount of dependence is unequal between a smooth and an uneven plane. If atoms are to be loosened from a smooth plane, a step must be created. Suppose that N atoms have been loosening, in other words, a hole where N is a number of vacancies have been created. In that case, the free energy of the system

will increase with the value $N\Delta\mu$. If the hole is supposed to be circular, the area of the hole is relative to the number of vacancies N and it is relative to the square meter of the radius. Due to the step that has been created, the smooth plane's positive step free energy (γ) increases and it is proportional to the length of the step. Because the step free energy (γ) is proportional to the radius of the hole linearly, a critical value (r*) is obtained for the ray of the hole, as shown in Fig 14. The crossing of the nucleation wall formed by the free energy is a precondition for the growth of the hole. If the hole in a smooth plane is smaller than a critical value (r*), it is highly probable that it will disappear, but a hole that is bigger than the critical value is able to continue growing.

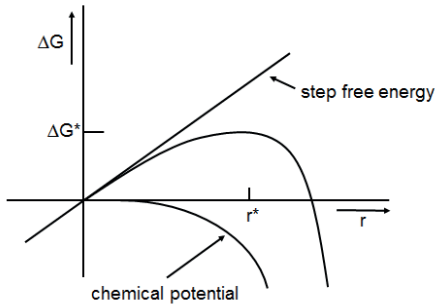


Fig 14. Free energy of the smooth surface as a function of the radius of the hole on the surface [redrawn from Elwenspoek 1998].

To begin etching, a two-dimensional nucleation wall must be gained. The etching rate contains the factor exp ($-\Delta G^*/kT$) where ΔG^* is the free energy of the critical nucleus:

$$\Delta G^* = \xi\gamma / \Delta\mu \qquad (14)$$

In the formula, γ is the step free energy and ξ is the geometric factor of the unevenness which depends on the crystallographic plane on which the atom is situated. When $\Delta G^*/kT$ is large, the etching rate will be extremely low. This will be the situation when the solution is weak or when there is a big step free energy in the plane ((111) plane).

The second mechanism that produces steps, in other words the active sections, is a screw dislocation (Fig 15a). The screw dislocation moves in the lattice by 'climbing'

and produces a step on the surface of the crystal. The step moves as the crystal is either grown (Fig 15b) or etched (Fig 15c). The growth rate and etching rate of the crystal defect are proportional $\Delta\mu^2$ and an uneven crystallographic plane is proportional $\Delta\mu$.

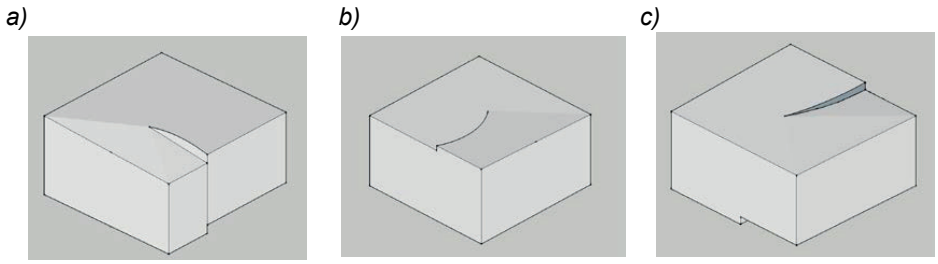


Fig 15. a. Step caused by screw dislocation. b. The step moves when a crystal is grown and c. The step moves when a crystal is etched [redrawn from Elwenspoek 1998].

Elwenspoek's theory leads to the following conclusions:

1. An uneven crystallographic plane etches much faster than a smooth plane. In the diamond lattice, the only smooth plane is (111) although it is possible that with the help of a surface rearrangement and/or absorption, the planes (100) and (110) could become smooth.
2. The activation energy of smooth crystallographic planes contains the free energy of the critical nucleus. The energy wall of the chemical reaction and diffusion in solution affect activation energy. The former is an anisotropic factor and the latter an isotropic factor. The anisotropic factor does not have any effect on uneven planes. Because it has the greatest step free energy, the (111) plane has the greatest activation energy, in other words, the (111) plane etches the slowest.
3. Both the difference of the chemical potential ($\Delta\mu$) and of the step free energy (γ) depend on the etch type. These parameters perhaps explain a part of the variation of the etching rate, of separate degrees of anisotropy and of the dependence on the temperature of the etchant.

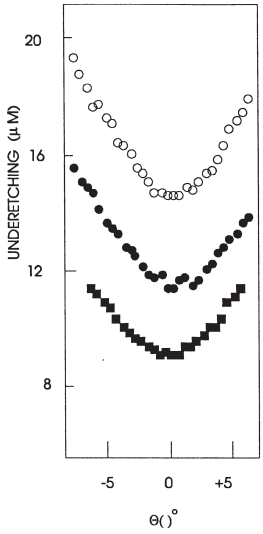


Fig 16. Under-etching of (111) plane as a function of the corner mistake in KOH etchant (40%). White circles: 30 °C, 300 min; black rectangles 70 °C, 15 min; black circles 108 °C, 3 min [Elwenspoek 1994].

4. In Fig 16, the under-etching of the smooth plane increases as a function of the corner mistake. The under-etching increases because the etching direction changes. In that case, the steps of the new etching direction reveal and the etching takes place faster. Because the density of the steps is proportional to the size of the corner mistake, the etching rate is also proportional to the size of corner mistake.
5. Information about the physical state of the real crystal surface can be obtained from the etching results. However, the direct results of the state of the crystal surface will be obtained only when the surface is in contact with the vacuum. How the crystal surface will react when it is in contact with water, KOH or something else can be quite separate from that of a vacuum.
6. The crystal equilibrium dominate smooth planes which have the smallest surface free energy (= a surface tension). There is great step free energy on these planes, in other words they grow and etch slowly. When the surface tension or form of the balance is known, the growing and etching behaviour of planes can be estimated.

7. The nucleation wall of the smooth plane will fail when the under-saturation of the etchant grows such that $\Delta G^* << kT$. In that case every vacancy which has formed with a thermal variation will serve as the nucleation centre and the smooth plane will etch at a rate that corresponds to the uneven plane. This situation is known as a kinetic inequality. When all the planes are kinetically unequal, anisotropic etching will change to isotropic etching. In KOH etching, the under-saturation is high at the beginning of the process and the etching is isotropic. In isotropic HF:NHO_3 etchant, the etching will change after a long etching time to anisotropic when the under-saturation of the etchant falls below the starting point of the kinetic inequality.

2.3 Atomistic model

The theory of silicon wet etching based on the probability of removal of an atom as an explicit function of the number of its nearest and second nearest neighbours was presented by the author and colleagues [Gosálvez 2001]. The considerations and assumptions of the model are as follows:

1. Silicon atoms lie in the locations of a diamond structure.
2. The neighbourhood of an atom contains both nearest and second nearest neighbours (or, simply, 'first' and 'second' neighbours). There is thus a 'first neighbourhood' and a 'second neighbourhood'.
3. An atom is considered to be on the surface if the number of first neighbours is less than or equal to three. Such atoms are referred to as 'surface atoms'.
4. When a surface atom leaves, each first neighbour is left behind with one additional dangling bond, which is quickly paired by a hydroxide ion from the etching solution. For each first neighbour, this results in the weakening of the Si-Si back bonds to the rest of the structure. Therefore, when a surface atom is removed, the energy cost of breaking the bonds to its first neighbours depends not only on the number of first neighbours missing (i.e. hydroxide ions directly linked to the atom) but also on the number of missing second neighbours, because the presence of hydroxide ions in their locations additionally weakens the bonds which still keep the atom linked to the current first neighbours. This dependency on the number of first and second neighbours missing can be

stated as a dependency on the number of first and second neighbours that are still present in the neighbourhood. One number is related to the other by simple subtraction from the maximum possible number of first or second neighbours; 4 and 12, respectively.

5. The probability of removal of an atom with n_1 first neighbours and n_2 second neighbours, $p(n_1, n_2)$, is described by the following removal probability function:

$$p(n_1,n_2) = p_0 \frac{1}{1+e^{\beta\epsilon_1(n_1-n_1^0)}} \frac{1}{1+e^{\beta\epsilon_2(n_2-n_2^0)}} \qquad (15)$$

Where $\beta = 1/k_BT$, $p_0 = \left(1+e^{-\beta\varepsilon_1 n_1^0}\right)\left(1+e^{-\beta\varepsilon_2 n_2^0}\right)$ is used to satisfy $p(0,0) = 1$ and ε_1, ε_2, n_1^0 and n_2^0 the parameters of the model. The parameters ε_1 and ε_2 may be regarded as average energies of the interactions between first neighbours and between second neighbours, respectively. It is assumed that the energy of an atom with n_1 first neighbours and n_2 second neighbours is simply $E(n_1,n_2) = \varepsilon_1 n_1 + \varepsilon_2 n_2$. If only the first neighbourhood is considered it is noted that n_1 is a measure of the energy cost of the removal of an atom with n_1 first neighbours in units of ε_1. Therefore, ε_1 may be understood as the average energy cost of breaking one bond between first neighbours. Similarly, ε_2 may be considered as the average energy cost of suppressing the interaction between second neighbours.

6. The other two parameters, n_1^0 and n_2^0, can be understood as follows. The parameter n_1^0 is a threshold energy (in units of ε_1) below which an atom interacting only with its first neighbours will be dissolved at zero temperature, T = 0. Since n_1^0 is measured in units of ε_1, it also represents the average number of first-neighbour bonds that are broken at zero temperature as a result of the activity of the etchant. In this way, if the number of first neighbours, n_1, is less than n_1^0 then the atom will most likely be removed by the etchant at a finite temperature. Similarly, n_2^0 is a threshold energy (in units of ε_2) below which an atom that interacts only with its second neighbours will be dissolved at zero temperature. At a finite temperature, the atom will most likely be removed by the etchant if the number of second neighbours, n_2, is less than n_2^0.

The simulations show good agreement with the experiments. The model predicts the existence of fastest-etched planes, other than (110), in accordance with experimental findings, and describes accurately the evolution of under-etching below the masks for all mask orientations, including the slopes (as measured from the wafer surface) corresponding to the planes that appear below the mask. It is remarkable that such agreement is obtained with a difference in size scales of about five orders of magnitude. The results also show that the second neighbours must be fully incorporated into the modelling strategy in order to describe the under-etching processes with sufficient accuracy. The use of first neighbours alone, or a partial incorporation of the second neighbours, is not sufficient.

The model based on the physical hypothesis consisting of two independent mechanisms was presented by Lysko [2003]. The first mechanism is related to the electrostatic charge present at the sample interface. This charge is supposed to be responsible for the Si-Si bonds simultaneously break in specific locations of the crystal lattice and the whole mono atom layer (or several layers) being released to the etching solution. The etching vector associated with this mechanism is vertically oriented to the sample surface. The second mechanism of the model has the etching vector laterally oriented to the (111) plane and applies to the rough crystal surfaces and to the crystal planes other than (100) and (111). In the model, atoms that are highly exposed to the etching solution over the sample surface have lower activation energy and are etched away at much higher rates than with the vertical vector mechanism. This can be observed as a rough surface planarization and improvement of the crystal surface quality with the progress of the etching. The anisotropic etching model deals with the two stable silicon crystal planes (111) and (100), and five semi-stable crystal planes (110), (112), (113), (221), (331), which are present at the sample face, during the convex corner mask etching.

The mechanism of the convex corner undercutting by the theory of covalent bond density was explained by Dong *et al.* [Dong 2004]. The free bonds density of silicon atoms at the convex corner is higher than that in the common plane (111), so the convex corner is undercut during anisotropic wet etching. In contrast, silicon atoms have no free bonds at the concave corner, and the etching structure corresponds with the design.

All of these models explain the ideal etching of silicon. However, in the real etching process the results can vary dramatically from the ideal, as is shown in this work.

2.4 Modelling of anisotropic etching

Many different simulation tools have been developed to model anisotropic etching. The main simulation tools are those developed by Camon *et al.* [Camon 1996], van Scuhtelen *et al.* and van Veenendaal *et al.* [van Scuhtelen 1999, van Veenendaal 2000], Gosálvez *et al*. [Gosálvez 2001, Gosálvez 2002 1, Gosálvez 2002 2, Gosálvez 2003 1, Gosálvez 2003 2, Gosálvez 2003 3, Gosálvez 2009], Chahoud [Chahoud 2005], Nguyen and Elwenspoek [Nguyen 2006] and Zhou *et al.* [Zhou Z-F. 2006].

Simulation tools based on atomistic scale simulations are presented by Camon *et al.*, Gosálvez *et al.,* Chahoud and Zhou *et al.* Simulation tools using a physical model based on the network etch rate function are presented by van Scuhtelen *et al.* and van Veenendaal *et al.* and also by Nguyen and Elwenspoek. The main difference between these models is that the atomistic model is based on the probability of removal of an atom and the physical model is based on two parameters; the roughness of the smooth planes and the velocity factor of steps on these planes.

2.5 TMAH and effects of surfactants

TMAH as a silicon etching solution has attracted a great deal of attention due to its compatibility with CMOS technology. KOH is not compatible with semiconductor processing technologies due to potassium ion contamination. Potassium ions are fatal to minority carriers in CMOS devices and cause non-functional or unreliable components. TMAH guarantees a very good relationship between the etch rates of SiO_2 and silicon and does not attack exposed aluminium to the same extent as KOH. Doping of TMAH solutions with silicic acid and ammonium peroxsodisulphate enhances the properties of TMAH as a CMOS etchant [Elwenspoek 1998, Kovacs 1998, Lindroos 2010]. On the other hand, the etch rates of (100) plane and the (100)/(111) etch rate ratios in TMAH are lower and the surface roughness is rather poorer than those of the wafers etched in KOH solutions [Zubel 2012].

At low TMAH concentrations of 15–25 wt-%, the etched (100) plane surfaces tend to be covered with hillocks [Tsaur 2001, Zubel 2008, Zubel 2012]. Shikida *et al.* presented a comprehensive study of the etching characteristics of TMAH. By etching a hemispherical silicon specimen the authors were able to determine the etch rates of several silicon crystal planes and provide valuable information about the influence of etching conditions on the results. The etch rates of (100) and (110) planes in 25 wt-% TMAH at 70 °C were determined to be 0.278 μm/min and 0.675 μm/min, respectively. This means that the (100)/(110) ratio lower than one was similar to that obtained in pure KOH solutions, although the etch rates were lower than in KOH at the same temperature. Furthermore, the surface roughness was worse than in KOH, with values of Ra = 0.065 μm and Ra = 0.675 μm for (100) and (110) plane surfaces, respectively. These authors also observed that stirring was beneficial, especially at TMAH concentrations below 10 wt-%, which was not observed in pure KOH solutions [Shikida 1999].

Extensive studies on etching in TMAH + Triton solutions have been carried out by Gosalvez *et al*. [Gosalvez 2009] and Tang *et al.* [Tang 2009]. They not only presented very interesting results but also made an attempt to interpret the phenomena occurring during the etching in TMAH with the addition of the surfactant. They also obtained a rapid reduction of (110) planes at high (25 wt-%) concentrations of TMAH containing small additions of Triton and achieved a highly improved finish. Xu *et al.* [Xu 2011] have studied the fabrication of ultra-smooth 45° micromirrors on (100) plane using low concentration TMAH water solution with a NCW-1002 surfactant. Surfactant additions at 0.1 wt-% level have also been characterized, and they have major effects on crystal plane selectivity [Lindroos 2010, Cheng 2006]. Surfactant NC-200 (0.1 wt-%) was added to TMAH solutions with concentrations of 10 wt-%, 20 wt-% and 25 wt-%. Polyoxyethylene-alkyl-phenyl-ether surfactant has a hydrophobic head '$CH_3(CH_2)_8–C_6H_4$' and a hydrophilic tail '$O(CH_2CH_2O)_2OH$'. The etching characteristics (such as etch rate, convex corner undercutting and etching anisotropy) change dramatically when a small amount of surfactant is added to TMAH solution. For example, TMAH with several percent surfactant (30 wt-% polyoxythene alkyl phenyl ether) added has the unusual property of etching <100> directions faster than <110> directions, leaving (110) planes exposed after short etches and, with 25 wt-%

TMAH + 0.1 wt-% NC-200 surfactant, convex corner undercutting was almost completely eliminated for etched depths of 20–25 µm.

2.6 Etch masking

It may be thought that all materials that etch at a low enough rate in the anisotropic etchant can be used as mask materials. However, there are some additional requirements:

- The mask layer has to be chemically stable in the etching solution.
- The mask layer has to have good adhesion with silicon. Poor adhesion leads to mask under-etching.
- The mask layer has to be defect-free; otherwise the etching solution penetrates into silicon via defects.
- Selectivity of 100:1 is already good, but 200:1 or even 400:1 would be better. However, 400:1 selectivity is not achievable to KOH.

Generally silicon oxide and silicon nitride are used as mask layers. Both fulfil the above conditions, and both are grown according to well-standardized processes and are compatible with CMOS process. Typical thicknesses of silicon oxide etching mask layers are 200–800 nm but with silicon nitride a thickness of only about 50 nm is used. Much thicker silicon oxide layers are needed because silicon oxide dissolves in KOH much faster than silicon nitride. In order to withstand KOH etching of about eight hours, silicon oxide has to be at least 500 nm thick. With silicon nitride the same eight-hour process needs only 50 nm thickness. This is fortunate, however, as silicon nitride over 50 nm thick has a very high tension and it can crack easily and would thus be unsuitable to use as the etch mask. Thick silicon oxide layers are made in wet oxidation where both hydrogen and oxygen are conducted into the reaction chamber and burnt as water. Silicon nitride mask layers are usually grown in LPCVD reactors.

An alternative masking for KOH etching is to use a polymeric protective coating or ultra-thin fluorocarbon top layer and sub-oxide lower layer [Normand 2002], sputtered and spin coated PMMA [Bodas 2005 1], RF sputtered PTFE [Bodas 2005 2], ProTEK® B2 material [Canavese 2007] or advanced spin-on photosensitive (negative

photoresist) polymeric etch protection mask [Dalvi-Malhotra 2008]. For example, the ProTEK® B2 material introduces important advantages in protecting silicon during KOH etching. The polymer can easily be spin-coated onto and removed from a wafer, and its endurance allows for more than three hours of etching. The polymeric protection can successfully replace silicon oxide or silicon nitride, thus avoiding additional invasive processes on the chip, because a high temperature is not required and no stress is induced on the surface [Canavese 2007]. However, PMMA coatings suffer from a lack of photosensitivity and insufficient adhesion. To provide photosensitivity and strong adhesion, an epoxy-containing polymer and a photoacid generator (PGA) are added to poly(styrene-co-acrylonitrile) materials. This new technology enhances the throughput by reducing the number of steps in the process and simplifies the process flow with minimal impact on the overall undercut performance [Dalvi-Malhotra 2008].

Polymeric masks were not used due to the huge effort needed to make such a drastic process change.

3. Properties of silicon

3.1 Silicon wafer manufacturing

Silicon wafer manufacturing is a multistep process that begins with purification of sand to metallurgical grade silicon and further processing to high-purity polysilicon (electronic grade silicon) and ends with final polishing and defect inspection. Two techniques dominate the production of single crystals. One is a zone-melting method commonly called the float-zone (FZ) method and the other is a pulling method called the Czochralski (CZ) method. Most single crystals, over 80%, are produced by the CZ method. If high purity or oxygen-free silicon is needed, the FZ method is used. In CZ crystal growth, a silica crucible (SiO_2) is filled with undoped electronic grade silicon. The dopant is introduced by adding pieces of doped silicon (for a low doping concentration) or elemental dopants P, B, Sb or As (for a high doping concentration). The crucible is heated in a vacuum to around 1420 °C to melt the silicon. A single-crystal ingot is pulled from the melted silicon. The main steps of ingot pulling are shown in Fig 17.

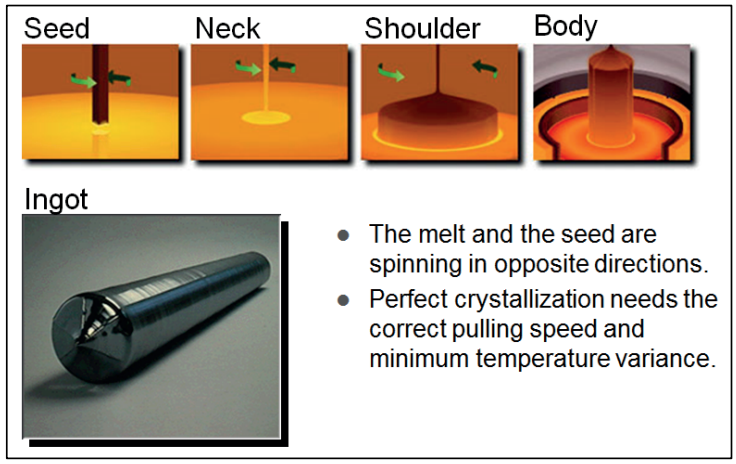


Fig 17. Single-crystalline silicon pulling by the Czochralski (CZ) Method.

The crystal orientation of the ingot is determined by the seed, of known crystal orientation. The seed is dipped into the silicon melt and the diameter of the ingot is determined by the pull and rotation rates. Impurities are incorporated from the melt into the ingot. All dopants and metallic impurities are enriched in the melt during the

pulling but the concentration of oxygen decreases as the pulling advances. This has to do with the decreased contact area between the melt and the quartz crucible and also with the flow patterns in the melt and the silica surface temperature. Magnetic field can be used to control the melt silicon. This is possible because molten silicon is electrically conductive. With a magnetic field, it is possible to reduce local temperature differences and also make the molten flow more stable. This leads to a stable melt and a more uniform ingot. The magnetic Czochralski (MCZ) growth method enables a better control of oxygen levels in the crystals. The effects of MCZ wafers in KOH etching are explored in chapter 7.1.

After crystal growth, the ingot is transformed into wafers by a long process which includes mechanical, thermal and chemical treatments and many cleaning and inspection steps. The main process steps in the standard wafer process are: slicing, edge rounding, lapping, slices etching, polishing and final clean. Fig 18 is a flowchart of the standard wafering process.

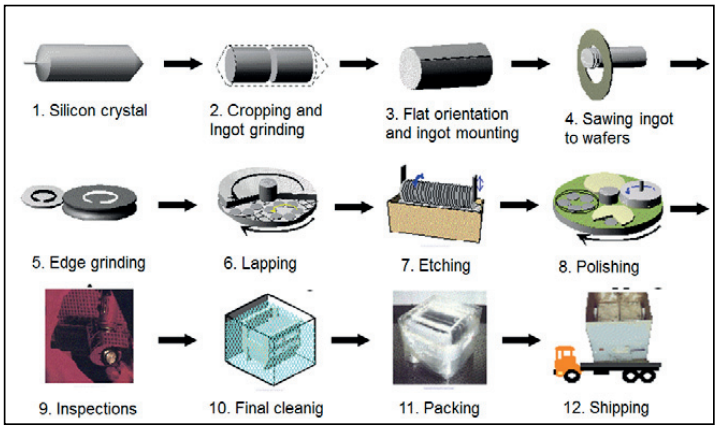


Fig 18. Flowchart of standard silicon wafering process.

The slicing step produces slices of silicon from a shaped ingot and critically defines the important factors of a wafer: its surface orientation, thickness, taper, bow and warp. The ingot must be rigidly mounted to maintain exact crystallographic orientation, obtained with X-ray diffraction, during the slicing process. A flat or a notch is ground into the ingot to establish orientation. The most common ways to slice ingots are inner diameter (ID) slicing or wire-saw slicing.

The edge rounding step can take place either before or after lapping. The edges of the silicon slices are rounded by an edge grinder. The edge rounding reduces mechanical defects, such as edge chips and cracks, substantially due to handling with tweezers or loading into furnace boats. The higher mechanical strength of the wafer edge ensures a lower incidence of process-induced plastic deformation (i.e., slip dislocations, which tend to concentrate at edge chips and cracks), and increases the wafer yield due to a lower frequency of wafer breakage during subsequent processes.

Lapping is performed on both sides of slides, primarily to remove the non-uniform damage left by slicing and to attain a high degree of parallelism and flatness of the slices. The abrasive slurry used for lapping is typically a mixture of alumina or silicon carbide and glycerine.

In the slice etching, the mechanical damage induced during the previous shaping steps is removed entirely by chemical etching. Both caustic (KOH) and acidic (HF-HNO_3) etches can be used. The high degree of flatness introduced in lapping is better preserved by caustic etching.

The polishing process produces a highly reflective and damage-free wafer surface. For example, in MEMS wafers both sides of the silicon wafer are polished if the processing is done on both sides of the wafer. The polishing of silicon is accomplished by a chemical-mechanical process using a polishing pad and polishing slurry of sodium hydroxide and fine silica particles. The removal rate and the resulting flatness and surface roughness of the wafer depend on various operating factors, such as temperature, pressure, pad material, rotation rates and slurry composition. In general a slower polishing rate, i.e. 0.1 µm/min, results in a smoother surface, i.e. <1 nm Rq roughness. High quality MEMS wafers have both sides polished simultaneously with special double-side polishing equipment modified from lapping tools.

The last but not least step in the standard silicon wafer process is the final clean. A primary concern in all microelectronic circuit and MEMS fabrication is the level of contamination/particles on the wafers and the removal of such contamination/particles

before further processing. The types of contaminants/particles range from organic compounds to metallic impurities that are encountered by handling or processing. Cleaning of wafers is absolutely necessary at many stages in device fabrication processes as well as in the initial wafer shaping processes. These contaminants/particles attach to the wafer surface either chemically or physically. A variety of wafer cleaning techniques have been used to remove various types of contamination/particles. The procedure most widely used in the semiconductor industry is the so-called Standard Clean (SC) method. This is a sequence of SC1 (ammonium hydroxide, hydrogen peroxide and DI wafer) solution, and SC2 (hydrochloric acid, hydrogen peroxide and DI water) solution, and finally dilute hydrofluoric acid (HF) solution. This procedure efficiently removes organic and metal contamination/particles and leaves the wafer surface hydrophobic.

3.2 Mechanical grinding and grinding damage

This thesis reports the pioneering efforts to replace standard polished wafers with lower-cost ground wafers in MEMS production.

In the future, semiconductors will require flatter wafers at a lower price. The method of lapping and polishing currently used to manufacture silicon wafers will not be able to meet the ever-increasing demand cost-effectively. Pei *et al.* [Pei 2005] report an experimental investigation into a grinding-based manufacturing method which has the potential to manufacture flat silicon wafers at a lower cost.

The most cost-effective method to reduce the thickness of a wafer with high accuracy and with low total thickness variation (TTV) is mechanical grinding (comprising both fine grinding, FG, and rough grinding, RG) [Yang Y. 2008, Zhang 2011]. However, grinding leads to damage to the wafer surface, which impacts on the mechanical properties of the wafer as well as on the electrical characteristics of the integrated circuits. In the grinding process, crystalline silicon (c-Si) is under huge compressive stress induced by the scratching of the diamond grits. In the loading cycle of indentation, Si-I (cubic diamond crystal structure) undergoes a phase transformation to metastable Si-II (β-tin crystal structure). When the load is released, the high-pressure phase turns into Si-III (body centred cubic crystal structure), Si-XII

(rhombohedral crystal structure) or amorphous silicon (a-Si), depending on the unloading rate. Other factors, such as shear stress due to the rotation of the wheel and heat generated by friction, facilitate the transformation to Si-II. In the grinding process, the grits sweep the wafer surface at high speed: therefore, the just-formed Si-II is immediately released from pressure and turns into amorphous Si.

Grinding damage and its distribution are summarized in multilayer damage models of FG-Si and RG-Si: see Figs 19a and 19b. The FG-Si model shows a relatively uniform layer build-up, consisting of a-Si (a few nanometres), plastically deformed Si (~2 μm), elastically stressed Si (~2 μm), and damage-free Si. There are irregularities associated with the surface roughness, and the top amorphous layer is extremely thin. Under a-Si condition, the stress never reaches the level necessary for phase transformation, whereas it is still enough to deform the silicon plastically.

a)

b)

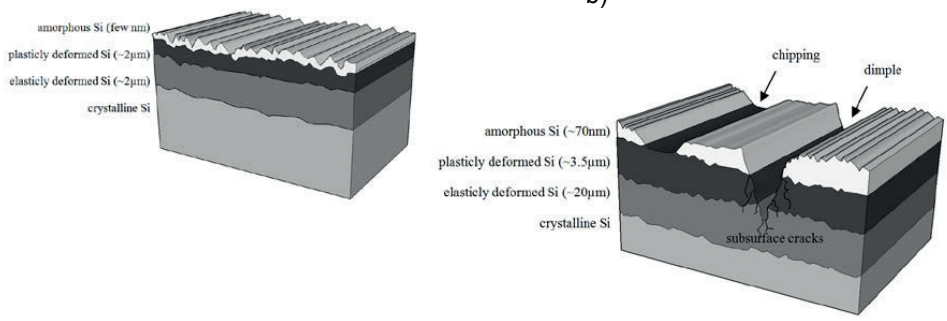


Fig 19. Damage models of FG-Si (a) and RG-Si (b) [redrawn fromYang Y 2008].

The RG-Si damage model is made up of ductile and brittle damage. Dimples from the brittle grinding are randomly mixed with the grinding grooves from the ductile grinding. The sharp corners of the dimples provide starting points for sub-surface cracks, which can propagate deeply with various shapes. Compared with the FG process, the load of RG is much higher and results in much greater thickness of each damaged layer. There are two kinds of regions on the RG-Si: grinding grooves and fracture dimples. The grinding grooves resemble the structure of the FG-Si, however with much thicker layers (a-Si ~70 nm, plastically deformed Si ~3.5 μm, and elastically stressed Si ~ 20

μm). Sub-surface cracks start from the corners of the dimples and propagate into the wafer.

The depth of the strain-induced damage layer by successively etching very thin layers from differently ground wafers, and measuring the strain-induced curvature (bow) between each etching step, was studied by Haapalinna [2004]. That study indicates that measurement of bow in silicon wafers was a sufficiently sensitive method to distinguish not only between the differences in surface and sub-surface damage caused by different grinding wheels, but also the differences due to varying grinding parameters. The bow value goes to the zero level below 0.2 μm removals in low damage wafers and 0.6 μm removals in higher damage wafers.

Preferential etches [Hull 1999] are etches that delineate crystal defects, such as cracks, dislocations, stacking faults and twins, by removing material faster where the defect meets the surface. Common preferential etches are, for example; Dash etch (1 HF (49%) : 3 HNO_3 (70%) : 10 CH_3COOH (100%)), Sirtl etch (1 HF (49%) : 1 CrO_3 (5M)) and Secco etch (HF (49%) : 1 $K_2Cr_2O_7$ (0.15M)). The etch-rate enhancement is due to a higher local reaction rate, rather than being transport-limited. KOH acts in a similar way. Spherical depressions arise from KOH preferential etching at some points on the surface of (100) plane in aqueous KOH with standard anisotropic etching conditions (20 wt-% and 60 °C) [van Veenendaal 2001 2]. The cause of this preferential etching might be small edge dislocation loops (associated with the stacking faults that emerge on (111) plane) or aggregates of point defects that etch away fast.

Coarse grind and fine grind surfaces which are etched for about 60 seconds in 20 wt-% and 60 °C KOH are shown in Figs 20a and 20b. On the etched surface, it can see cracks caused by coarse grinding which are enlarged in KOH etching. KOH etchant penetrates into the cracks and etches the surrounding silicon much faster because in the crack there are many other crystal planes to attach which etch much faster than the (100) surface plane. This phenomenon can be seen when the fine grind removal is too shallow and the subsurface damage caused by coarse grind is not removed totally in the fine grind process step. Chapters 7.2 and 7.3 explores the effects of using ground wafers in KOH etching.

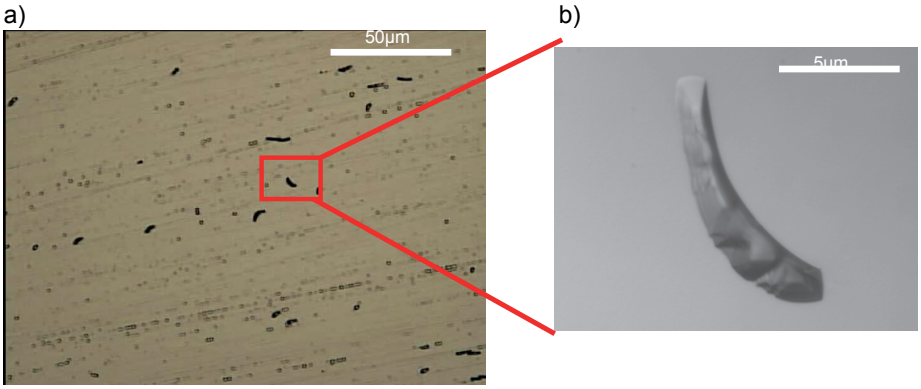


Fig 20. Fine-grind silicon surface, preferential etched with KOH (20 wt-% and 60 °C) for 60 s, which still has subsurface damage caused by coarse grinding.

3.3 Crystal defects

Lattice structure theories [Shimura 1989] are based on the ideal crystal yield strength, which is calculated to be from 100 to 10,000 times greater than the value of a real crystal of the measured value. The same paradox is in magnetic permeability, and other known structure sensitive properties. The difference between theory and practice is due to the defects that exist in all real crystals. Defects in the lattice are the points where the atomic positions differ from the regular grid. The majority of the atoms in a crystal are in regular lattice positions, and crystal defects disturbances extend over relatively small areas in the lattice, but still crystal defects influence sensitive properties crucial to the crystal structure.

Since crystal defects must adapt to a regular environment, they occur with certain regularity. This forced adaptation limits the number of potential crystal defects so that they occur within a relatively small number of types. Crystal defects are grouped into four categories: point defects, and one-, two- and three-dimensional defects. Point defects are classified as internal (intrinsic) and external (extrinsic) points, like errors. Internal point defects are vacancies and self-interstitial atoms, and external point defects are substitution impurity atoms and interstitial impurity atoms. One-dimensional crystal defects are called dislocations. Two-dimensional crystal defects

are stacking faults, twins and grain boundaries, and three-dimensional crystal defects are voids and negative crystals which are composed of several voids and precipitates.

3.3.1 Internal point defects

A self-interstitial atom-and-vacancy pair is called a Frenkel defect. It occurs when the atom moves to its own lattice position, for example, as a result of thermal vibration of the intermediate rather than an atom, and an empty space or vacancy remains. Vacancies are also formed if the lattice position atom diffuses on the surface of the crystal to form a new surface. This is called a Schottky defect.

The energy required to form a vacancy is about 1 eV, and this is achieved by heating the crystals sufficiently. When the high temperature of the crystal is cooled rapidly, vacancies cannot be filled and they remain on the crystal. Furthermore, a plastic deformation or an irradiation (e.g. neutron bombardment) generates vacancies. The sources of the vacancies are free surfaces, grain boundaries and dislocations. The thermodynamic stability requires that the crystalline material always has vacancies the number of which depends on the temperature. In an equilibrium situation vacancies form at the same rate as they are filled. The switching of vacancies in the crystal happens so that one of the surrounding atoms is transferred into a free position from its initial position and the atom's initial position becomes a vacancy. Since the lattice atoms are relatively easy to move, empty locations and vacancies promote diffusion in crystal. Vacancies also act as traps of charge carriers and as promoters of impurity diffusion.

3.3.2 External point defects

Impurity location is determined by crystal matrix and differences in impurity size and electrical charges. Interstitial atoms are atoms of foreign material which are in the intermediate positions in the crystal lattice. Often, the interstitial atom is too large for the available space. Consequently, an elastic field will arise when the surrounding atoms move from their initial positions. Substitution impurity atoms are atoms of foreign material which are in the crystal lattice points. Due to the size difference,

substitution impurity atoms cause stress in their environment but do not actually change the structure of the lattice, so they are not exactly crystal defects. Therefore, semiconductors are intentionally doped with substitution impurity atoms to improve their electrical characteristics. For example, silicon is doped with B (p-type semiconductor), and P, As, Sb (n-type semiconductor).

The foreign substitution impurity atoms have harmful effects on semiconductor properties. The most harmful impurities in silicon are K, Na, Cr, Fe, Cu, Co and Ni, which cause large electrical change, distort the lattice and behave like traps for minority charge carriers. These unwanted impurities accumulate in the various stages in the semiconductor process, and therefore semiconductor products are manufactured in extremely clean environments. Some impurities in silicon, such as oxygen, are desirable. Oxygen strengthens the silicon wafer and promotes internal gettering, which means internal transport of harmful impurities to the inner part of wafer, and therefore, leaves cleaner surfaces to use in IC manufacturing.

3.3.3 One-dimensional crystal defects

One-dimensional crystal defects are called dislocations. When the silicon crystal is under external stress, it first yields elastically then, after the yield point, plastically. The permanent deformation occurs in such a way that the dense packing crystal planes (111) slide relative to each other along dense packing directions <110>. In dislocations the atomic planes change atomic bonds locally. In the centre of the dislocation, atoms are moved symmetrically from their initial positions. Due to this definition, the dislocation cannot end in the crystal, instead it ends either on the free surface of the grain boundaries or the second dislocation, or it forms a closed loop, i.e. the dislocation loop. Although dislocation means disturbance to the regular crystal structure, the structure is completely determined. The structure varies according to the direction in which the dislocation passes through the crystal. Edge dislocation is perpendicular to the direction against the slide, while screw dislocation is parallel with a sliding direction. Straight dislocations that move over long distances are the most harmful. These form, e.g. diffusion pipes and spikes in epitaxial (EPI) layers which cause severe functional disorders through leakage of currents and/or destruction of the component. Dislocations also reduce the minority charge carrier's lifetime.

Dislocations move very easily in hot single-crystal silicon, during thermal stress [Huang 2005] or especially during crystal growth. For this reason, the conditions of the crystal growing process need to be as stable as possible in order not to create dislocations. In practice, the transition of direct dislocations to the crystal can be prevented completely by growing a thin neck at the top of the ingot (3–4 mm thick) (see Fig 17) and a tapered tail at the other end.

3.3.4 Two-dimensional crystal defects

Two-dimensional crystal defects are stacking faults, twins and grain boundaries. Stacking fault consists of an incomplete transition to the atomic plane (Shockley partial dislocation) or when the lattice generates excess atomic plane (Fig. 21a) or absent atomic plane (Fig. 21b). These are called Frank partial dislocations. The effects of two-dimensional crystal defects in KOH etching are explored in chapters 7.1, 7.2 and 7.3.

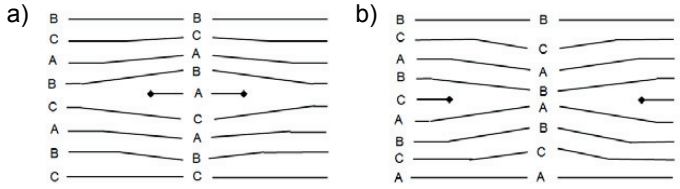


Fig 21. Stacking faults generated by excess atomic plane (a) or absent atomic plane (b). These are called Frank partial dislocations.

A stacking fault is generated in the case of Frank partial dislocation when an atom group expands to the extra atomic plane or a vacancy group expands as a missing atomic plane. An extraordinary number of atoms arise, for example, during crystal growth or during other plastic deformation, e.g. grinding. Missing the atomic level born though of the so-called vacancy collapse in which a large number of vacancies are collected on the same atom plane. In that phenomenon, the wrong atomic planes are in contact with each other. Such a stacking fault is only possible in EPI layers.

Twins and grain boundaries are wide-ranging and thus easy to notice during crystal growth process and to remove afterwards. Twins are generated with slip sliding or

mechanical twinning during crystal growth. The structure is symmetrical on both sides of twins but they are a mirror image of each other. Grain boundaries arise in crystal growth when the dislocations lock in to the line and the crystal loses its structure. In this case, the crystal cannot be used in semiconductor manufacturing due to its inhomogeneity.

3.3.5 Three-dimensional crystal defects

Three-dimensional crystal defects are voids and negative crystals (which are composed of several voids) and precipitates. When a number of vacancies combine together, a void (empty cavity of the crystal) is generated. These occur during crystal growth [Choe 1995, Hwang 2003, Yu 2004] by the combined effects of the speed of crystal pull and rotation, as well as the viscosity of the melt silicon. However, voids are rare in CZ-grown silicon crystals. Negative crystals consist of a number of voids.

Precipitate is an impurity caused or formed in a faulty area in the lattice. It occurs when the temperature change (normally a decrease) occurs in crystal at a supersaturated temperature and the crystal matrix is no longer able to keep the impurity in the intermediate position in the crystal lattice and it is expelled out of the lattice. Driven by diffusion, the impurity atoms pass to crystal defects, if there are any, and heterogeneously nucleate there. However, if there are no crystal defects in the crystal matrix, the precipitates nucleate randomly, which is referred to as homogeneous nucleation. Heterogeneous nucleation is much more common than homogeneous nucleation. Diffusion drives atoms in to precipitates which expand until they reach solubility balance.

Precipitates strengthen the crystal structure by preventing the movement of dislocations. The main precipitates in semiconductors are caused by metals or by oxygen. In silicon, precipitates are formed to SiO_2 and to MeSi (silicide). Since the SiO_2 takes approximately double the volume of single atoms, a stacking fault is generated around the precipitate. This partial dislocation absorbs metals and other impurities. This generation of precipitates is used in the internal gettering process in wafer manufacturing when the wafer surface is cleaned of impurities.

In standard Czochralski (CZ)-grown silicon wafer [Choe 2004] the amount of oxygen is 15 – 20 ppma. With magnetic-field-assisted Czochralski (MCZ) crystal growth, the amount of oxygen is reduced to 4 – 11 ppma. The oxygen level in silicon influences many applications in addition to etching. Low oxygen level wafers are used to fabricate particle detectors with improved radiation hardness [Härkönen 2005]. High oxygen level wafers improve floating-gate-type flash memory characteristics [Hirano 2007]. Slip propagation from wafer edge to wafer centre and surface dislocation are explained by the plastic deformation of wafer due to the relaxation of internal stress during wafer cooling after high temperature steps. In high oxygen concentration wafers, the oxygen precipitates prevent the propagation of slip. Therefore, the selection of wafers for integrated systems with both electronics and MEMS parts may have opposing requirements concerning oxygen levels of the wafers. The effects of oxygen level in KOH etching are explored in chapter 7.1.

3.4 Wafer characterization

3.4.1 Wafer thickness and flatness definitions

Flatness is one of the most critical parameters of MEMS wafers [Shimura 1989]. It directly impacts the line width capability, process latitude and throughput of a device. The process and the equipment used to fabricate devices define the flatness that can be achieved. Processes utilizing 1 x 1 imaging systems are sensitive to global flatness (Fig 22), whereas stepper imaging systems are sensitive to local site flatness (Fig 23). The most common parameter analysed is total indicating reading (TIR) for a vacuum chuck mounted wafer. As Fig 22 depicts, TIR concerns front-side referenced measurements. An imaginary reference plane is superimposed on the surface, approximating a least squares fit of that surface. The TIR is defined as the sum of the maximum positive and negative deviation from this reference plane. If the reference is chosen to coincide with the focal plane of the mask aligner, the focal plane deviation (FPD) is defined as the largest deviation, positive or negative, from this plane.

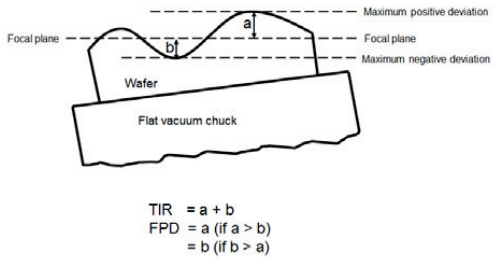


Fig 22. Global flatness with characteristic TIR and FPD [redrawn from Shimura 1989].

In order to determine specified local site flatness, it is necessary to simulate wafer stepper equipment. Fig 23 shows a wafer divided into an array that represents exposure areas of typically 15 x 15 mm or 20 x 20 mm. Viewing the site cross section of a square chip, TIR or FPD can be defined for each exposure site.

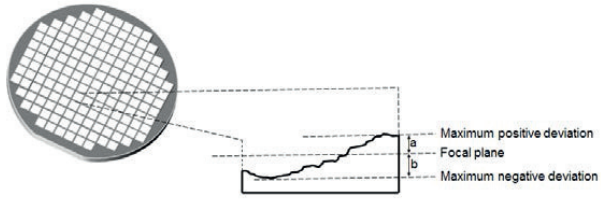


Fig 23. Local site flatness for wafer divided into exposure arrays [redrawn from Shimura 1989].

Bow relates to the concave or convex deformation of a wafer and is independent of thickness variation because it is applied to both polished and unpolished slices in a free unclamped state. Reading the two values a and b of Fig 24, the wafer bow is defined as half of the measured value, that is, (a-b) / 2.

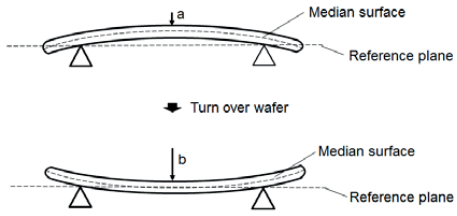


Fig 24. Wafer bow and its measurements [redrawn from Shimura 1989].

As shown in Fig 25, the bow may not affect the photolithographic processes if the wafer surface is sufficiently flat. In extreme cases, however, the clamping action of vacuum chucking cannot remove the bow entirely. The presence of excessive thickness variation and warp of a silicon wafer will affect its ability to perform high quality line imaging. A wafer warped by thermal processing may cause an additional problem of difficulty in vacuum chuck mounting.

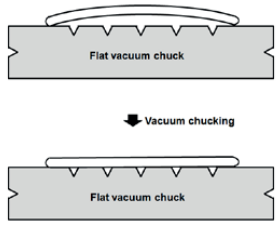


Fig 25. Removal of wafer bow by flat vacuum chucking [redrawn from Shimura 1989]

Warp is defined as the difference between the maximum and minimum distances of the median surface of the wafer from a reference plane encountered during the scanning pattern. Total thickness variation (TTV) is defined as the difference between the maximum and minimum values of thickness of the wafer. Fig 26 depicts some deformed wafer shapes with related warp and TTV.

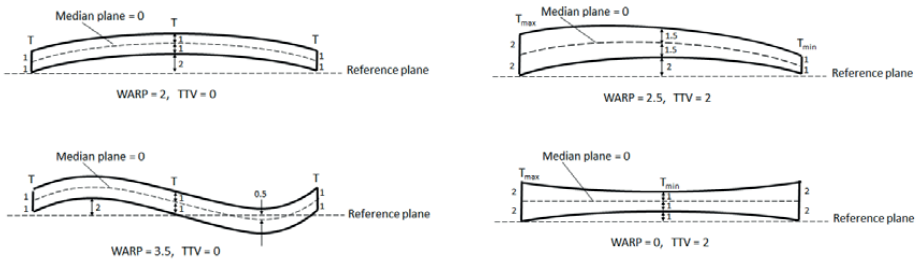


Fig 26. Deformed wafer shapes with related Warp and TTV [redrawn from Shimura 1989]

The wafers used in wet etched accelerometer production must have very low TTV value. The best results are achieved when TTV is well below 1 µm. Local site flatness is not applicable because local thickness deviation cannot compensate in whole wafer etching process. Bow and warp should be at low levels, below 30 µm is usually acceptable.

3.4.2 Microscopy and visualization

Optical microscopy resolution is roughly one micrometre, i.e. similar to wavelength. This is useful for practically all MEMS and solar cell and display devices, while for modern ICs and nanotechnology it is hopelessly inadequate. Electron microscopes can distinguish much smaller features. SEM (scanning electron microscopy) can detect features about 5 nm in size, and TEM (transmission electron microscopy) can even see atoms. However, the preparation of samples for TEM is difficult and time consuming. SEM operates very much like an optical microscope but with higher magnification and better depth of focus.

SPM (scanning probe microscopy) uses a sharp nanoneedle tip on a soft cantilever to scan the sample. One SPM technique is AFM (atomic force microscopy). It has a resolution on the scale of nanometres and it is a favourite measuring tool in microfabrication. The AFM is popular as a surface characterization tool but it is also very good for measuring lateral and vertical dimensions in the micrometre and nanometre range.

Surface roughness is described with many parameters. It can be calculated either on a profile (line) or on a surface (area). The profile roughness parameters (Ra and Rq) are more common but the area roughness parameters (Sa and Sq) give more significant values. Ra and Sa are arithmetic averages of absolute values, and Rq and Sq are root mean squared, that is, a statistical measure of the magnitude of a varying quantity. In practice, from the same surface, the Ra or Sa values are always smaller values than Rq or Sq values.

4. KOH etching of silicon

4.1 KOH etching parameters

The first detailed study of the KOH etching parameters was conducted by Price [1973]. Studying the mixture of water, KOH and isopropyl alcohol, he noticed the maximum etching rate was reached at around 30 wt-% KOH. Without the addition of alcohol, the maximum etching rate was reached at 10–15 wt-%. Price noticed generally that the addition of isopropyl alcohol reduced the etching rate and that the activation energy of the (100) plane was between 0.52 and 0.69 eV. With the mixture, he did not notice any effect on the etching rate, which he interpreted as pointing to the fact that the reaction is not dependent on diffusion. In optimum conditions, Price achieved an etch ratio of 35:1 between crystal planes (100) and (111). Kendall [1979] achieved the etch ratio of 500:1 at 55 wt-% KOH between the same crystal planes. More information on (110), (111) and SiO_2 etch ratios was published by Clark and colleagues [1987]. According to them, in 9–54 wt-% KOH solutions the activation energies for the various crystal planes were: (110): 0.6–0.8 eV, (111): 0.4–0.9 eV and SiO_2: 0.8–1.0 eV.

The most important issue in the anisotropic behaviour of silicon in caustic echants is the etching of the (111) plane, which is much slower than the others. The activation energy of the (111) plane has been measured at 0.7 eV [Seidel 1990 1]. In 100 ˚C KOH solution, the etching ratios of the planes (110):(100):(111) were 50:30:1 and in KOH at room temperature the etching ratios were 160:100:1. In spite of nearly the same activation energies ((100) = 0.59 eV and (110) = 0.61 eV) (110) plane etched 60% faster than (100) plane.

Table 1 shows the etching rates of the (100) plane as a function of temperature and KOH concentration to 1–10 Ω–cm wafers. The values in Table 1 have been calculated according to Fig 10 from which a function (16) is obtained for the etching rate:

$$R = k_o [H_2O]^4 [KOH]^{1/4} e^{(-E_a/kT)} \quad (16)$$

In equation (16): E_a = 0.595 eV and k_o = 2480 μm/h.

Table 1. Etching rates of the (100) plane (μm/h) in different concentrations and temperatures for 1–10 Ω-cm wafers [Seidel 1990 1].

	Temperature[˚C]								
% KOH	20˚	30˚	40˚	50˚	60˚	70˚	80˚	90˚	100˚
10	1.49	3.2	6.7	13.3	25.2	46	82	140	233
15	1.56	3.4	7.0	14.0	26.5	49	86	147	245
20	1.57	3.4	7.1	14.0	26.7	49	86	148	246
25	1.53	3.3	6.9	13.6	25.9	47	84	144	239
30	1.44	3.1	6.5	12.8	24.4	45	79	135	225
35	1.32	2.9	5.9	11.8	22.3	41	72	124	206
40	1.17	2.5	5.3	10.5	19.9	36	64	110	184
45	1.01	2.2	4.6	9.0	17.1	31	55	95	158
50	0.84	1.8	3.8	7.5	14.2	26	46	79	131
55	0.66	1.4	3.0	5.9	11.2	21	36	62	104
60	0.50	1.1	2.2	4.4	8.4	15	27	47	78

The fastest etching plane was identified as (411) by Mayer *et al.* [1990] in conditions of 15–50 wt-% and 60–100 °C KOH. When a convex corner is under-etched it becomes blunt corner, as shown in Fig 27. In under-etching the (411) planes will overlap an uneven surface (110).

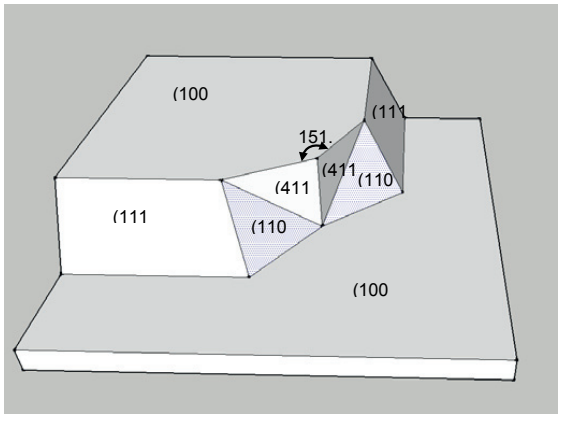


Fig 27. The convex corner under-etching and formation of the fastest etching plane [redrawn from Mayer 1990].

Experiments with etching on spherical surfaces [Sato 1997, Sato 1998, Tokaro 1998] differed from the results of Mayer *et al.* (Fig 28). Sato *et al.* found that at 40 °C and 40 wt-% KOH the fastest etching plane is the (110) plane. When the temperature increases, this fastest etching plane will differ maximum two, which are at 70 °C for the (540) plane and at 90 °C for the (320) plane. In 30 wt-% solution, the situation is the same although there are already two fastest etching planes at 40 °C. At a temperature of 70 °C, the maximum etch rate is at the (530) plane, and at 90 °C the maximum etch rate is at the (210) plane. Very similar results were obtained by Ju *et al.* [Ju 1992] and Hesketh *et al.* [Hesketh 1993].

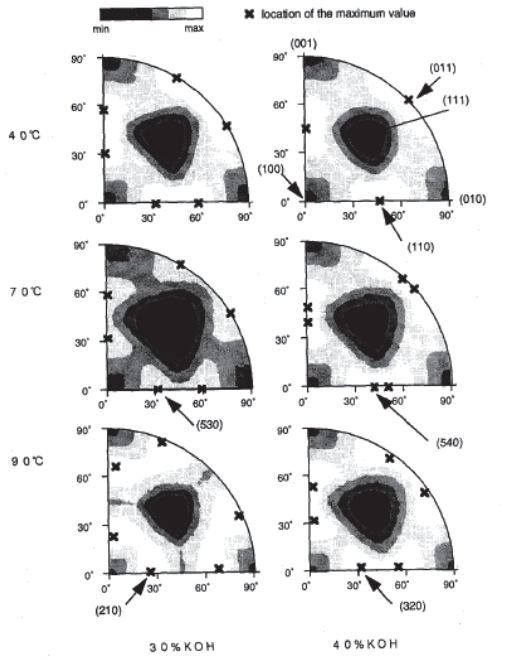


Fig 28. Fastest etching planes in a single-crystal silicon spherical in different temperatures and different concentrations [Sato 1997].

Table 2 [Sato 1998] presents the values of the etching rates of the different crystal planes in three different concentrations of KOH.

Table 2. Etching rates of the different crystal planes (μm/min) in three different concentrations at a temperature of 70 °C. The values in brackets have been normalized according to the (110) plane [Sato 1998].

	KOH concentration					
	30 wt-%		40 wt-%		50 wt-%	
Crystallographic orientation	rate (μm/min)	normalized rate	rate (μm/min)	normalized rate	rate (μm/min)	normalized rate
(100)	0.797	(0.548)	0.599	(0.463)	0.539	(0.619)
(110)	1.455	(1.000)	1.294	(1.000)	0.870	(1.000)
(210)	1.561	(1.072)	1.233	(0.953)	0.959	(1.103)
(211)	1.319	(0.906)	0.950	(0.734)	0.621	(0.714)
(221)	0.714	(0.491)	0.544	(0.420)	0.322	(0.371)
(310)	1.456	(1.000)	1.088	(0.841)	0.757	(0.871)
(311)	1.436	(0.987)	1.067	(0.824)	0.746	(0.858)
(320)	1.543	(1.060)	1.287	(0.995)	1.013	(1.165)
(331)	1.160	(0.797)	0.800	(0.619)	0.489	(0.563)
(530)	1.556	(1.069)	1.280	(0.989)	1.033	(1.188)
(540)	1.512	(1.039)	1.529	(0.994)	0.914	(1.051)
(111)	0.005	(0.004)	0.009	(0.007)	0.009	(0.010)

Two-step anisotropic etching for polygon-shaped microstructures was studied by Kang, Haskard and Samaan [1997]. The structure was obtained by a two-step etching process on a (100) silicon wafer using a 40 wt-% KOH silicon anisotropic etching solution at 85 °C. The (111) plane was created during the first normal anisotropic etching process and the high-index plane was obtained from a second etching step without a silicon dioxide mask. The new plane was considered as a (310) plane, having an angle of 18.43° to the (100) plane. Kang *et al.* considered that a polygon-shaped microstructure can easily be obtained by this method and the structure has excellent reproducibility due to the anisotropic characteristics of the silicon orientation. The method has been successfully applied by Kang *et al.* to fabricate a silicon micromould for a plug-type microvalve. Studies of etching silicon structures bounded by (311) sidewalls were continued by Resnik *et al.* [2000]. They concluded that convex corners of (311) intersections were significantly less undercut compared with mask etching mode while severe rounding occurred at concave corners. Self-

compensation of convex corners can be achieved in KOH solution, while in TMAH this effect is not generally achievable, except for small initial undercuts. Based on this process Burt *et al.* [2007] introduced a simple method for high yield fabrication of sharp silicon tips.

Undercutting phenomena were studied by Shikida *et al.* [2002] with a (100) silicon wafer to explain why a (311) plane appears under the convex corner of a masking area, and why the plane is stable during the etching process. They analysed the etching rate as a function of crystallographic orientations and found that the (311) plane has unique etching characteristics. The (311) plane is located at the saddle point in the etching-rate diagram (Fig 29). The saddle point in the etching diagram depends on the etching conditions. For example, the point is located around the (311) plane when the KOH concentration is 34 wt-%. In this case, the facet that actually appeared in the undercut area was also a (311) plane, and not a (411) plane, as described by Mayer *et al*. [1990]. Therefore, Shikida *et al.* continue their discussion assuming that the facet plane that appeared was a (311) plane. The (100) plane on high boron doped wafers and the plane with the fastest etching as a function of temperature and concentration are explored in chapter 6.1.

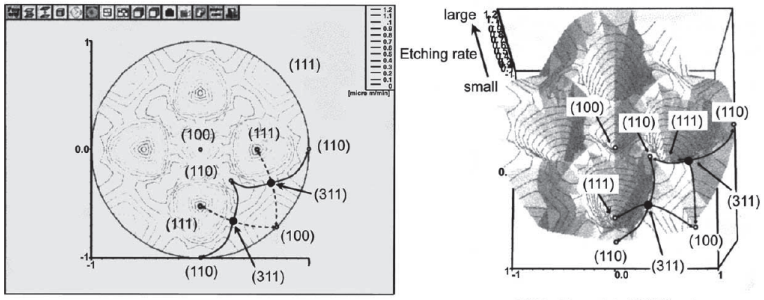


Fig 29. Distribution pattern of etching rate showing saddle point of (311) plane (34.0 wt-% KOH) [Shikida 2002].

The etching characteristics of planes (100) and (110) at high temperature ranges near the boiling point of KOH solutions were studied by Tanaka *et al*. [2004]. The etching rates of planes (100) and (110) at near the boiling point were 5–9 times and 4–20 times higher, respectively, than those at 80 °C in KOH concentrations of more than 32

wt-%. At 145 °C in 50 wt-% KOH, a (100) plane smooth surface was achieved with a high etching rate of 9.7 µm/min and at 135 °C in 45–47 wt-% KOH, a (110) plane smooth surface was achieved with an ultra-high etching rate of 20 µm/min. Arrhenius plots of the etching rates were linear from 80 °C to near the boiling point. Tanaka *et al*. considered that the activation process at the higher temperature is the same as that at the lower temperature.

4.1.1 Etchant agitation

The effects of agitation of the etchant have been studied for decades. Agitation prevents settling of the etchant and results in more uniform etching. King *et al.* [1991] studied mechanical mixing. More studies have been done with ultrasonic agitation [Tabata 1991, Kuntman 1992, Sheu 2001, Chen 2002, Kim 2004, Nüsse 2004, Yang C-R 2005 1, Park 2008]. There is also at least one study [Dziuban 2000] of microwave enhanced etching.

Especially small and deep grooves [Nüsse 2004] with a high aspect ratio cause difficulties in conventional etching because the time controlled etching process is often not reproducible. Rough bottoms to etched cavities are also found. The main reason for these problems is hydrogen which is a by-product of the chemical reaction. Hydrogen settles down on the surface of the wafer until a bubble is formed big enough to loosen into the solution. During that retention period, the silicon is micro-masked and, consequently, the reaction in that area is interrupted for some time. To drive hydrogen out of small gaps is even more difficult, so that the etching rate decreases with the depth of the groove. Without use of ultrasound, anisotropic KOH etching of deep trenches always leads to insufficient results, e.g. rough surfaces. The effects of agitation in KOH etching are explored in chapter 6.2.

4.1.2 Dissolved silicon

The effect of dissolved silicon on KOH etchant was studied by Dorsch, Hein and Obermeier [1997]. Silicon was dissolved in KOH (33 wt-% at 80 °C) and the change of the etching rate was followed as a function of the amount of dissolved silicon. The density of the KOH solution increased from 1.33 g/cm^3 for zero dissolved silicon to 1.55 g/cm^3 for 190 mg/cm^3 dissolved silicon with almost linear dependence. The maximum amount of dissolved silicon used in the study was 190 mg/cm^3, which corresponds to the density 1.561 g/cm^3 of KOH. The etching rate of the (100) plane as a function of the dissolved silicon increased by 7% of its initial value and at its maximum there was 125 mg/cm^3 of dissolved silicon. The etching rate began to decrease after this point.

The anisotropy of the etching changes as a function of the amount of dissolved silicon, so that at over 58 mg/cm^3 the under-etching begins to increase and the oblique planes overlap more and more unevenly. The area of smooth (411) plane becomes smaller and the area of the uneven plane increases. With 160 mg/cm^3 the uneven oblique plane has formed and it is not possible to determine the plane direction. The effect of dissolved silicon can be avoided by changing the etchant frequently. Due to the contamination caused by dissolved silicon, fresh KOH is used for deep etching to improve reproducibility.

4.1.3 Boron doping concentration and etch-stop techniques

The effects of boron doping concentration on the silicon etching rate were studied by Seidel *et al.* [1990 2]. Fig 30a shows the results where the KOH temperature of the solution has been kept at 60 °C and compared with varying KOH concentrations and the effect on the etching rate of the different doped wafers. In the figure it can be noted that the etching rate decreases rapidly at all the KOH concentrations when the doping degree of the wafer rises more than 10^{19} cm^{-3}. However, the smaller the KOH concentration, the more rapid is the decrease of etching rate.

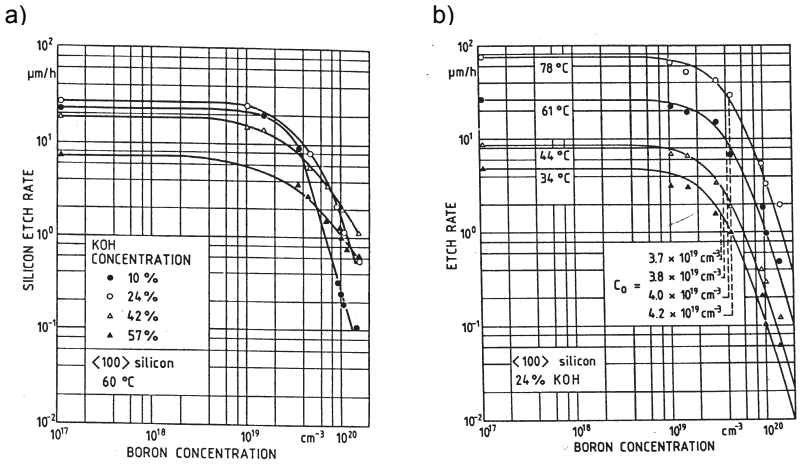


Fig 30. a. Change in the etching rate of the (100) plane as a function of boron doping concentration at different KOH concentrations [Seidel 1990 2]
b. Change in the etching rate of the (100) plane as a function of boron doping concentration at different KOH temperatures [Seidel 1990 2].

In Fig 30b, the concentration of the KOH solutions has been kept at 24 wt-% and the temperature of the solution has been varied. In that case also the etching rate will decrease fast at all temperatures when the degree of doping of the wafer rises more than 10^{19} cm^{-3}. In Fig 30b, one can further notice that the change in the etching rate is the same at different temperatures.

Very high boron doping causes non-uniform etching results. This can also be seen in Fig 30a, where the etching rate decreases rapidly as a function of boron concentration increase. The practical limit of wafer resistivity is about 0.017 Ohm-cm (> 10^{19} cm^{-3}). If the resistivity is lower than that, the etching result is not uniform over the wafer. However, if the resistivity goes higher than 0.023 Ohm-cm (< 9×10^{18} cm^{-3}) the electrical conductivity of the wafer is not high enough for most sensitive sensors. The higher the resistivity of the wafer, the greater is the electrical noise of the component.

The compatibility of a heavy boron doping process with bulk micromachining to fabricate silicon slabs a few microns thick was studied by Fonseca *et al*. [2008].

These doped slabs are advantageous as thermal spreaders and infrared absorbers in devices, such as microhotplates and thermopiles, built on free-standing membranes, which are used for different gas detection techniques (metal oxide gas sensors or non-dispersive infrared optical gas detection). In order to retain a silicon slab after wet anisotropic etching, heavily boron-doped regions must be previously defined in the silicon. The rationale for this is that anisotropic etchants will not affect the silicon nitride membrane nor heavily boron-doped regions since the etching reaction needs free electrons to proceed and the presence of electrons is scarce in those materials. In the case of those p++ regions the etch rate will not be zero but will decrease dramatically when boron concentration is above 10^{19} cm^{-3}. P+ etch stop technique is also used [Iosub 2002] in the fabrication of silicon membranes. Another etch-stop technique is electrochemical etch-stop technique [Voss 1991, Chung 2008].

In this thesis, the p+ etch stop technique is not used because the etched beams are in the centre of the wafer and it has not been possible to define heavily boron-doped regions in the wafer.

4.1.4 Alcohol additives and organic and inorganic agents

The effects of different alcohol additives to KOH and TMAH etching have been studied very thoroughly by Zubel and colleagues [1998 - 2012]. They have also studied the anisotropy effects of different organic and inorganic agents. Barycka and Zubel studied silicon monocrystalline wafers of (100), (110) and (111) orientations etched with OH-isopropanol solution [Barycka 1995]. They found that the etching rates are completely different in solutions of other compositions, which led to the development of other planes. For instance, the most rapidly etched planes in NaOH solutions are the (221) planes, whereas the (110) planes are not developed in this case because their etching rate is greater than that of the (100) plane.

The influence of caustic solution concentration, type of cation (K+ or Na+) and IPA additive on the etching rate of various crystallographic planes and the shape of etched figures was studied in [Zubel 1998 1]. The main result was that, in solutions of pure caustic KOH or NaOH, (110), (331), and (221) planes were etched more rapidly than the (100) plane. Consequently, as a result of the etching of holes, (100) planes

develop apart from (111) planes, the islands are limited by (221) and (331) planes of very fast etch rate, with very large under-etching. Isopropanol added to the etching solution causes a lowering of the etch rate of high index planes, but changes in the etch rate of these planes as compared with caustic solution alone also depend on the kind of cation used. Zubel *et al*. concluded that the influence of IPA on slowing the etching rate of high index planes is far stronger for K+ ions than for Na+ ions.

The main result of these studies [Zubel 2001 1] was the discovery of the 'IPA effect'. Molecules of IPA introduced to the KOH solution, similarly to TMA^+ ions (present in TMAH solution), adhere to some crystallographic planes, hindering the access of etching agents (OH^- ions and H_2O molecules) and slowing their etching rate. In effect the shapes of figures developed in TMAH solutions and in solutions of KOH with IPA additive are exactly alike, which suggests that a similar mechanism is involved in both processes. Zubel called this mechanism the 'IPA effect'.

The influence of atomic configuration of different planes on adsorption processes associated with anisotropic etching of silicon was studied in Zubel's second article of 2001 [Zubel 2001 2]. The process was carried out in KOH and TMAH solutions at a stabilized temperature, ranging from 60 to 90 °C. The concentration of KOH was changed from 3 to 10 M. The main result of the study was that in KOH + IPA solutions, the (110), (221), (331) or (441) planes develop even more slowly than the (100) plane, and are eventually the slowest ones in the above mentioned directions. The structures etched in KOH and in KOH + IPA solutions differ considerably from each other. From the fabrication point of view, it is especially important in etching of the structures with convex corners, used in the 'bossed' type structures applied in pressure sensors, for example. The KOH + IPA solutions, where the convex corners preserve much more regular shapes than in pure KOH, seem to be much more advantageous for the fabrication of that kind of structures.

Zubel *et al.* further found that other alcohols result in changing silicon etching anisotropy [Zubel 2002]. The alcohols with one hydroxyl group exhibited similar effects on isopropyl alcohol. They caused a strong reduction of etch rates of (hh1) type planes, usually developing at the side-walls of etched convex figures. This was the reason for the reduction of convex corner undercut (see Fig 31). The alcohols with

more than one hydroxyl group did not influence the etching anisotropy and caused deterioration of surface finish. The connection of alcohol properties with (hh1) etch rate reduction has been analysed. It has been stated that the advantageous effect of the alcohols from the propanol and butanol groups is connected with their low surface tension. The structures etched in KOH + tert-butanol solution imaged almost ideally in the shapes of etched mesas. Unfortunately, the etched surface was covered with numerous hillock-like structures. There were, however, areas free of hillocks which allow Zubel *et al.* to hope that some modification of the etching process (KOH advert-butanol concentration, temperature, stirring) will lead to the improvement of surface finish.

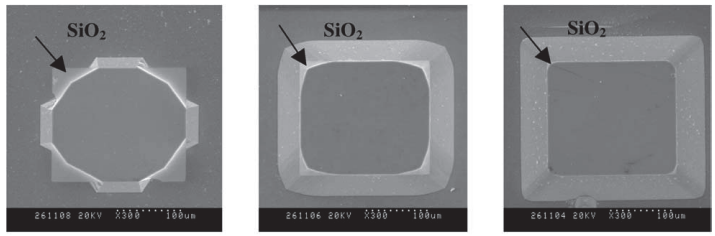


Fig 31. Convex figures etched in (a) 10M KOH solution (t = 30 min), (b) 5M KOH + IPA solution (t = 60 min), and (c) 5M KOH + tert-butanol solution (t = 60min) [Zubel 2002].

More recently, Zubel *et al*. studied the etch rates and morphologies of (100) and (110) plane surfaces etched in TMAH + Triton, TMAH + IPA and TMAH + butanol, as well as ternary TMAH solutions containing alcohols and surfactants [Zubel 2012]. TMAH solutions containing butanol seem to be superior to solutions containing IPA in terms of reduction of etched surface roughness. The best values of roughness parameters (Ra = 0.0322μm and Rq = 0.0549μm) were obtained for (110) surfaces etched in the ternary TMAH + Triton + butanol solutions. Another advantage of these solutions is the high boiling point of butanol (99.5 °C), which offers the possibility of carrying out the etching processes at elevated temperatures. The etching rate ratios for (100)/(110) planes obtained in TMAH + alcohol and TMAH + Triton + alcohol solutions were close to but usually lower than one. However, they were larger than the anisotropy ratio obtained in 25% TMAH. An inverse anisotropy for (100)/(110) > 1 was only achieved in TMAH + Triton solutions.

Various other researchers have also studied the influences of alcohol additives and organic and inorganic agents on KOH anisotropic etching. Anisotropic etching of silicon in a complexant redox caustic system was investigated in [Moldovan 1999]. Divan, Moldovan and Camon [Divan 1999] studied the influence of surface preparation prior to KOH etching and of surfactants added to the etchant over the etching rates and roughness of the (111) and (100) plane surfaces. C.-R. Yang *et al.* [Yang C-R 2005 2] studied three ion-typed surfactants, including anionic SDSS, cationic ASPEG and non-ionic PEG. In KOH solution with isopropyl alcohol added, a high KOH concentration and high temperature caused the selection of (100) instead of (110) plane walls, allowing reliable fabrication of (100) plane walls with improved surface smoothness due to the isopropyl alcohol [Powell 2001]. Very similar results have been obtained by others [Vázsonyi 2002, Chandrasekaran 2005].

The etching rates on the (100) and (110) planes at various temperatures and concentrations of a KOH/alcoholic moderator (glycerol, ethylene glycerol, 1.2-propanediol, 1.3-propanediol, isopropanol (IPA), or 1.5-pentanediol) were studied [Cho 2004]. The addition of 1.5-pentanediol to the KOH solution resulted in an improvement in the etching anisotropy as well as a smoother etched (100) surface than with the addition of IPA to the KOH solution. Another advantage of using KOH/1.5-pentanediol as etchant is that it could be used at higher temperatures (higher than 80 ˚C); where IPA had an evaporation problem.

Studies of the influences of alcohol additives on the etch rate of (111) planes have found totally opposite results. Philipsen [2009] concluded that hydrogen peroxide and isopropyl alcohol chemically ‘activate’ silicon surfaces, etching in KOH solution, which then leads to an increased chemical reactivity. Shah [2010] studied the absolute etch rate of silicon (111) with optical interferometry and found that the etch rate of the (111) plane is constant at 0.62 ±0.07 μm/h and independent of caustic concentration for 1–5 M KOH solutions at 60 ˚C. Only at lower caustic concentrations did the etch rate decrease and adding isopropanol slightly lowered the absolute etch rate.

In this thesis, no additives were used in KOH etching. The elements were designed for a pure KOH etching process. Redesign and process re-evaluation with additives would have been a major effort, especially because all prior work has used standard

n-type or p-type wafers and there are no reported effects on p++ type wafers that it is used. Even the oxygen levels of tested wafers are not always reported.

4.1.5 Metal impurities

Influences of pure metal impurities are less studied than the alcohol additives and organic and inorganic agents discussed in the preceding sections. The main studies in this area are carried out by [Hein 1997, Tanaka 2000, Tanaka 2006, Tanaka 2007, Bergenstof Nielsen 2000, Mihalcea 2001].

Hein *et al*. added clean metal impurities Ni, Al, Cu, Zn, Fe, Cr (99.999% and 99.99999%) to KOH solution (33 wt-% at 80 °C) and changes in the (100) plane and convex corner etching rate and surface roughness were reported [Hein 1997]. Fig 32 shows the changes in the anisotropy. Cu and Ni reduce anisotropy but their effect saturates fast. Al, Zn, Fe, Cr and Na increase anisotropy and their effect saturates more slowly than Cu and Ni.

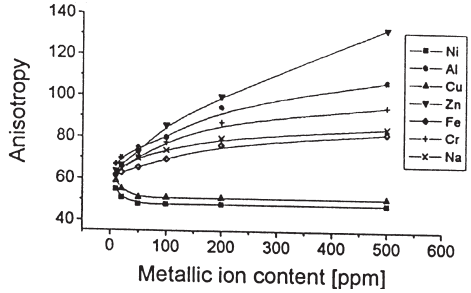


Fig 32. Anisotropy of silicon as function of the amount of metal impurities in KOH solution [Hein 1997].

The surface of the (100) plane that has been etched becomes more uneven as a function of the impurity content but the effect saturates in the area of 100–200 ppm. The etching plane of the convex corner changes and the surface quality becomes uneven as a function of the impurity concentration. The etching plane changes from about (411) plane (corresponding to an angle of 151°) to about (311) plane (corresponding to an angle of 143°).

Roughness of the etched surface increases rapidly as the impurity concentration increases. Hein *et al.* explained this phenomenon as adsorption of the metal ions to the silicon surface during the etching process. Based on the studies, the (111) plane roughness of the etched surface was identical to that of the (100) plane. In high sodium concentrations (>10 000 ppm) hillocks occurred in the etched surface of the (100) plane, and holes in the (111) plane [Hein 1997].

The effect of small amounts of impurities in KOH anisotropic etching was reported by Tanaka *et al*. [Tanaka 2000]. They investigated the etching characteristics of (110) plane surface in aqueous KOH solutions containing ppb-levels of Cu, Pb, Ag, Zn, Mg and Fe. They found that that a ppb-level of Cu roughens the silicon surface and that the etching rate is changed by ppb-level of Cu and Pb (Fig 33). The effects of Cu and Pb can be explained by the interaction between ions and hydrogen gas generated during etching based on the oxidation–reduction potential of Cu, Pb and H. The potential oxidation–reduction values of the impurities against normal hydrogen electrode (NHE) are shown in Fig 33. Cu or Pb in caustic solutions at high pH is indicated to become Cu ion (CuO_2^{-2}) or Pb ion ($HpbO_2^{-}$) and hydrogen gas is generated by the etching reaction (equation 17 and 18) in caustic solution.

$$\mathbf{Si + 2OH^- \rightarrow Si(OH)_4 + 4e^-} \quad (17)$$

$$\mathbf{2H_2O + 4e^- \rightarrow 4OH^- + 2H_2} \quad (18)$$

Cu metal particles deposit on the Si surface during etching because the oxidation–reduction potential of Cu (-0.40V) is higher than that of H (-0.85V). It is considered that Cu ion is reduced to Cu metal by hydrogen and Cu particles on the Si surface can act as an etching mask. On the other hand, as shown in Fig 33, because the oxidation–reduction potential value of Pb (-0.91V) is equivalent to that of H (-0.85V), it is assumed that the reaction of Pb reduction–ionization can oppose the etching reaction, thus the etching rate is changed. Because Pb reduction–ionization is in equilibrium, it is considered that Pb deposited on the Si surface is limited and does not affect the roughness of the surface.

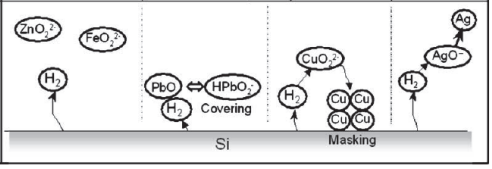
Impurity	Zn	Mg	Fe	Pb	H	Cu	Ag
Potential (V vs. NHE)	-1.45	-1.25	-1.05	-0.91	-0.85	-0.40	+0.25
Change in etch rate	No change			Lowering	—	Lowering	No change
Change in surface roughness	No change			No change	—	Roughening	No change
Behavior of ions during etching	Existing ions give no effect to reaction			The reaction of Pb reduction-ionization changes the etching reaction.		Cu metal particles are deposited on the Si surface and act as an etching mask	Ag metal particles reduced due to hydrogen in the solution give no effect to reaction
Model							

Fig 33. Model of behaviour of Cu, Pb, Ag, Zn, Mg and Fe impurities during anisotropic KOH etching (110 °C and 34 wt-% KOH) [Tanaka 2006].

The oxidation–reduction potential of Ag (+0.25V) is more positive than that of Cu (-0.40V) as shown in Fig 33. Because the potential of Ag is too high, an Ag ion reduces to an Ag metal particle directly in the solution due to the hydrogen gas produced during etching, and the effect of Ag does not appear on the etching properties. The potential for Zn (-1.45V), Mg (-1.25V) and Fe (-1.05V) ions is lower than that of hydrogen. As a result, these ions can exist in the solution and they are not changed, so the etching properties are not affected.

Etching rates of p-type Si (110) as a function of Cu concentration and Pb concentration (110 °C and 32 wt-% KOH) are shown in Figs 34a and 34b). Fig 34a shows the relation between etching rate and concentration of Cu. The etching rate decreased gradually above 100 ppb of Cu. The rate was 9 μm/min at 20 ppb but decreased to 7 μm/min at 1000 ppb. Fig 34b shows the relation between etching rate and concentration of Pb. For Pb concentrations less than 100 ppb, the etching rate decreased with increasing Pb content, but with Pb concentrations above 300 ppb the etching rate increased.

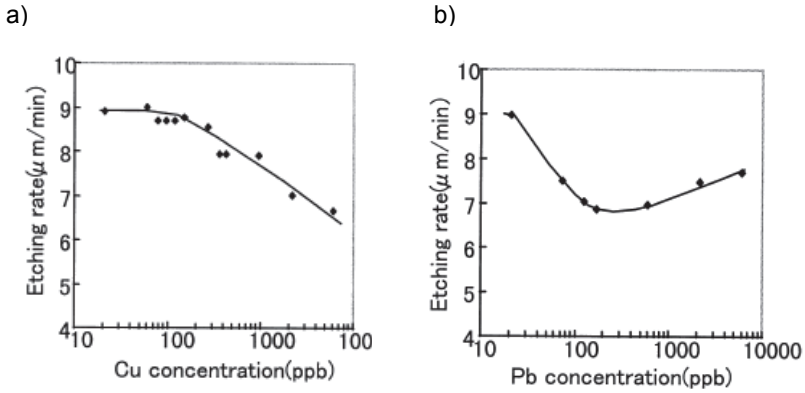


Fig 34. Etching rate of p-type Si (110) versus (a) concentration of Cu and versus (b) concentration of Pb (110 °C and 32 wt-% KOH) [Tanaka 2000].

The effect of Mg in KOH solution anisotropic wet etching of Si and the compensation for Cu impurity in KOH solution were investigated [Tanaka 2007]. This study found that the etch rate of the (100) and (110) planes decreased gradually above 10 ppm Mg concentration. It also found that anisotropy was the same with and without the addition of Mg and that over 10 ppm the addition of Mg did not affect the roughness of the etched surface. However, the roughening effect of ppb-level Cu could be controlled by the addition of Mg at ppm-level.

Deposition of inorganic (Fe_xO_y) particles in connection with the KOH etching of silicon membranes was reported by [Bergenstof Nielsen 2000]. The source of the particles reported was the KOH pills used for making the etching bath. When not removed, the particles caused etch pits on the silicon surface when further processed. The addition of Sb and As at millimol concentrations to a 40 wt-% KOH solution was studied [Mihalcea 2001]. They observed extremely smooth plane (100) surfaces with Rq roughness below 2 nm. The explanation was that the film of the elements Sb or As floats on the surface and changes the oxidation/dissolution behaviour of the silicon and finally leads to a mirror-like surface. The effects of Pb impurities on KOH etching are explored in chapter 6.3.

4.1.6 Dimensional control in anisotropic etching

The precision of the anisotropic etching is restricted by many factors. On the p-type wafer the under-etching is greater than that of the n-type wafer and the quality of the surface which has etched is worse on the p-type wafer than on the n-type wafer. Other factors which affect etching are the precision of the position of lithography and mask, (111) plane etching and the physical inaccuracies of the wafer.

The inaccuracy of the lithography and the inaccuracy of the position of the mask cause deviations in the desired figures. The figures, which are generally etched, are so large that the line width of the lithography is quite enough. A more important factor is the position of the mask, where inaccuracy causes the transforming of the desired figures in the etching. The (111) plane etches 80–120 times more slowly than other planes. During a long and deep etching the (111) plane has time to etch under the mask oxide because the etchant has the longest time (Fig 35) to take effect on it. The angle deviation ($\Delta\phi$) this is created from is:

$$\tan \Delta\phi = (1/3)^{½} * R_{111} / R_{100} \qquad (19)$$

If the relation of the etching rates is R_{111}/R_{100} = 1/100, then $\Delta\phi = 0.33°$. When a wafer is 500 µm thick, lateral deviation is 8 µm on both sides of the wafer. This deviation must be taken into consideration, for example, in making micro optical devices. This is also a geometrical study but in the real etching process the oxygen level and crystal defects of the wafer must be considered in a precise analysis, as shown in chapter 7.

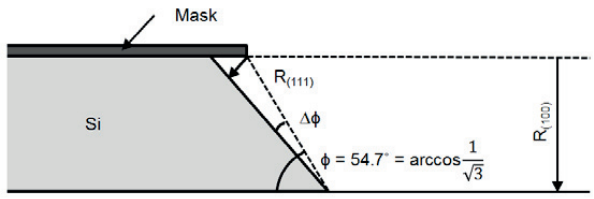


Fig 35. Etching of the (111) plane under mask oxide [redrawn from Lang 1996].

The physical inaccuracies of the wafer are; the taper of the wafer, in other words the wafer is not even, orientation mistake of the surface of the wafer, and orientation mistake of the identification level. Taper causes mistakes in the lithography, in other words, the desired holes do not reach correct sizes. This causes mistakes, for example, in the two-sided etching of the membrane where a faulty hole in the mask causes a membrane of a faulty size. In the case of the orientation mistake of the surface of the wafer, the levels are not parallel with the surface of the (100) wafer. This causes the right-angled etched figures to be wedge-shaped (Fig 36 a). In case of the orientation mistake of the identification level, the levels are not parallel with the identification level (110). This causes the broadening of right-angled figures and the change of the direction of figures from an original direction (Fig 36 b).

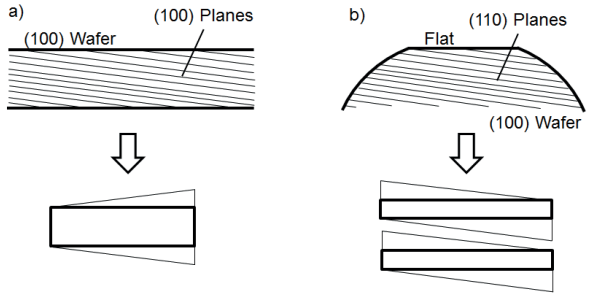


Fig 36. (a) Orientation error of the surface of the wafer makes a rectangular shape become tapered in anisotropic etching [adapted from Lang 1996]. (b) Orientation mistake of the flat surface causes a rectangular shape to become a parallelogram in anisotropic etching [redrawn from Lang 1996].

Wafer specifications today make it possible to define flat orientations within +/-0.2°, which is enough for most applications.

4.2 Hillocks

Hillocks are detected on the surface of etched silicon. All anisotropic etchants seem to produce hillocks. Hillocks are like small pyramid shapes and the sides of the pyramids follow precisely the crystal orientation of the wafer. Hillocks are usually reported as being pyramidal or near pyramidal protrusions from (100) surfaces, bounded by convex edges, and from (111) or "near-(111)" planes. The basic hillock morphology is depicted in Figs 37a and 37b. Fig. 37a shows an idealized pyramidal shape bounded by (111) planes. Tan [1994] reported in detail on hillocks created in KOH and found that they were bounded by sharply defined convex edges, and (567)-family planes, a few degrees off from (111) planes. These are represented by the “near-(111)” planes in Fig 37b. Beside these symmetrical hillocks there are also hillocks that are round in shape on the bottom. These kinds of hillock are supposed to be generated from gas bubbles.

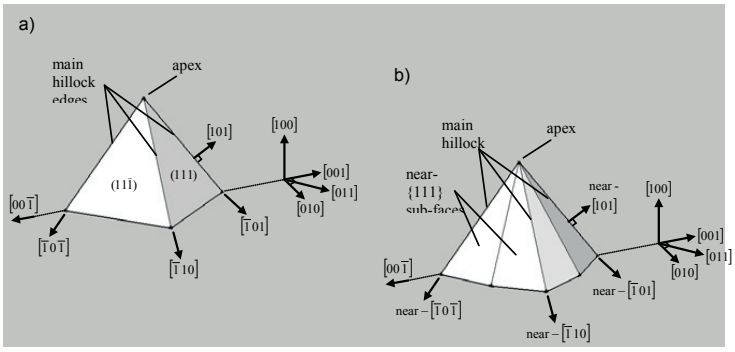


Fig 37. Schematic figures of hillocks. (a) a hillock having (111) plane side walls and (b) a hillock whose side walls are close to the (111) plane, for example, (567) plane [redrawn from Landsberger 1996].

The reasons for the formation of hillocks are reported as: micromasking of oxygen precipitates [Matsuoka 1992, Bhatnagar 1993], incomplete dissolution of reaction products remaining on the etched surface [Tan 1994, Landsberger 1996, Zubel 1998, Elwnespoek 1998, Khizhnyak 2006, Zubel 2008], hydrogen bubbles created in the

dissolution process [Schröder 1999, Yang C-R 2005, Haiss 2006], local stabilization of distributed apex atoms by (metal) impurities from solution [Gosalvez 2003], surface active substance, temperature, etchant concentration, etch agitation and the presence of gases [King 1991, Vazsonyi 1998, Suárez 2008, Mirabella 2008]. Last but not least, the study by Singh *et al.* [Singh 2001] indicates that the growth of pyramids begins at preferred sites which may arise due to crystalline defects or wetting.

Compared with no agitation, magnetic stirring, and ultrasonic agitation, the etchant modified by the addition of anionic surfactant was studied to evaluate the etching properties of (100) silicon plane in 30 wt-% KOH [Yang C-R 2005 1]. The experimental results indicate the following conclusions:

1. Ultrasonic agitation is an efficient technique to achieve higher etching rate and smoother etched surface. Surface roughness below 15 nm and an etching rate above 1.2 µm/min can be achieved.
2. Surface roughness of 7.5 nm can be achieved in KOH with surfactant at 100 °C. That is about eight times better than that using the pure KOH solution without agitation.
3. An etching rate of 4.9 µm/min can be achieved in KOH with surfactant at 100 °C. That is 1.44 times better than that in the pure KOH solution with ultrasonic agitation.
4. The change in anisotropy is not obvious in KOH solution with surfactant added.
4. The etching properties are promoted more efficiently in the KOH solution with anionic surfactant-added than by using ultrasonic agitation.
5. The roughness of the etched surface reaches optical quality when using the anionic surfactant.

4.3 Etch pits

A typical overview of the (111) plane wafer after KOH etching is shown in Fig 38. Very large eccentrical etch pits cover the surface. Steps are generated in the centre of the pit and move outwards. In this movement, steps bunch and form large macrosteps, possibly due to impurities adsorbed onto the surface. Near the edge of the pit, shell-like ridges have formed perpendicularly in the step direction. The eccentricity of the

pits is due to the fact that the wafer surface is not exactly aligned to the (111) crystal plane. The pits have several types of centres. Pits are visible with a pointy centre, with a line centre, with a double centre and without a centre, as indicated in Fig 38. The pits without a centre have a fairly flat bottom. Larger and smaller pits appear on the surface although the larger ones seem to overgrow the smaller ones. The larger pits are up to several micrometres deep.

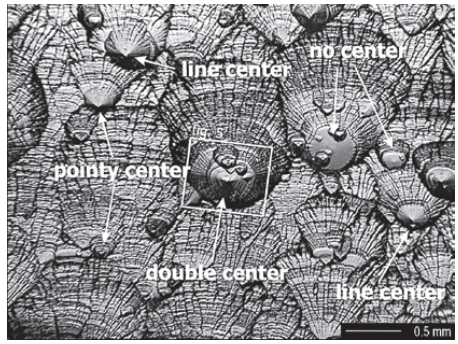


Fig 38. Typical overviews of the (111) plane wafer with etch pits after KOH etching. [Nijdam 2000].

The nature of etch pits that arise during anisotropic etching in KOH on (111) wafer surfaces was studied by Nijdam *et al*. [Nijdam 1999, Njidam 2000]. They found that bulk stacking faults in the crystal lattice give rise to deep etching pits. These dislocations give rise to locally increased mechanical stress on the crystal lattice. This area is etched slightly faster by KOH than the surrounding stress-free area, thus generating steps and pits. Since dissolved oxygen is causing the dislocations, wafers with low oxygen content will lead to flatter (111) plane wafer surfaces. They also found that other dislocations, of which the nature is still unclear, do not give rise to etching pits.

A similar study on crystal plane etching has been carried out for (100) wafers [Hölke 1999]. It was found that oxygen precipitates affect strongly rhe (110):(111) selectivity, and reduce the available aspect ratios. The proposed remedy was annealing at 1300 ^{o}C, which dissolves oxygen precipitates, and results in 230:1 (100):(111) etch rate ratio in KOH. This approach, however, is not generally applicable because 1300 $^{\circ}$C annealing requires special furnace hardware. At least, it was not available to us.

The fact that the depressions on (100) planes are spherical seems to imply that the (100) plane step velocity is isotropic [van Veenendaal 2001 1, van Veenendaal 2001 2]. Monte Carlo simulations have clearly shown that for a surface that is almost kinetically roughened, the step velocity is isotropic. Haimi and Lindroos [Haimi 2003] studied the evolution of roughness and concluded that crystal defects could act as velocity sources in etching the (100) silicon surface.

Oxygen concentration in silicon has been shown to correlate with increased etch rate of the (111) plane and, consequently, larger mask undercut [Kwa 1995, Mervelle 1997, Nijdam 1999, Hölke 1999, Njidam 2000, Müller 2000, Hein 2000, van Veenendaal 2001 1, van Veenendaal 2001 2, Haimi 2003]. This has been explained by stresses owing to oxygen precipitates. It has been found that bulk-stacking faults in the crystal lattice give rise to deep etching artefacts. These dislocations give rise to locally increased mechanical stress in the crystal lattice. The stressed area is etched slightly faster than the surrounding stress-free area [Nijdam 1999, Njidam 2000]. The same mechanism also explains the generation of steps and artefacts, leading to roughening of the (111) walls. Oxygen precipitates are problematic because their formation is an interplay between the initial oxygen concentration of the wafer and the subsequent thermal treatments. Since dissolved oxygen is causing the dislocations, float zone (FZ) wafers with low oxygen content were found to lead to smoother (111) wafer surfaces [Nijdam 1999, Njidam 2000]. The effects of oxygen level on KOH etching are explored in chapter 7.1.

5. Test structures and measurement tools

5.1 Etch test structures

Author's etch test structures are made on 'short loop' wafers which are faster to produce than true device structures. Besides, when etch test structures are standardized, they can show more quickly if something is changed in the process because they are simpler and easier to study than true devices. As to the properties of KOH, the temperature of the etchant, the concentration, the flow, the amount of the dissolved silicon and the dissolved impurities affect the etching of the silicon. As to the properties of the wafer, the amount of oxygen, the resistivity, the crystal defects and TTV affects etching. Furthermore, several external factors which have not previously been studied affect the etching process. These external factors are, for example, the force of the lighting which affects the electric properties of the silicon, external temperature and moisture and the pre-processing of the wafers and etchant. The effect of these external variables can only be standardized by performing all the tests equally and in the same conditions.

When characterizing anisotropy, the etching rate of the different crystal planes is studied. This can be studied with figures which appear radially on the surface of the wafer [Zielke 1995]. In this case, the direction of one radial figure will correspond in the direction of certain planes according to a stereographic projection (Fig 39). The dots in the projection correspond to the different crystal planes, and the directions which correspond to them are obtained from the margins of the projection.

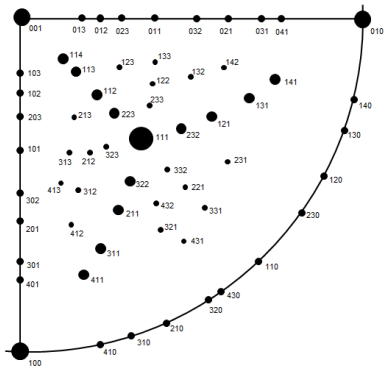


Fig 39. Part of the stereographic projection of the plane (001).

The wagon-wheel figure is given as an example of the radial figures which has been made long and very narrow openings to the mask in the form of a circle (Fig 40a).

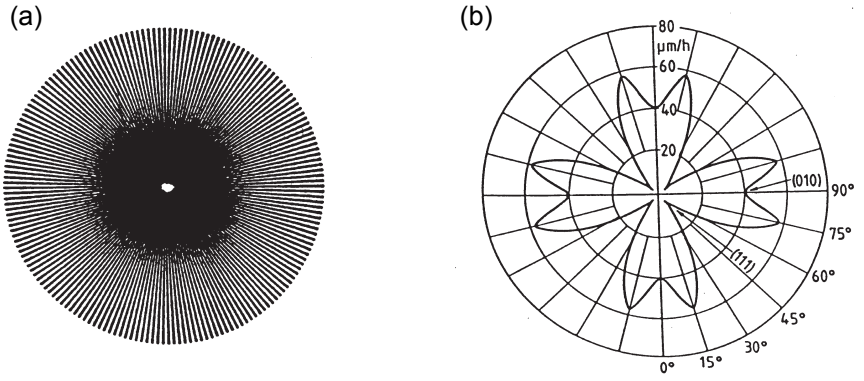


Fig 40. (a) Wagon-wheel figure: a test figure for determination of anisotropy [redrawn from Seidel 1990 1].
(b) wafer-wagon wheel figure or 'flower figure' etched on (100) plane wafer with the etching rates of the different planes (temperature 78 °C and concentration of KOH 50 wt-%) [Seidel 1990 1].

When the wagon wheel (Fig 40 a) is etched by KOH, under-etching will occur and result in a figure that is shown in Fig 40b. The length of the ray under-etched at a certain corner is directly proportional to the etching rate of the crystallographic plane, which corresponds to this corner. Furthermore, the four-fold symmetry of the (100) wafer can be seen from the 'flower figure'. In Fig 40b, it can be noted that the under-etching of the (111) plane (at 45° corners) is nearly zero. The etching is rapid on the (100) plane (0 and 90 at the corners). However, the maximum etching rate is not on the (100) plane but on both its sides, this means that in silicon there are planes that etch faster than the (100) plane.

Other methods for measurement of anisotropy include the etching of single crystal spheres and the etching of sphere-shaped holes on the wafer. In the former, spheres, as round as possible, are etched in KOH, and the surface of the spheres is etched to a polyhedron. The planes that etch fastest form the surfaces of the polyhedron and

the planes with slower etch rate disappear and form the corners of the polyhedron. In the etching of sphere-shaped holes, the sphere surfaces will disappear when the planes that etch fastest etch, and planes with slower etching rates form new walls to the hole, as shown in Figs 41a and 41b. The results of the etching of both spheres and sphere-shaped holes are measured with profilometry [Hesketh 1993, Ju 1992].

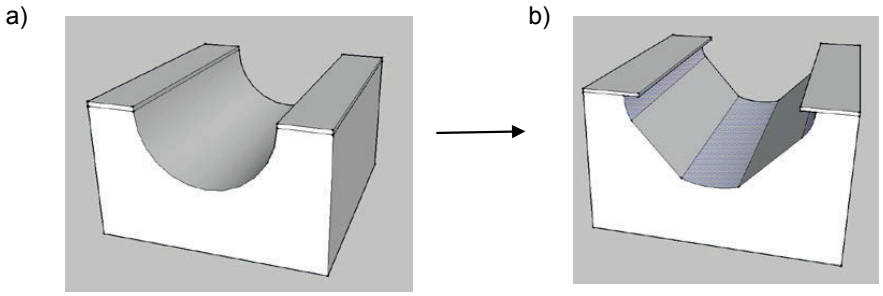


Fig 41. (a) Cylinder-shaped hole. (b) The faster etching planes (the violet areas) and the planes that etch more slowly form the walls of the hole [adapted from Elwenspoek 1994]

5.2 Convex corner compensation

Direction <110> rectangles as corner compensation figures were proposed in [Bao 1993]. Their <110> direction rectangles were thicker than the rectangles proposed by Offereins, Kühl and Sandmaier [Offereins 1991]. Furthermore, rectangles can be one or more 90° angles to control the etching front and to reduce the space needed by the figure [Bao 1993]. The simplest form of the figure, which gives the best etching result, is an L shape having one 90° angle (Fig 42). The figure was dimensioned according to formula (20) [Bao 1993] using the fastest etching plane, the (411) plane.

$$L = L_{eff} - (B * (\tan 30.96)^{-1}) \qquad (20)$$

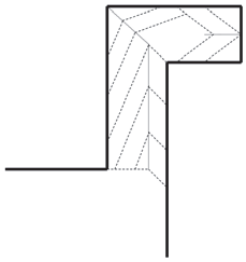


Fig 42. <110> direction corner compensation figure, which has the form of L and its etching behaviour.

The etching rate of the (110) plane is 2.7 times quicker than that of the (100) plane, according to [Offereins 1991]. This means that the effective length of the figure (L_{eff}) is 2.7 times the vertical etching depth (d). When the last etched right-angled triangle (B times $(\tan 30.96)^{-1}$) is reduced from the effective length of the figure (L_{eff}), the length (L) is obtained.

Perfect and sharp free end corners of silicon cantilever structures have been achieved by KOH anisotropic etching of silicon [Biswas 2006]. Among various corner compensation schemes it was noted that sharp right-angled corners with no deformation may be obtained by using the corner compensation layout of adding two rectangular blocks placed perpendicular with respect to each other at the free end corners. Based on the experimental results, an empirical relation was derived to achieve complete corner protection during anisotropic etching of silicon. The exact dimensions of the compensation patterns may be calculated using the relation for a desired etch depth of a cantilever structure with given length and width. Fig 43 shows a 3D schematic view of the corner compensation layout.

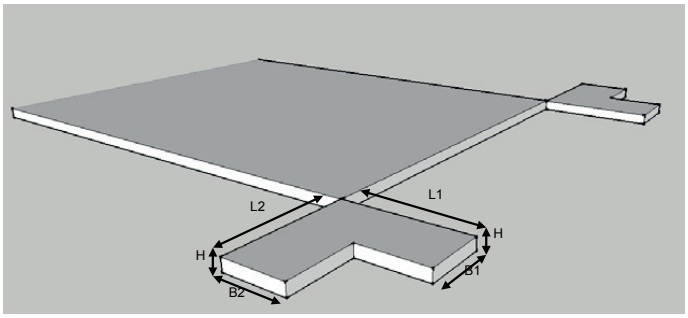


Fig 43. 3D schematic view of the corner compensation layout, which yields the most desired free end corners [redrawn from Biswas 2006].

The empirical relations obtained from the experimental data are as follows:

$$L1 = L2 = 2.86*H \quad (21)$$

$$B1 = 2.14*H \quad (22)$$

$$B2 = 1.43*H \quad (23)$$

Where H is the total etch depth up to which corner protection is required. L1 and L2 and B1 and B2 are the length and breadth of rectangular compensation blocks oriented along the length and width of the cantilever beam, respectively. The above relations are true for both n-type and p-type silicon substrates.

The above is only geometry but in real cases the wafer properties and surface finish affect the corner compensation. For example, in Fig 44, the corner compensation structure etched very differently as a function of different surface finish. This phenomenon is explained in chapter 7.2. In Fig 44a, the under-etching of the (111) plane is minimal (a fine ground wafer with 60s KOH etching), and in Fig 44b, the under-etching of the (111) plane is maximal (a fine ground wafer without KOH etching). In Fig 44c (a reference polished wafer), the under-etching of the (111) plane is somewhere between Figs 44a and 44b. Pillars etched in wafers were photographed

with an optical microscope, and the mask under-etching of the (111) plane was measured from the pictures by using Matrox pattern recognition software.

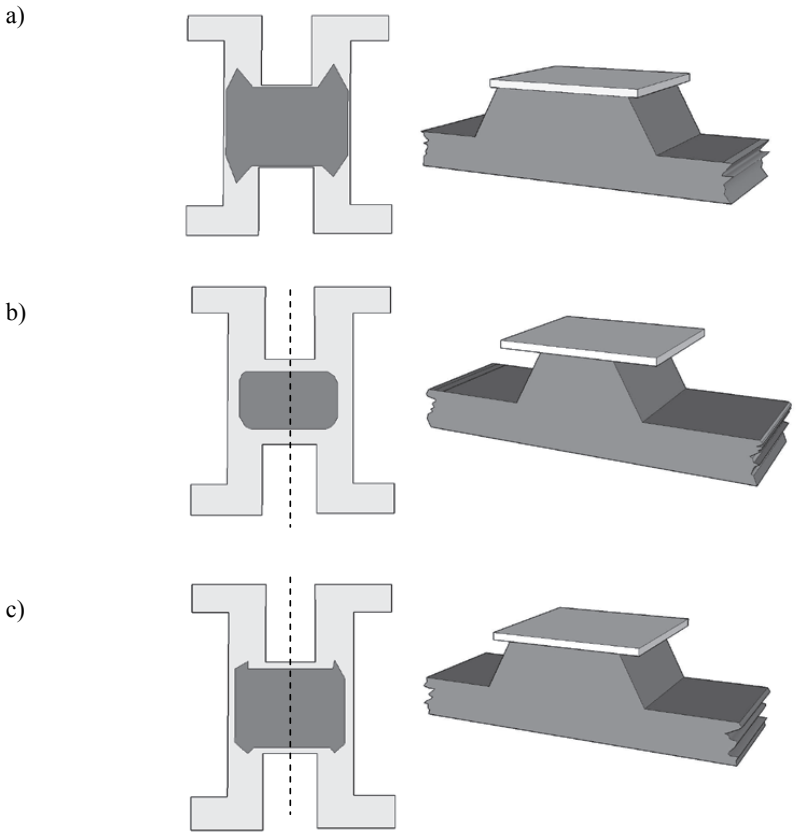


Fig 44. Author corner compensation design and the resulting mask undercut from chapter 7.2: (a) a fine ground wafer with 60s KOH etching, (b) a fine ground wafer without KOH etching and (c) reference polished wafer. The 3D drawing shows a cut along the dotted line.

5.3 Accelerometer as a test structure

A capacitive accelerometer with KOH etched seismic mass was used as a test device (Fig 45). The seismic mass is fabricated in the middle wafer by a double-sided, nested mask etching process.

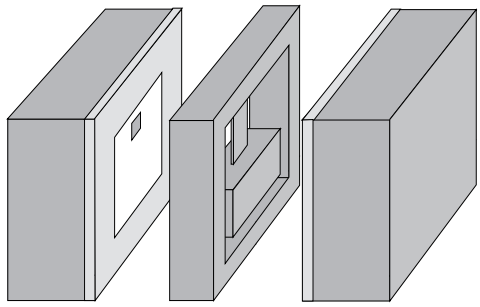


Fig 45. Schematic figure of a bulk micromachined accelerometer: anisotropic KOH wet etching defines the single crystalline silicon seismic mass and spring beam in the middle wafer

P+ (100) CZ silicon wafers of 150 mm diameter and thickness of 300 µm and 380 µm were used. Due to their symmetric structure, double-side polished wafers (DSP) were employed. The resistivity spec of the wafers was 0.020–0.025 Ohm-cm. Wafers were wet oxidized at 1050 °C and the thickness of the grown mask oxide was measured by ellipsometry or reflectometry to be approximately 0.8 µm. A 0.2 µm-thick LPCVD silicon nitride was deposited at 770 °C on top of the oxide layer for double layer masking (peeling masks). Peeling masks were patterned on both sides of the wafer. Nitride was etched in SF_6/O_2 plasma using the LAM Research Inc. LAM 590 etching tool, while oxide was wet etched with BHF using a Semitool SAT3061T spray tool.

The wafers were cleaned in SC1 (ammonia-peroxide solution) and rinsed in DI water before KOH etching. Etching solutions were mixed from Honeywell PURNAL quality KOH and DI water. The first short KOH etching defines the area to be released in the end. Etching conditions are KOH temperature of 65 °C and concentration 20 wt-%. The exposed oxide mask on top of the beam is then etched away in BHF, and the second KOH etching step uses a nitride mask to etch through the wafer in the rim area and to define the beam area. These etches are done batch wise in a turbulent flow dynamic etching bath. In the turbulent flow bath cassette, a rotation speed of 27 rpm and rotation direction change every 15 min were used. The final beam thinning etch (75 °C, concentration 40 wt-%, a static etching bath) was done one wafer at a

time, with 18 μm as the target thickness for the beam. The resulting seismic masses and beams are shown in Fig 46.

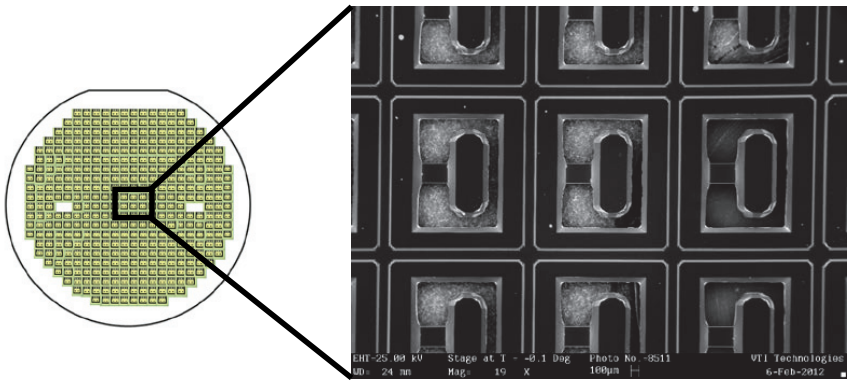


Fig 46. SEM picture of successfully etched anisotropic KOH wet etched single crystalline silicon seismic masses and spring beams in the wafer.

A spring beam made as single crystalline silicon has an ideal elasticity [Cardinale 1996, Sankar 2007, Othman 2009]. The deflection δ of a spring beam under load, *F*, is simply described using elasticity theory for small beam deflections *(δ<< L)*:

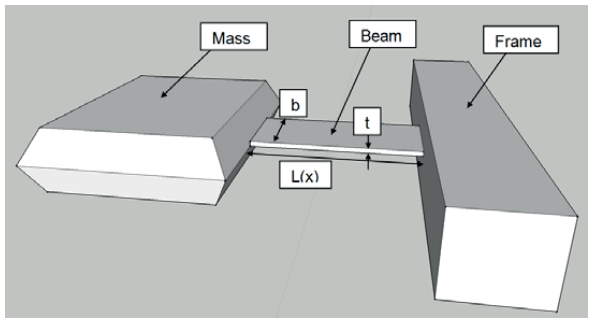
$$\delta = \frac{FL^3}{3YI} \tag{24}$$

Where *L* is the beam's effective length (i.e., the distance from the fixed end of the beam to the point of the applied load), $Y = E\sim (1 - \nu^2)$ is the plate modulus of the spring with *E* being the Young's modulus (for silicon E = 167Gpa) and ν being Poisson's ratio, and *I* is the centroid of revolution. Figs 47a and 47b illustrate the beam dimensions and load-deflection variables. For a prismatic spring beam with rectangular cross-section, $I = bt^3/12$ where *b* and *t* are the width and thickness of the beam, respectively. Equation (24) then becomes:

$$\delta = \frac{4FL^3}{Ybt^3} \tag{25}$$

Equation (25) shows that deflection is highly sensitive to the effective length and thickness.

a)



b)

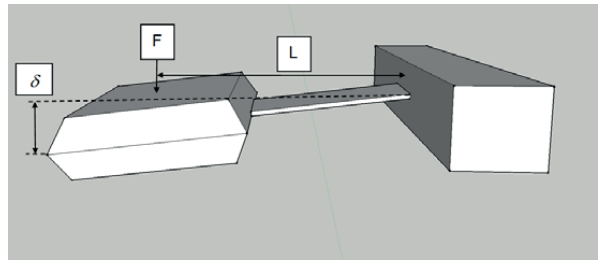


Fig 47. (a) Schematic representations of the accelerometer seismic mass and spring beam dimensions
(b) Schematic representations of the accelerometer seismic mass and spring beam load-deflection variables

The seismic mass moment of inertia or the angular mass (N/m) is a measure of an object's resistance to changes in its rotation rate. The moment of inertia for seismic mass is:

$$k1 = E\frac{I}{12l^3} \tag{26}$$

In equation (26) for one spring beam seismic mass the $I = (bt^3/12)k_{geom}$ where b and t are the width and thickness of the beam and $k_{geom} = 1.072$ (empirical coefficient). For tow spring beam seismic mass the $I = 2(bt^3/12)k_{geom}$.

The main problems in the deepest and longest etching processes are variation in etch rates across the wafer and wafer-to-wafer. Small variations in the etch rate of (100) plane result in variation of beam thickness which can be considerable due to

cubic dependence (Equation 26). From the accelerometer point of view variation in the beam thickness means inaccuracy or nonlinearity to acceleration determination. Fig 48 shows nonlinearity measurement results of analog SCA1020 sensor component. Fifteen randomly selected components were measured in a centrifuge from -3g to +3g at different temperatures from -40 °C up to 125°. Measurement results of different components are shown in different coloured curves and the results are fitted to 1.7g as zero volt. The nonlinearity spec of the component is +/-45mg between -1.7g and +1.7g in a temperature range of -40 °C to +125 °C.

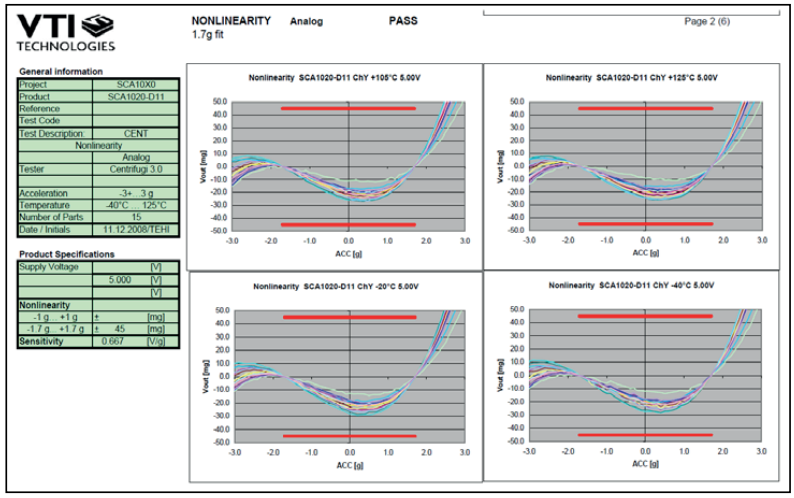


Fig 48. Centrifuge nonlinearity measurement results of analog 2g SCA1020 sensor component. Measurements show the seismic mass move (Vout change) from -3g to +3g. To pass result the Vout (mg) should be in the specification (+/-45mg) in the whole measurement area (-1.7g to +1.7g) and at all temperatures.

As Fig 48 shows, the components results are quite individual and some components are closer to the spec limit than others. Fig 48 shows that components whose Vout is closer to the spec limit in -1.7g–+1.7g are also more sensitive to g-value change. The sensing element moving mass sensitivity to g-value is illustrated in Fig 49. When two different elements with different beam dimensions see the same g-value, the mass with thinner, narrower or longer beam (Fig 49a) will move more than the mass with

thicker, wider or shorter beam (Fig 49b) and cause more nonlinearity to the component.

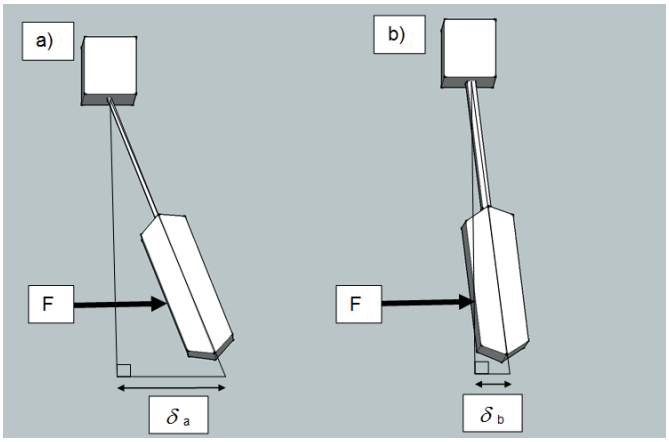


Fig 49. Schematic illustrations of two different elements with different beam dimensions show the same g-value. The mass with thinner, narrower or longer beam (a) will move more than the mass with thicker, wider or shorter beam (b) and cause more nonlinearity to the component.

5.4 Measurement tools

5.4.1 Beam dimension measurements

The beam dimensions were measured with the non-contact laser profilometer measurement tool from UBM/Keyence or FRT Microprof 200 TTV in five or nine different locations on a wafer (Fig 50). The Keyence LT sensor uses the confocal principle of dynamic focusing to reduce measurement errors. A laser beam with a spot size of 2 µm is used to scan the surface. The FRT Microprof 200 TTV tool is a metrology system for measuring the absolute thickness variation of wafer with maximum TTV resolution <10 nm. A laser beam with a spot size of 2 µm was used to scan the surface.

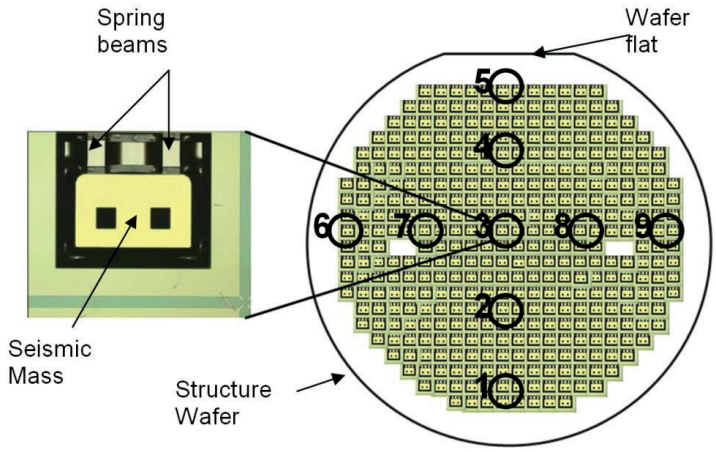


Fig 50. Anisotropically etched seismic masses and two spring beams of an accelerometer and laser profilometer measurement sites (numbered black circles) across the wafer.

5.4.2 Roughness measurements

Surface roughness was measured by either Micromap 560 optical profilometer or NT-MDT NTegra, Atomic Force Microscope (AFM). Micromap 560 is an interference microscope that enables contactless measurement of surface micro-geometry in 3D. The height resolution of the tool is approximately 1 nm and the size of the surface measurement area was either 153 x 119 µm or 754 x 588 µm. The number of measurement pixels was 304 x 228. NT-MDT NTegra is an AFM tool. AFM is a very high-resolution type of scanning probe microscopy, with demonstrated resolution in the order of fractions of nanometres, more than 1000 times better than the optical diffraction limit. The AFM measurements were made in Aalto University facilities in Micronova in Espoo, Finland. Measurements were made in tapping mode with scanning head setup. Measurement areas were 20 x 20 µm and 10 x 10 µm. Measurement analysis and surface figures were made with the Nova 1.0.26.1443 AFM analysis software tool.

5.4.3 Microscopy

Direction <110> and etching and angle of fastest etching plane projection were measured from wafers etched with a special anisotropy figure. The figure was photographed with optical microscope, and the under SiO_2 mask etched direction of <110> etching length and the projection angle of the plane that etched fastest were measured from the picture by using figure treatment Matrox software. Fig. 51 shows the measured dimensions of the etched figure.

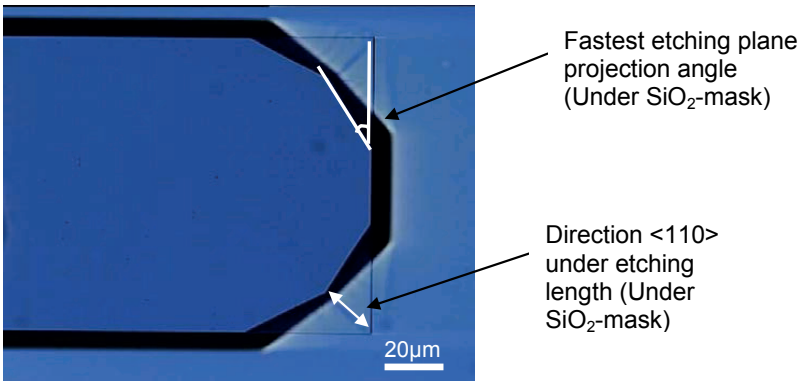


Fig 51. Anisotropically etched figure and the measured dimensions: projection angle of fastest etching plane and direction <110> under etching length.

A schematic of the test structure figure with corner compensation structures is shown in Fig 52, as well as the 3D image of an ideally etched test pillar structure.

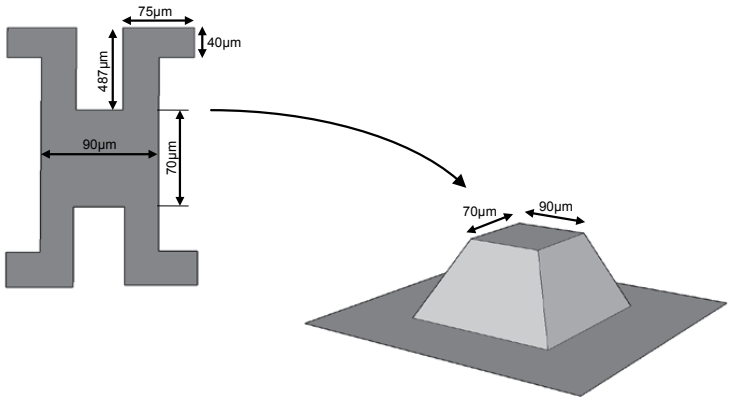


Fig 52. Corner compensated silicon test structure after ideal etching.

6. Silicon etch rate and uniformity

The present chapter introduces the first three different phenomena that influence the anisotropic etching of silicon in aqueous KOH solution. They are:

1) Etching temperature and KOH concentration - chapter 6.1
2) Etching equipment and agitation - chapter 6.2
3) Impurities in etching solution - chapter 6.3

6.1 The etch rate variations of p+ silicon wafers

In the present study, the etching behaviour of highly boron doped (20–25m Ω-cm) silicon wafers in aqueous KOH solutions was investigated. Differences in etch rates between the (100) and other crystal planes are utilized in the processes. However, in the literature different results are reported for the positions of maximum etch rates as a function of KOH concentration. The position of maximum etch rate of the (100) crystal plane is reported to be located between 10 and 15 wt-% KOH [Price 1973], or near 20 wt-% KOH [Seidel 1990 1]. Furthermore, different planes are reported to have the fastest etching rate; (212) [Wu 1989], (130) [Puers 1990], (411) [Mayer 1990] and (110), (320) and (540) [Sato 1997], respectively.

Wafers used in experiments were double-side polished P+(100) CZ wafers. These wafers were oxidized by wet oxidation at 1050 °C and the thickness of the grown oxide was approximately 1.5 µm. A test mask pattern of rectangular windows with subdivision into angles of 3° on the outer circle of the wafer was lithographically transferred to the oxidized wafers (Fig 53).

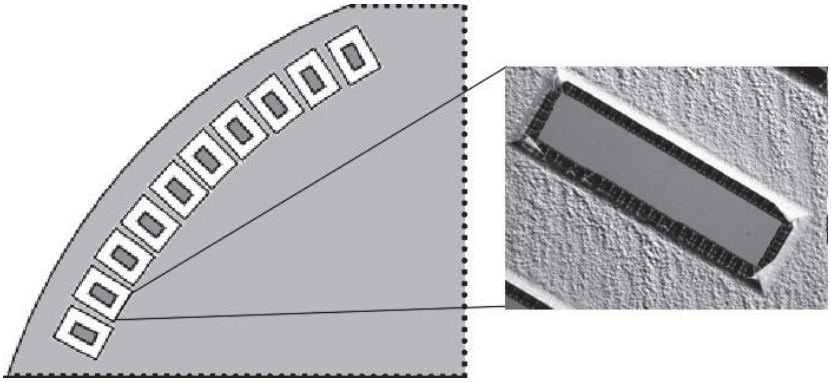


Fig 53. A test mask pattern of rectangular windows with subdivision into angles of 3° on outer circle of the wafer. An optical microscope picture of under-etched rectangular window in the enlarged picture.

Before etching, the wafers were cleaned by the SC1 cleaning process, and after etching, the wafers were rinsed in DI water. The etching solutions were mixed from Merck's high purity, p.a. quality KOH pellets and DI water. The experimental temperatures of KOH solutions were 65, 70, and 75 °C. In the 65 and 75 °C experiments, the concentrations used were 10, 20, 30 and 40 wt-% KOH, and in the 70°C experiments, the concentrations used were 5, 15, 25 and 35 wt-% KOH. In each experiment, ten wafers were etched to a depth of approximately 70 μm. From the industrial point of view, faster etching condition is recommended aiming at shorter etching time. [Tanaka 2004] studied new working conditions typically at 130 °C with 45–47 wt-% KOH concentrations of KOH. The surface roughness and process stability seem to be in control in Tanaka high temperature process. However, the lifetime of the bath in long etchings causes changes in planes (100) and (110) etching rates as a function of KOH concentration. Furthermore, the selectivity against oxide mask in such high temperature etching is problematic. In this thesis, such high temperatures or concentrations are not used because in the accelerometer beam etching, the etching accuracy and uniformity are much more important than the etching time. Besides, two different mask oxide thicknesses are used whose selectivity against etchant must be high enough so that the masks do not fail during etching.

The etch rate of the (100) crystal plane and the etch rates of fastest etch plane projections were measured as function of process conditions. The under-etch rate of window in angle 45° corresponds to the etch rate of (100) crystal plane. The under-etch rate of window in angle 27° is assumed to correspond to the etch rate of (31X) crystal plane projection in angle 26.57° (where X can be 1,2,3…). The under-etch rate of window in angle 30° is assumed to correspond to the etch rate of (41X) crystal plane projection in angle 30.96° (where X can be 1, 2, 3…). Etch rates were calculated from averages of under-etch rates from several places and both sides of the wafers. Under-etch rates were measured with optical microscopy.

6.1.1 Etch rate results and model

The measured and the modelled etch rates are presented as a function of KOH concentration in Fig 54. The figure shows the relationship between etch rates, KOH concentrations and KOH temperatures. The increase in the KOH temperature is noted to increase all three etch rates but the shape of the curves seems to remain similar. However, the increase in the KOH concentration reveals a maximum in the etch rates. The modelled graphs in Fig 54 show that the maximum etch rate of (31X) crystal plane projection is located near 7 wt-% KOH and the maximum etch rate of (41X) crystal plane projection is located near 10 wt-% KOH. The maximum etch rate of (100) crystal plane is located near 12 wt-% KOH.

The etch rate of the (31X) crystal plane projection decreases as a function of increasing KOH concentration more rapidly than the etch rate of the (41X) crystal plane projection, as is also shown in Fig 54. It means that the etch rates cross each other and the angle of the fastest etch plane projection change. In lower concentrations, the fastest etch plane projection is (31X) crystal plane projection, and in higher concentrations, the fastest etch plane projection is (41X) crystal plane projection. The place of the fastest etch plane change varies as a function of KOH temperature. The place change of the fastest etch plane projection occurs in approximately 15 wt-% KOH at 75 °C and approximately in 20 wt-% KOH at 70 °C. In KOH at a temperature of 65 °C the place change takes place in about 30 wt-% KOH.

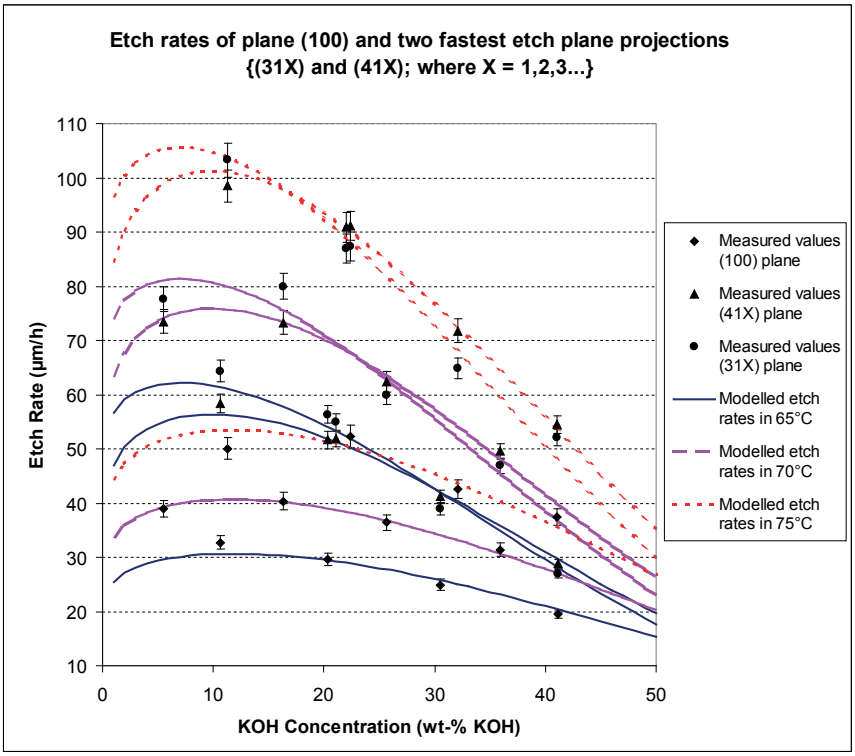


Fig 54. Etch rates of plane (100) and two fastest etch plane projections (31X) and (41X) (where X = 1,2,3…) as a function of KOH concentration. Compare Fig 10.

The etch rates of different etch planes were fitted to a similar empirical equation (27) presented by Seidel *et al*. [Seidel 1990 1]. In the equation (27), R is the etch rate and E is the activation energy:

$$R = k_0 [H_2O]^X [KOH]^Y e^{(-E / kT)} \quad (27)$$

The coefficients in equation (27) were determined by linear regression analysis from the measured values. The values of the coefficients are presented in Table 3.

Table 3. Coefficients for different etch planes in equation (27).

	k_0 (μm/h)	X	Y	E (eV)
Crystal plane (100)	9243	3.40	0.11	0.56
Plane projection (41X)	134	4.87	0.12	0.59
Plane projection (31X)	4	5.30	0.08	0.54

6.1.2 Higher index plane etch rates

The values of the coefficients in equation (27) are k_0 = 2480, X = 4, Y = 0.25 and E = 0.595 [Seidel 1990 1]. The maximum etch rate of (100) crystal plane was near 20 wt-% of KOH following from the coefficients X and Y in the equation. Based on Palik's suggestions [Palik 1983], Seidel *et al.* [Seidel 1990 1] assume that the following reactions take place at the (100) plane surface. The first step is a reaction of a silicon atom, attached with two bonds to the solid, with two OH^- ions from the solution. This reaction delivers two electrons to the solid. The electrons are thought to stay localized near the surface of silicon due to downward bending of energy bands. The second step is an ionization of the $Si(OH)_2$ complex, which delivers two further electrons to the surface region of the solid. In the third step, positively charged $Si(OH)_2^{++}$ complex reacts with two OH^- ions from the solution resulting in a soluble $Si(OH)_4$ molecule. Finally, the four electrons on the silicon surface react with water, producing OH^- ions and hydrogen. As a conclusion, Seidel *et al.* [Seidel 1990 1] assume that the dissolution of one silicon atom involves four electrons and four water molecules. This is supported by experimentally observed correlation between the fourth power of the water concentration and the etch rate of the (100) crystal plane.

The results of the study do not show the fourth power correlation between the water concentration and the etch rate of the (100) crystal plane. However, if the above described reaction sequences are used, the coefficients X in the table will represent the number of electrons and water molecules involved in each of the etching reactions. In the case of the fastest etching planes, the values of the coefficients X exceed 4, whereas X for (100) crystal plane is under 4. This is an indication that the production and the consumption of electrons and OH^- ions do not necessarily take place at the same type of crystallographic site.

The results of the present study indicate that there are differences between the etching reactions of different etch planes. The difference may be connected to transferring electrons. This could explain why the different etch planes have the position of maximum etch rates as a function of KOH concentration in different places. Furthermore, this could also explain why the fastest etching planes are sensitive to experimental conditions.

6.2 Rotational vs. laminar KOH etch bath

The author had at his disposal two different etch bath setups, hence the uniformity of silicon etching in rotational and flow-through etch baths was studied. The supply of reactants and the removal of reaction products are strongly affected by flow patterns in the bath, and subsequently, large differences are observed in uniformity of etching. The test structures for these measurements are accelerometer beams, etched on to double-side polished (DSP) wafers. Variation of beam thickness is measured across the wafer, within batch (wafer-to-wafer) and batch-to-batch. A thorough statistical analysis includes thousands of etched wafers. The main problems in the deepest and longest etching processes are variations in the etch rate across the wafer and wafer-to-wafer. Small variations in the rate of (100) plane result in variation in beam thickness that can be considerable due to cubic dependence (equation 28). From the accelerometer point of view the beam thickness variation means inaccuracy to acceleration determination.

For etching of the (100) plane beam DSP wafers, double sided lithography and masking must be employed. Etching is carried out in multiple steps with the deepest and longest etching around 150 µm deep and lasting about 5 hours. The etching bath temperature and concentration are accurately controlled to achieve the required beam thickness control.

The wafers used were DSP 150 mm diameter P+(100) CZ silicon wafers, with total thickness variation (max–min) below 1 µm. Wafers were wet oxidized at 1050 °C and the thickness was approximately 0.8 µm. On top of the thermal oxide layer, a 0.2 µm

thick PECVD silicon nitride was deposited for double layer masking. Four lithography and four etching steps (two on both sides of the wafer) were used to create the mask patterns for the spring beams and seismic masses. The nitride was etched with LAM Research Inc. LAM 590 plasma etching tool with SF_6/O_2 plasma, and the oxide was etched in Semitool SAT3061T spray etching tool with BHF.

Before KOH etching, the wafers were cleaned by the SC1 cleaning process, and after etching, the wafers were rinsed in DI water. The etching solutions were mixed from Honeywell PURNAL quality KOH and DI water. The KOH solutions were at a temperature of 65 °C and concentration of 20 wt-%. These parameters were chosen because of the high anisotropy etch rate crystal plane and the low etch rate of the mask. In each run, a full cassette of 25 wafers was etched to approximately 150 μm depth from both sides simultaneously. The resulting seismic mass and beams are shown in Fig 50.

A so-called dynamic etching bath is used: KOH is agitated to flow between the wafers to ensure uniform etching. Two basic types of dynamic etching baths were tested. In flow-through design (Fig 55a), the wafer cassette and the wafers are static and KOH solution is pumped from the bottom of bath upwards through the cassette and in between the wafers. In the rotational design (Fig 55b), the whole cassette and the wafers in it are rotated in the KOH solution.

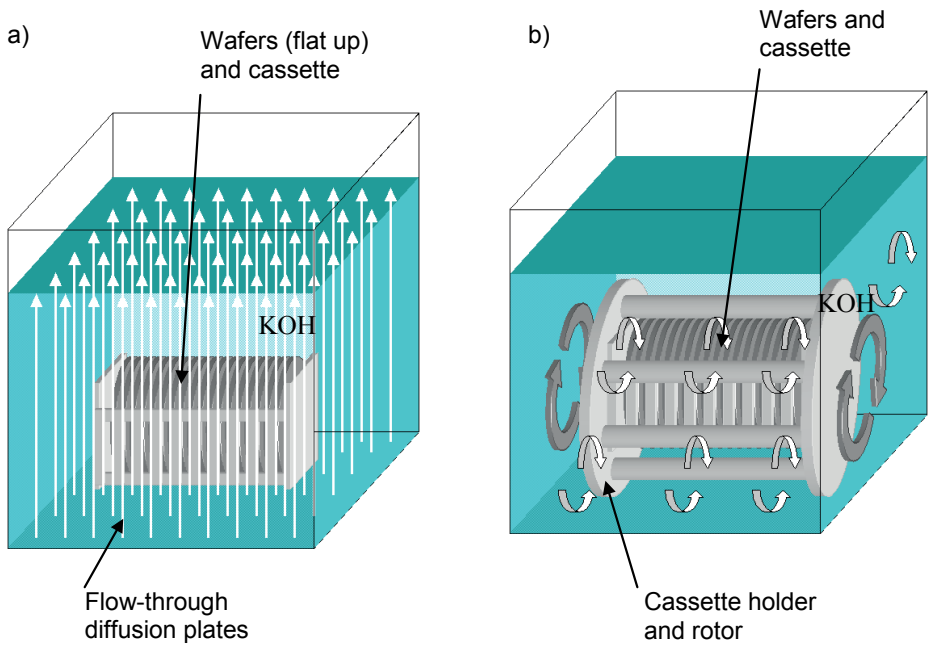


Fig 55. Schematic figures of (a) flow-through wet etching bath and (b) rotational flow wet etching bath.

The best processes for both baths were sought for in designed experiments. The parameters are given in Tables 4 and 5. In the flow-through experiment, the etchant flow and the pump pressure variables were maximum and minimum values for the bath. In the rotational flow experiment, the maximum cassette rotation speed is 50 rpm. In author's previous experiments and chapter 4.1.1, it was found that with rotation the etching results are better than when the cassette is not rotated. It was also found that when the direction of rotation is changed during etching the etch results were even better. A single experiment consists of etching a full cassette of 25 wafers.

Table 4. Variables for flow-through experiment:

etchant flow:	20 l/min	25 l/min	30 l/min
pump pressure:	2.5 bar	3.25 bar	4 bar
cassette type:	standard profile		high profile[1]

[1] High profile cassette: the walls of the cassette were modified as high as the wafers.

Table 5. Variables for rotational flow experiment:

cassette rotation speed:	12 rpm	27 rpm	30 rpm	50 rpm
rotation direction change:	5 min	15 min	18 min	30 min

Additionally, the flow rate and flow direction of the etchant, the sizes and positions of the holes in the cassette through which the etchant flows, etchant overflow directions, wafer cassette types, position of the cassette in the bath and distance between the wafers (wafers in every second slot) were varied. The beam thicknesses were measured in five or nine different locations on a wafer (Fig 50) with a non-contact laser profilometer measurement tool from UBM/Keyence.

6.2.1 Batch level study of rate and uniformity

Temperature variation in the flow-through bath was measured in 17 different locations and three different depths: in top of the bath the temperature was 64.6 °C, in the middle of the bath the temperature was 64.8 °C, and in the bottom of the bath the temperature was 65.0 °C. Because the bottom of the bath had a higher temperature, faster etching was expected there, but this turned out not to be the case. In the rotational flow bath, the temperature variation was similar.

In the flow-through bath, the distance between wafers was found to be one variable that influenced etching. As shown in Fig 56, wide spacing led to standard deviation of the beam thickness across the wafer of 0.4–0.7 µm, while dense spacing resulted in 1–2 µm variation across the wafer.

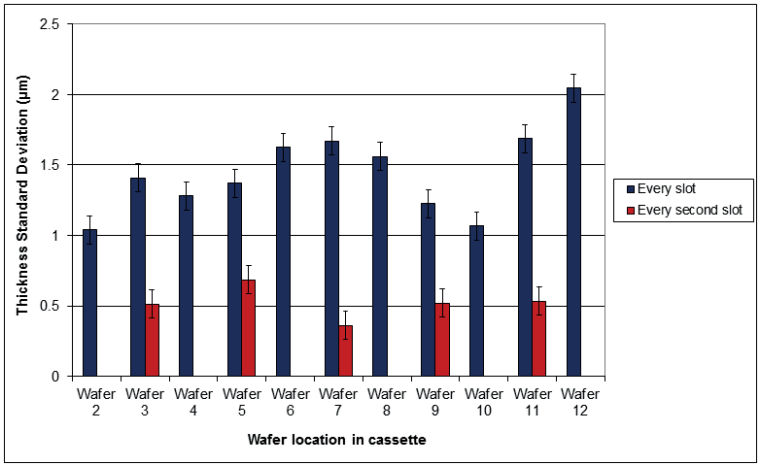


Fig 56. Influence of the distance between wafers in flow-through bath to etching results. Wide spacing led to beam thickness standard deviation across the wafer of 0.4–0.7 µm, while dense spacing resulted in 1–2 µm variation across the wafer.

The results of the flow-through bath experiment are summarized in Table 6. For the flow-through bath, the best process was found to be: high profile carrier, with 30 l/min flow rate and 4 bar pump pressure (which are the maximum values available in the equipment). The run had the lowest etch result (thickness standard deviation) with a value of 0.322 µm.

Table 6. Flow-through bath experiment: etch bath parameters and thickness uniformity results.

Cassette type	Etchant flow (l/min)	Pump pressure (bar)	Etch result - thickness Std. Dev (µm)
Standard profile	20	2.5	0.442
Standard profile	30	4	0.422
High profile	20	2.5	0.472
Standard profile	20	4	0.470
High profile	30	4	0.322
High profile	25	3.25	0.376
Standard profile	25	3.25	0.416

The rotational flow bath experiment results are summarized in Table 7. For the rotational flow bath, the best process was found to be: 27 rpm cassette rotation speed and 15 min rotation direction change. The run had the lowest etch result (thickness standard deviation) with a value of 0.268 µm. This result is also better than the best

result from the flow-through bath, but otherwise the etching results for both baths are quite similar.

Table 7. Rotational flow bath experiments: etch bath parameters and etch uniformity results.

Cassette rotation speed (rpm)	Rotation direction change (min)	Etch result - thickness Std. Dev (µm)
50	5	0.304
50	30	0.371
27	15	0.268
12	5	0.414
12	30	0.473
27	5	0.404
30	18	0.340

After the best processes were found, the experiment was continued with 22 batches to compare the best of both bath types. Ten batches were processed in the flow-through bath and twelve batches in the rotational flow bath. Each batch contained 25 wafers. Comparison of accelerometer beam thickness variation capability between baths is shown in Fig 57. It can be seen that the beam thickness variation is much smaller for the rotational flow bath. The standard deviation of beam thickness for the rotational flow bath is 0.38 µm ± 0.13 µm and that for the flow-through bath is 0.51 µm ± 0.16 µm, or 34% higher.

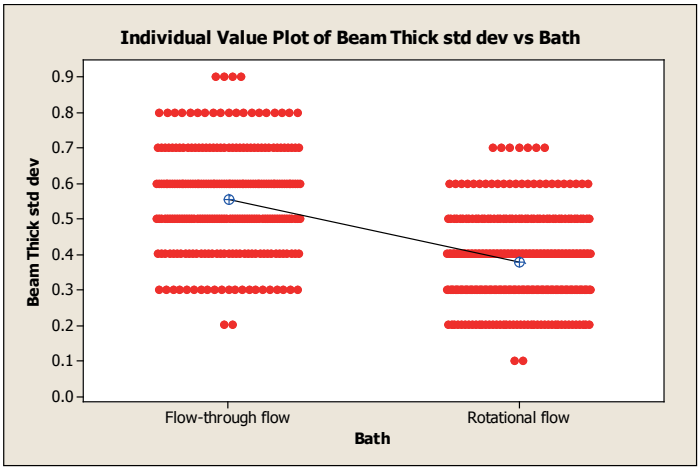


Fig 57. Comparison of accelerometer beam thickness between flow-through and rotational designs. The standard deviation of beam thickness for the rotational bath is 0.38 µm ± 0.13 µm (292 wafers; 2628 data points) and for the flow-through bath 0.51 µm ± 0.16 µm (165 wafers, 1485 data points).

Comparison of batch-to-batch process capability is shown in Fig 58. It can be seen that in the flow-through bath the standard deviations of beam thickness are 0.4–0.7 µm but in the rotational flow bath it is just 0.3–0.4 µm.

a)

b)

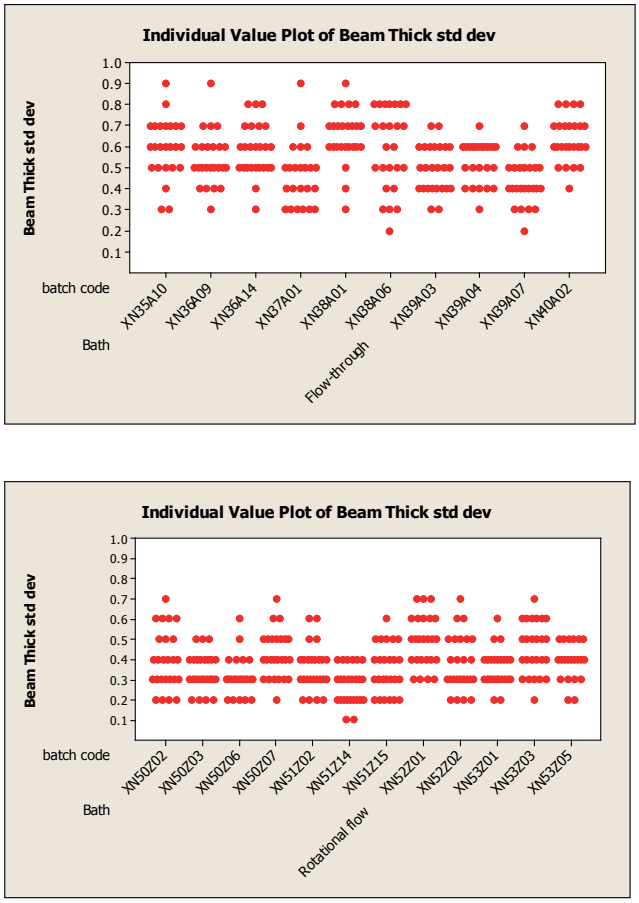


Fig 58. Variation in standard deviation of beam thickness over 10 batches in two baths each (25 wafers in one batch): (a) flow-through bath σ= 0.4–0.7 µm; (b) rotational flow bath σ= 0.3–0.4 µm.

Beam thicknesses across the wafer are shown in Tables 8 and 9. Eight wafers within each batch are compared. In the flow-through bath (Table 8), the position 5 beam near the flat (uppermost) position is consistently the thinnest (i.e., highest etch rate). No such dependency is seen in the rotational flow bath (Table 9). The results also show higher wafer-to-wafer variation in thickness in the flow-through bath.

Table 8. Flow-through bath: beam thicknesses of eight wafers in one batch, measured at 9 points. Measurement point MP5 is always the thinnest.

Flow-through bath

Wafer	1	2	13	14	15	16	24	25	Average	Std Dev
MP1	82.81	83.86	80.71	82.86	82.40	82.67	83.61	82.43	82.67	0.95
MP2	83.47	84.00	80.73	82.62	82.54	82.67	84.56	82.12	82.84	1.19
MP3	82.85	83.19	79.65	82.22	81.23	81.88	83.61	81.95	82.07	1.25
MP4	82.59	83.34	79.72	81.80	81.31	81.44	83.38	81.55	81.89	1.21
MP5	82.97	82.46	79.11	81.14	80.53	80.73	82.20	80.82	81.25	1.25
MP6	82.21	83.49	80.25	81.96	81.98	81.99	83.23	81.78	82.11	0.98
MP7	82.46	83.25	80.68	82.35	82.48	82.55	83.85	82.20	82.48	0.91
MP8	82.66	83.51	79.77	81.87	81.67	81.48	83.46	82.04	82.06	1.21
MP9	82.79	83.67	80.35	82.34	82.12	82.11	83.20	81.92	82.31	1.00
Average	82.76	83.42	80.11	82.13	81.81	81.95	83.46	81.87	82.19	1.07
Std Dev	0.35	0.45	0.57	0.51	0.68	0.65	0.62	0.47	0.54	0.11
Max-Min	1.26	1.54	1.62	1.72	2.01	1.94	2.36	1.61	1.76	0.34

Table 9. Rotational flow bath: beam thicknesses of eight wafers in one batch, measured at 9 points. No one measurement point is clearly thinner or thicker than any other.

Rotational flow bath

Wafer	1	2	13	14	15	16	24	25	Average	Std Dev
MP1	83.38	85.34	83.98	86.90	84.03	86.15	85.87	85.92	85.20	1.25
MP2	83.07	85.18	83.69	86.97	83.94	85.71	85.36	85.39	84.91	1.27
MP3	83.07	84.46	83.68	86.73	84.27	85.83	85.63	85.44	84.89	1.22
MP4	83.51	84.54	84.00	86.33	84.50	85.44	85.42	85.21	84.87	0.90
MP5	83.51	84.83	83.62	85.81	83.93	84.61	84.75	84.49	84.44	0.75
MP6	83.20	85.59	82.90	85.57	83.82	84.56	84.61	84.39	84.33	0.99
MP7	83.12	84.60	83.60	86.76	84.25	85.64	85.12	85.33	84.80	1.17
MP8	83.45	84.84	83.56	86.44	84.23	85.25	85.27	85.25	84.79	1.00
MP9	82.90	84.61	83.58	85.23	83.61	84.62	84.67	84.74	84.25	0.79
Average	83.25	84.89	83.62	86.30	84.06	85.31	85.19	85.13	84.72	1.01
Std Dev	0.22	0.40	0.32	0.63	0.27	0.59	0.44	0.49	0.42	0.15
Max-Min	0.61	1.13	1.10	1.74	0.89	1.59	1.26	1.53	1.23	0.38

Variations in thickness of etched beam across the wafer are shown in Figs 59a and 59b. It is evident that even at the wafer level the etching results are better with rotational flow than with flow-through. In Fig 59a it can be seen that at measurement points 1, 2 and 3 the beam thickness is identical and the thinnest beams were found at point 5. Because initial wafer thickness distribution do not explain this phenomenon, it means that in the top part of the flow-through etching bath the etch rate is at its maximum. There is also some lateral variation, but not to the extent seen in the vertical direction. In the rotational flow bath (Fig 59b) much more uniform distribution of beam thickness is obtained.

a) b)

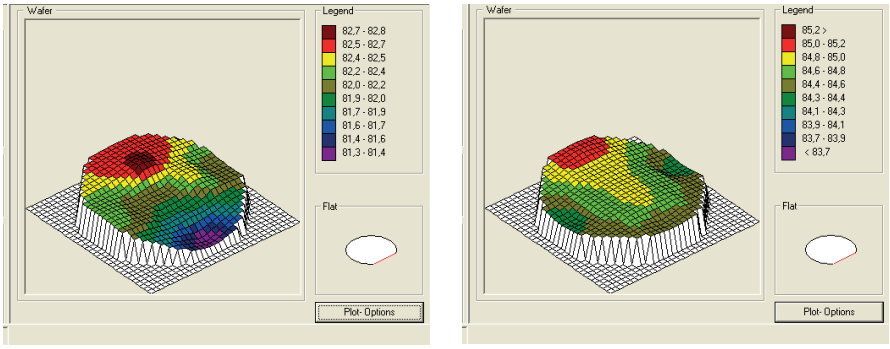


Fig 59 (a) Beam thicknesses near the flat of the wafer are thinner than on the wafer top (σ = 0.57%) in the flow-through bath. (b) In the rotational flow bath the beam thickness uniformity is much improved (σ = 0.37%).

In the flow-through process equipment, there is a consistent significant difference in etch rate between the top and bottom parts of the bath, and because the wafers are static, between the wafer top and bottom. Because the temperature of the bath is higher at the bottom, faster etching at the top cannot be a temperature effect. Neither was able to show any differences in KOH concentration in different parts of the bath.

The roles of reactant supply and the removal of reaction products remain to be explained. Because concentrated solutions are used, OH^- ions and H_2O are not in short supply. However, the etch reaction end products can also influence the overall rate. Products, namely $SiO_2(OH)_2^-$ and H_2 gas, can mask the silicon surface so that

the etching reaction slows down. Hydrogen bubbles are known to cause significant etch rate reduction by preventing etchant from reaching the silicon surface [Seidel 1990 1]. Because in the flow-through bath the flow direction is upwards, it is expected that an overabundance of reaction products, H_2 bubbles, will be transported upwards, and therefore, the upper part (downstream) is swept by the fully developed flow, and is less shielded by hydrogen bubbles. This has been observed in other studies, too [Yang C-R 2005 1]. In the rotational flow system, no direction is preferred, and etch uniformity is better. Thus the potential benefit of the flow-through system, improved control of etchant flow, is not beneficial from the point of view of etch uniformity.

6.2.2 Uniformity across wafer and batch

The results of beam thickness variation across wafer and wafer-to-wafer are studied as a function of etch bath design. Rotational flow design is clearly superior to flow-through design as far as uniformity is concerned. Variation in thickness, wafer-to-wafer and within wafer, in a flow-through bath is 34% higher than in the rotational flow etching equipment.

Contrary to some theoretical considerations, flow-through does not seem to offer benefits with regard to etch uniformity. More controlled influx of etchants is achieved, but, at the same time, removal of the product of the etching reaction is always in the downstream direction. This, author's speculation, is the reason for consistently higher etch rate at wafer top (which is downstream in the flow-through system). Local temperature and etchant concentration as possible explanations are ruled out, and therefore, it led to assume that the more efficient removal of etch products in downstream areas is responsible for the observed higher etch rate.

Process optimization of the flow-through process did not result in as good uniformity as rotational flow process except when wafer spacing was increased. This, however, leads to an unacceptable loss of productivity. A fundamental change in the flow-through process equipment, wafer rotation in flow or flow rotation around wafer could be used to achieve highly uniform etching but then the system complexity would clearly increase.

6.3 Metal impurities in KOH

This part of the study reports how very small changes of Pb impurity with very low concentration level (ppb concentrations) in the aqueous KOH solution used in the MEMS industry can influence significantly the results of anisotropic KOH wet etching of (100) silicon wafers. This chapter also presents the influence of Fe impurity residues on multiple KOH wet etching results when residues are not cleaned away with SC2.

Wafer pretreatment was identical to that described in 6.2 above. The etching solutions in all experiments were mixed from Honeywell 50% Puranal® 17514 quality KOH and DI water. In Pb experiments, two batches of KOH were used (batch #82460 and #81340). Chemical composition was analysed by the vendor, using Inductively Coupled Plasma Atomic Emission Spectrometry (IPC-AES). Analysis results (Table 10) show that there is a difference in K_2CO_3, Na, Al, Ca, Fe, Mg, Zn and Pb concentrations between the two batches. Other impurity concentrations are similar between the batches and the Cu concentration is below 50 ppb in both batches. In lot 82460 the Pb content was 300 ppb, and in lot 81340 the Pb content was 200 ppb. Based on [Tanaka 2000] the main impurity of interest is thus Pb.

Table 10. Analysis of KOH purity by Inductively Coupled Plasma Atomic Emission Spectrometry (IPC-AES).

	Honeywell 50% Purnal	Honeywell 50% Purnal
lot	82460	81340
assay	49.80 %	50 %
assay of K2CO3	400 ppm	500 ppm
Sodium (Na)	1700 ppm	1800 ppm
Aluminium (Al)	< 500 ppb	< 1000 ppb
Calsium (Ca)	800 ppb	< 1000 ppb
Cobalt (Co)	< 200 ppb	< 200ppb
Chromium (Cr)	< 100 ppb	< 100 ppb
Copper (Cu)	**< 50 ppb**	**< 50 ppb**
Iron (Fe)	< 500 ppb	1000 ppb
Magnesium (Mg)	< 300 ppb	< 500 ppb
Manganese (Mn)	< 300 ppb	< 300 ppb
Nickel (Ni)	< 100 ppb	< 100 ppb
Zink (Zn)	< 300 ppb	< 500 ppb
Lead (Pb)	**300 ppb**	**200 ppb**
Chloride	< 1500 ppb	< 1500 ppb
Phosphate (PO2)	< 1500 ppb	< 1500 ppb
Silicate (as SiO2)	< 1500 ppb	< 1500 ppb
Sulphate (SO4)	< 1500 ppb	< 1500 ppb
Total N	< 2000 ppb	< 2000 ppb

The beam dimensions were measured in nine different locations on a wafer with the non-contact laser profilometer measurement tool from UBM/Keyence (Fig 50). Direction <110> etching and angle of fastest etching plane projection were measured from wafers etched with special anisotropy figure. The etched anisotropy figure was photographed with an optical microscope, and under a SiO_2 mask the under-etching length of etched direction <110> and the fastest etching plane projection angle were measured from the picture using figure treatment software. Fig 51 shows the measured dimensions of the etched anisotropy figure.

6.3.1 The effects of metallic impurities on rate and surface quality

A particular phenomenon can be observed on these experimental wafers. After KOH etching, the etched surface was covered by particles. SEM EDS analysis shows that particles contain iron (Fe) and oxygen. When not removed, the particles cause shallow etch pits on the silicon surface in further KOH etching steps, as shown in Fig 60. It was also found that the particles can be removed by SC2 cleaning after the etching step. Bergenstof Nielsen *et al.* [Bergenstof Nielsen 2000] reported deposition of inorganic (Fe_xO_y) particles in connection with the KOH etching of silicon membranes. They reported that the source of the particles was the KOH pills used for making the etching bath.

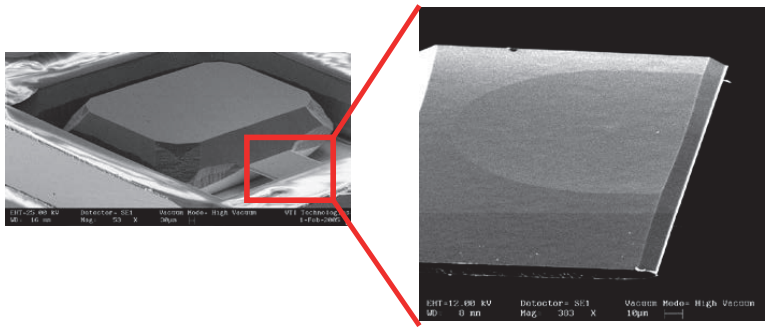


Fig 60. SEM picture of anisotropic KOH wet etched single crystalline silicon seismic mass and spring beam. In the spring beam, there is a shallow etch pit caused by (Fe_xO_y) particles.

The same kind of shallow etch pits, shown in Fig 61, are formed on the etched surface when it is exposed to oxygen plasma before etching. The main difference between shallow etch pits caused by Fe_xO_y particles and those caused by oxygen plasma is that the latter pits are always like twins. This kind of etching result indicates that the oxygen plasma induced stacking faults to the crystal structure. Stacking faults are a type of crystal defect having a twin structure like the shallow etch pit in Fig 61.

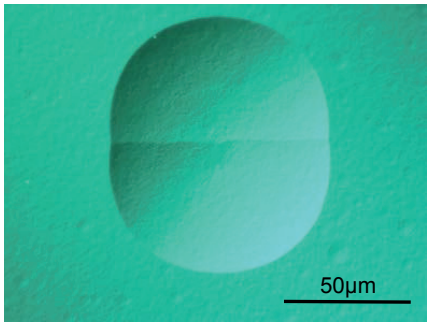


Fig 61. Microscope picture of anisotropic KOH wet etched single crystalline silicon wafer surface with wide twin etch pit induced by oxygen plasma.

Based on the measurements of the etched anisotropy test figures, the increase in the concentration of Pb ion does not influence the anisotropy ((110) plane / (100) plane etching rate) and the fastest etching plane projection angle. Anisotropy is about 4.0 and the average of the fastest etching plane projection angles is 28.7°, which is average from (31X) crystal plane projection in angle 26.57° (where X can be 1,2,3…) and (41X) crystal plane projection in angle 30.96° (where X can be 1, 2, 3…). This is the case because around the 65 °C and 20 wt-% KOH the fastest etching plane can alternate between these two crystals.

The etch rates of planes (100), (110) and (111) are shown in Table 11. Table shows that there is a difference in the etching of (100) plane and (110) plane between aqueous KOH with low Pb concentration (200 ppb) and with high Pb concentration (300 ppb).

Table 11. Anisotropic etch rates of planes (100), (110) and (111) in low Pb concentration (200 ppb) aqueous KOH and high Pb concentration (300 ppb) aqueous KOH 65 °C and 20 wt-%.

Pb concentration (ppb)	(100) plane etching rate (µm/min)	(100) plane etching rate (µm/min)	(100) plane etching rate (µm/min)
200ppb	0.516	2.086	0.015
300ppb	0.477	1.927	0.013

In the accelerometer, with a six-hour etching process, with Pb concentration of 300 ppb, the etching amount of (100) plane is about 28 µm smaller than with Pb concentration of 200 ppb, and for (110) plane the etching amount is about 115 µm smaller in Pb concentration of 300 ppb than in Pb concentration of 200 ppb. In a six-hour etching, this 28 µm difference in plane (100) etching amount means a 7% difference in (100) plane etch rate, and in plane (110) the 115 µm difference in etching amount means also about 7% difference in etch rate. However, still in a six-hour etching, the etching amount of (111) plane in Pb concentration of 300 ppb is below 1 µm smaller than in Pb concentration of 200 ppb. In plane (111), this below 1 µm difference in etch rate means about a 12% difference between Pb concentration 200 ppb and 300 ppb. However, this result of difference in etch amount and etch rate for plane (111) is unsure because the below 1 µm difference in etching amount is very hard to measure precisely.

The effects of small amounts of copper and lead impurities on KOH anisotropic etching in 32 wt-% and 110 °C KOH solution were studied in [Tanaka 2000, Tanaka 2006]. It was found that ppb-level of Cu roughens the silicon surface from 1 µm to over 4 µm when Cu concentration increases from 100 ppb to 300 ppb. After the Cu concentration increases above 200 ppb, the etching rate of plane (110) starts to decrease linearly from 9 µm/min to below 7 µm/min in 10 000 ppb Cu concentration. The influence of Pb on the etching rate of (110) plane is more complex. The etch rate decreases from 9 µm/min to 7 µm/min when Pb concentration increases from 20 ppb to 100 ppb. Above 300 ppb Pb concentration, the etch rate again starts to increase, and in 10 000 ppb Pb concentration the etch rate is about 8 µm/min. In the results, with 20 wt-% and 65 °C, the etch rate of (110) plane was 2.086 µm/min with 200 ppb Pb concentration and 1.927 µm/min with 300 ppb Pb concentration. For (100) plane the etch rates were 0.516 µm/min and 0.477 µm/min. Comparison shows that in 32

wt-% and 110 °C KOH solution the influence on etch rate of (110) plane is about zero when Pb concentration increases from 200sppb to 300sppb. The results show that in 20 wt-% and 65 °C KOH solution the influence on etch rate of (110) plane is about 7% when Pb concentration increases from 200 ppb to 300 ppb.

The effects of Cu and Pb are explained by the interaction between ions and hydrogen gas generated during etching based on the oxidation–reduction potentials of Cu, Pb and H. Because the oxidation–reduction potential values of Pb are equivalent to that of H, it is assumed that the reaction of Pb reduction–ionization can be opposed to the etching reaction, thus the etching rate is changed. The oxidation–reduction potential values of the against normal hydrogen electrode (NHE) are shown in Table 12.

Table 12. Reduction–oxidation potential in caustic solution at high pH.

Impurity	Zn	Mg	Fe	Pb	H	Cu	Ag
Potential (V vs. NHE)	-1.45	-1.25	-1.05	-0.91	-0.85	-0.40	+0.25

Cu and Pb exist as Cu ion (CuO_2^{2-}) or Pb ion ($HpbO_2^-$). It is found that the potentials of Cu and Pb, both of which change the etch rate and surface morphology significantly, are close to that of hydrogen. The effect of Cu and Pb ions on the solution can be explained by the interaction between each of these ions and the hydrogen generated at the oxidation step during etching. Although author's results are not identical with Tanaka *et al.,* the author agrees with their proposed model.

The reaction between hydrogen and Cu or Pb is considered as follows:

$$CuO_2^{2-} + H_2 \rightarrow Cu + OH^- \quad (28)$$

$$HpbO_2^- + H_2O \longleftrightarrow PbO_2 + OH^- + H_2 \quad (29)$$

Cu metal particles deposit on the Si surface during etching. Because the oxidation–reduction potential of Cu (-0.40V) is higher than that of H (-0.85V), it is considered that Cu ion is reduced to Cu metal by H, and Cu particles on the Si surface can act as an etching mask. On the other hand, because the oxidation–reduction potential value of Pb (-0.91V) is close to that of H (-0.85V), it is assumed that the reaction of Pb reduction–ionization can oppose to the etching reaction, thus the etching rate is

changed. Because Pb reduction–ionization is in equilibrium, it is considered that Pb deposition on the Si surface is limited and does not affect the Si surface roughness.

The oxidation–reduction potential of Ag (+0.25V) is more positive than that of Cu (-0.40V). Because the potential of Ag is too high, the Ag ion reduces to Ag metal particle directly in the solution due to the H gas produced during etching, and the effect of Ag does not appear on the etching properties. The potentials for Zn (-1.45V), Mg (-1.25V) and Fe (-1.05V) ions are lower than that of H. As a result, these ions can exist in the solution and they are not changed, so the etching properties are not affected.

In the experiments, the KOH solution of 20 wt-% at 65 °C and (100) silicon wafers was used. Tanaka *et al.* used a hemispherical single-crystal silicon specimen to evaluate the effect of the ppb-level of Cu or Pb on KOH solution for a number of crystallographic orientations. The specimen was etched at 110 °C in 34 wt-% KOH without addition, with addition of 360 ppb Pb and with addition of 360 ppb Cu. This study found a difference in etch rates between 0 and 3μm/min. The maximum decrease in all orientations was 24.4% with 360 ppb of Cu and 12.9% with 360 ppb of Pb. With the addition of Cu, the location of the maximum etch rate moved from the vicinity of the (210) orientation to the (110) plane. The etch rate from the top to the (311) and (312) planes decreased to about 80% of that without addition almost uniformly. The etch rate decreased most in the vicinity of the (210) plane. The etch rate in the vicinity of the (111) and (100) planes did not change. With the addition of Pb, the anisotropy of the etch rates was almost the same as without Pb, but the etch rate decreased at almost all orientations. The etch rate from the top to the (100), (311) and (321) planes decreased by about 10% almost uniformly. The etch rate in the vicinity of the (110) plane decreased most. Compared with the addition of Cu, the decrease of etch rate with the addition of Pb is minor, but the etch rate decreased uniformly for all orientations.

In the vicinity of the (111) plane, the difference in the etch rate did not change with the addition of Cu or Pb. A triangular contour of a valley centred at (111) in case of KOH without an addition means that a mono-hydride terminated step is more stable than a di-hydride terminated step. With the addition of Cu or Pb, almost the same triangular

appeared with the same triangular contours. Therefore, it seems that Cu and Pb are not active on di-hydride terminated steps.

6.3.2 Metal-induced roughness and rate anomaly

Roughness and etch rate anomalies in lead-contamined KOH are explored in this experiment. An increase of Pb concentration from 200 ppb to 300 ppb decreases the etching rate of the (100) plane and (110) plane over 7% and the (111) plane etching rate by over 12%. However, the (111) plane etching rate is so small that it is very hard to measure the difference in etching amounts precisely. Even after six hours of etching the difference is below 1 μm. Besides, the Pb ion concentration increases do not have any influence on the anisotropy ((110) plane etch rate / (100) plane etch rate) and the fastest etching plane projection angle. The effect of Pb can be explained by the interaction between ions and hydrogen gas generated during etching based on the oxidation–reduction potentials of Pb and H. Because the oxidation–reduction potential value of Pb is equivalent to that of H, it is assumed that the reaction of Pb reduction–ionization can oppose the etching reaction, thus the etching rate is changed. Therefore, only by controlling the ppb level of certain impurities (Cu and Pb) and controlling certain process steps before KOH etching (for example, resist patterns oxygen plasma etching) and by removing carefully all etching residues from the etched silicon surface (for example, Fe_xO_y particles), it is possible to achieve the most even physical and mechanical structures for MEMS and be able to approach silicon NEMS structures.

7. Silicon wafer engineering for KOH etch optimization

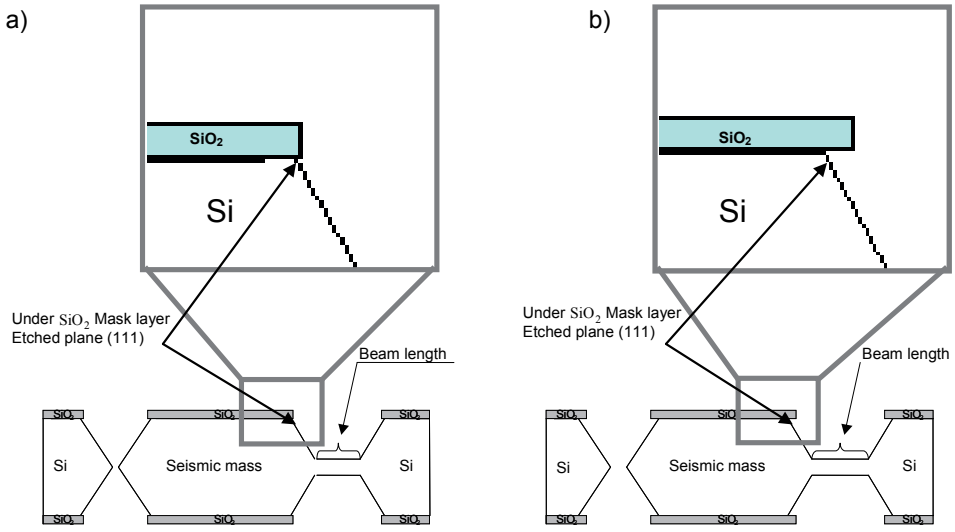
The present chapter introduces the first three different phenomena that influence the anisotropic etching of silicon in aqueous KOH solution. They are:

1) Impurities in Si wafer - chapter 7.1
2) Surface finish of Si wafer and removal of defects (KOH dip) - chapter 7.2
3) Surface finish of Si wafer and removal of defects (Ultra Poligrind) - chapter 7.3

7.1 MEMS beam length control by optimizing silicon oxygen concentration for wet etching

In this study, the magnetic-field-assisted Czochralski (MCZ) wafers that have recently become available [Härkönen 2005] are used. They have much lower oxygen concentration than traditional CZ wafers. Anisotropy variation in KOH etching due to oxygen concentration was studied. This variation affects MEMS beam length directly, and consequently accelerometer performance. An even more serious problem due to oxygen level variation is unsuccessful etching of a seismic mass, which causes non-functioning accelerometers. This chapter shows that both low and high oxygen concentrations are beneficial for KOH etching, but that the intermediate range is problematic.

An accelerometer with KOH etched seismic mass was used as a test device. The seismic mass is fabricated in the middle wafer by a double-sided, nested mask etching process. The etching of the (111) plane under the SiO_2 mask results in beam length differences, as shown in Fig 62. Larger under-etching (higher etch rate of (111) plane) results in longer beams. It also results in lighter seismic mass because (111) planes form the walls of the seismic mass. However, the influence of seismic mass weight on the measuring capability of the accelerometer sensor element is minor compared to the influence of the beam length.



7 ppma oxygen level wafer

15 ppma oxygen level wafer

Fig 62. Schematic of seismic mass (111) sidewall plane etching under SiO_2 mask for two oxygen levels: under-etching is more serious in the case of oxygen level of 15 ppma (a) than for 7 ppma (b).

P+(100) CZ silicon wafers of 150 mm diameter and 380 µm thickness were used. Because of their symmetric structure, double-side polished wafers (DSP) were employed. The bulk oxygen levels of the CZ wafers were 15 ppma (7.5 x1 0^{17} cm^{-3}). The bulk oxygen levels of the MCZ wafers were 10 ppma (5.0 x 10^{17} cm^{-3}) and 7 ppma (3.5 x 10^{17} cm^{-3}). The bulk oxygen of the wafers was measured with SIMS by EAG Analytical Laboratory in the USA under protocol ASTM F1366-92.

The wafer pretreatment was as described in 6.2 above. The wafers were cleaned in SC1 (ammonia-peroxide solution) and rinsed in DI water before KOH etching. Etching solutions were mixed from Honeywell PURNAL quality KOH and DI water. The first short KOH etching defines the area to be released in the end. Etching conditions were 65 °C and concentration 20 wt-%. The exposed oxide mask on top of the beam is etched away in BHF and the second KOH etch step uses a nitride mask to etch through the wafer in the rim area and to define the beam area. These etches are done batch wise in a turbulent flow dynamic etching bath. In turbulent flow, bath

cassette rotation speed of 27 rpm and rotation direction change every 15 min were used. The final beam thinning etch (75 °C concentration 40 wt-%, a static etching bath) was done on one wafer at a time, with target thickness for the beam of 18 µm. The resulting seismic mass and beam are shown in Fig 1. The beam dimensions were measured in nine different locations on a wafer with non-contact laser profilometer from UBM/Keyence (Fig 50).

7.1.1 Beam length dependence on oxygen

Three different oxygen concentration levels were chosen for the study. The highest of these, 15 ppma, is also available in standard CZ material, but the 10 ppma and 7 ppma levels are only available from Magnetic-field-assisted Czochralski (MCZ) crystal growth.

Seismic mass etching of these materials leads to markedly different end results, as shown in Fig 63. In these optical micrographs, it is evident that both high and low oxygen concentrations result in correctly etched seismic masses, but 10 ppma oxygen results in incompletely etched frame (Fig 63b). The problem areas are marked by ellipses. In those areas the seismic mass is still attached to the frame of the element and the element is not functional. This etching anomaly is frequent in 10 ppma wafers, but does not occur in 7 ppma and 15 ppma wafers. This means that the etch rate has been too slow and too unpredictable due to the difference in defect (stacking fault) density of the crystal.

a) b) c)

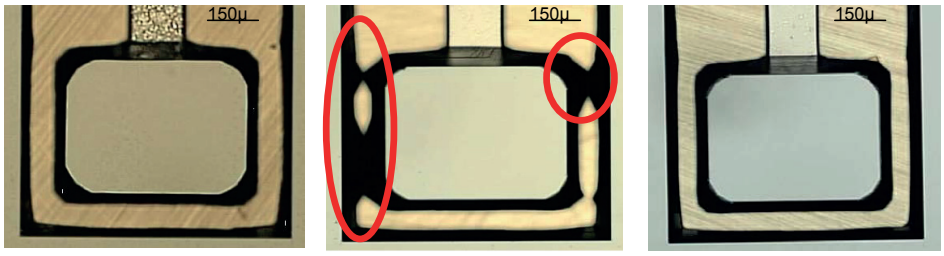


Fig. 63. Optical micrographs of etched seismic masses as a function of wafer oxygen level: (a) 15 ppma, (b) 10 ppma and (c) 7 ppma. Etching has failed in case (b) as evidenced by the discontinuous accelerometer frame.

Measured beam dimensions are shown in Fig 64. There is no difference in beam thickness between high and low oxygen level wafers because the wafers were etched to target thickness. The beam widths are almost identical for high and low oxygen level wafers: the 1.9 µm difference corresponds to just 1.4%. However, the beam length difference is significant. In high oxygen level wafers, the beam length is 6% longer than in the low oxygen case. Beam length differs due to the difference in defect (stacking fault) density of the crystal. This reflects changes in the etch rate of (111) plane and in anisotropy between planes (100:111).

However, later experiments have shown that to achieve identical beam widths in 7 ppm and 15ppm material the etching time in 40 wt-% KOH must be increased in 7 ppm material. In production this is done to split the second KOH etch step so that first the beam is etched to 150µm thickness in 20 wt-% KOH (65 °C) and from there to 80µm thickness in 40 wt-% KOH (75 °C).

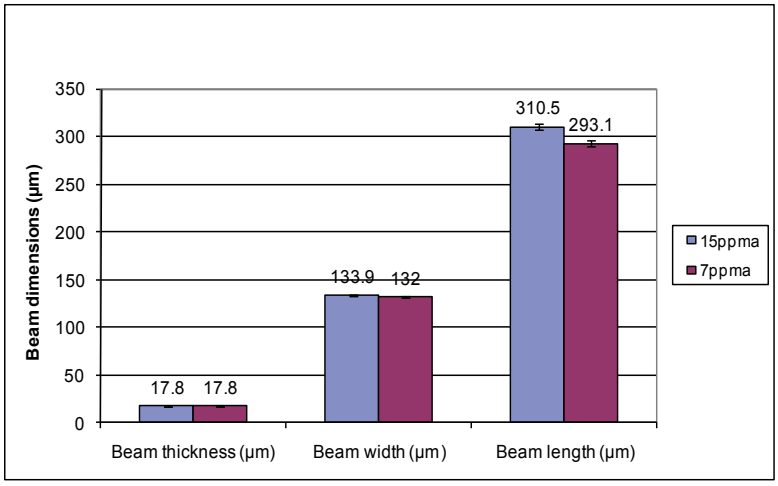


Fig 64. Beam thickness, beam width and beam length of MCZ wafers with high oxygen level (15 ppma) and low oxygen level (7 ppma). The results for 10 ppma beams are not shown because of failed etching.

The moment of inertia calculated from equation 26, when the value of 167 GPa is used for Young's modulus E, is 31.4 N/m for the 15 ppma cases and 36.8 N/m for the 7 ppma cases. In acceleration measurement this 5.4 N/m inertia difference means

over 10% difference in F3dB average value. F3dB is the frequency where the gain is 3 dB lower than the gain at a specified reference frequency. In many applications 10% difference in F3dB value means that the devices are outside specifications.

a)

b)

c)

Fig 65. Optical micrographs of etched (111) planes (seismic mass walls) as a function of wafer oxygen level: (a) 15 ppma, (b) 7 ppma and (c) 10 ppma.

In order to understand better the differences in etching behaviour, the etched (111) sidewalls were studied. In Fig 65a, it can be seen that the etched (111) plane of the 15 ppma wafer exhibits numerous etch artefacts and it is rough. The (111) plane of low oxygen material is very smooth, as shown in Fig 65b. The intermediate case is shown in Fig 65c. It is seen that etched (111) plane has fewer etch artefacts than the high oxygen material of Fig 65a, and it is partly very smooth, comparable to the low oxygen case. In the 15 ppma material, there is a high etch pit density due to the high density of small precipitates and, consequently, a high stacking fault density. The (111) etch rate is predictable due to a high number of randomly distributed defects. In the low oxygen material the amount of bulk oxygen stacking faults is low enough so that stress-free areas dominate the (111) plane etch rate and etching anomalies are absent. Oxygen level of 7 ppma is so low that oxygen precipitates are not able to form

and grow. The intermediate material leads to erratic etch rates depending on the details of the wafer's thermal history and particulars of the etching process.

Crystal plane anisotropy between (111) and (100) planes was 120:1 for FZ wafers and 70:1 for CZ wafers before thermal treatment, and 30:1 and 15:1 afterwards [Hein 2000]. This was explained as etch rate enhancement of the (111) plane due to stresses generated by oxygen precipitation.

The measured undercuts are about 8.5 µm in 15 ppma wafers and nil in 7 ppma wafers. These are much smaller than those in [Hein 2000] but the general trends are similar. Mask undercut measured in [Hein 2000] as a function of wafer oxygen concentration had a threshold value of 13–14 ppma. Below that the concentration undercut was constant at 20 µm, and above that it increased to 80 µm. This threshold value was coincident with oxygen precipitate formation due to high temperature anneals. The author assumes that the smaller undercuts result from the optimization of KOH etch parameters for the accelerometer. In different applications, the relative importance of different etch responses is different: for example, etched (100) bottom quality in membrane applications is more important than (111) sidewall quality, which is important in optical applications [Kwa 1995].

A similar study of crystal plane etching has been carried out for (110) wafers [Hölke 1999]. It was found that oxygen precipitates strongly affect (110):(111) selectivity, and reduce the available aspect ratios. The proposed remedy was 1300 °C annealing, which dissolves oxygen precipitates and results in 230:1 (100):(111) etch rate ratio in KOH. This approach, however, is not generally applicable because 1300 °C annealing requires special furnace hardware.

Similar superior surface quality of wafers with low oxygen concentration has been reported in [Kwa 1995], where 0.4 ppma FZ wafers were compared with 20–36 ppma CZ wafers. In [Hein 2000] surface roughness of the etched (111) wall was measured to increase from 5 nm to 30 nm for CZ material and from 5 nm to 20 nm for the FZ material during extended thermal treatments. However, the adoption of FZ material is often not an option, due to limited availability of MEMS-specified wafers with accurate

thickness, low TTV and orientation accuracy, and FZ material is not at all available in larger wafer sizes.

7.1.2 Optimizing silicon oxygen concentration

KOH etching results vary as a function of silicon wafer oxygen concentration. This has been explained by the stresses generated by oxygen precipitate formation during high temperature process steps. Using novel MCZ material, the author has found two different regions where silicon wet etching processes can be successfully carried out. Oxygen at 15 ppma results in reproducible KOH etching with rough surfaces. Material with 7 ppma results in reproducible KOH etching with smooth surfaces. The former material results in high uniform density of oxygen precipitates, while in the latter the material oxygen concentration is so low that precipitates cannot be formed during thermal treatments. However, the intermediate material with 10 ppma oxygen creates large and random oxygen precipitates which cause large anomalies in local etch rates. Etching results become highly dependent on details of oxygen concentration and thermal loads that the wafer has experienced. When the wafer oxygen level is 10 ppma, the relative proportions of bulk oxygen stacking fault areas and stress-free areas are similar and cause etching anomalies. In the worst case, the sensor element is still attached to the frame.

As a general strategy, thermal budget limitation is a way to reduce oxygen precipitate formation. However, due to other process requirements this is not always possible. Wafers with 10 ppma oxygen level wafers are used in the IC industry [Sama 2001] where suitable oxygen precipitation level in bulk reduces metal impurities in the active surface region by internal gettering. In the fabrication of integrated CMOS-MEMS devices, this oxygen level will be problematic for optimization of the MEMS part. As discussed in [Müller 2000], 15 ppma or even higher oxygen concentration may be more advantageous for integrated IC-MEMS devices. In simpler devices with a limited number of process steps, it may suffice to replace thermal mask oxides by (PE)CVD oxides deposited below 900 °C, and this reduction in thermal budget is enough to eliminate oxygen precipitates [US5131978 1992].

All structures that require accurate device dimension controls are critically dependent not only on KOH etch parameters but also on wafer oxygen level and thermal history. A change to 7 ppma MCZ material requires etch process qualification and device redesign. All functional dimensions and structures must be designed for the new material. Applications where this control is beneficial include mechanical beams and masses, and mirrors and other optical elements because it can produce smooth (111) planes.

7.2 Low cost non-polished MEMS wafers

In this study, the effects of grinding damage on a MEMS test structure are explored. This section shows how the grinding damage affects the dimensions of a MEMS pillar and acts as an accurate indicator of damage. Removal of damage by a short KOH etch (KOH dip) prior to etching MEMS structures is employed to recover high quality silicon. The results indicate that grinding plus KOH dip results in wafers comparable to polished wafers.

Wafers used in these experiments were 150 mm P+(100) CZ silicon wafers. Wafers were ground first with Mesh 320 wheel and in the second step by fine grind with Mesh 4000 grinding wheel (Disco Poligrind) over 30 µm.

After grinding, the wafers were cleaned in ammonia-peroxide (SC1) bath, and etched in KOH, after which they were rinsed in DI water. The etching solutions were mixed from Honeywell PURNAL quality KOH and DI water. The damage removal conditions of KOH solution were temperature 75 °C and concentration 40 wt-%. Etching was carried out in a temperature controlled static bath. These parameters correspond to standard static bath etching. Wafers were etched for 60 s and etching depth was approximately 0.6 µm on both sides. This step is termed ‘KOH dip’. Wafer pretreatment was as described in 6.2 above. The test structure is shown in Fig 66.

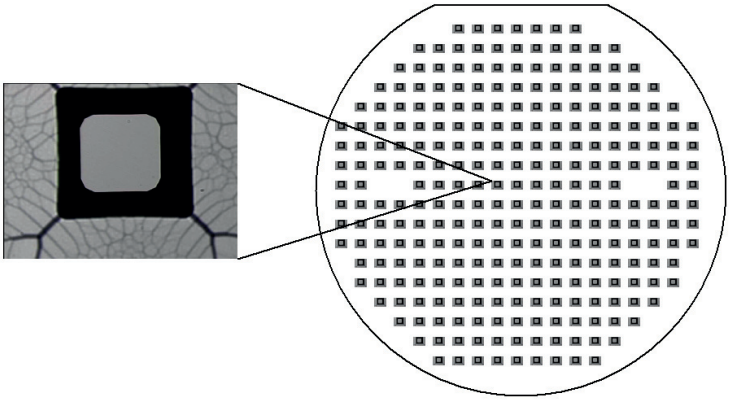


Fig 66. KOH etched silicon pillars in accelometer capping wafer.

The temperature of the KOH solution was 70 °C and the concentration was 15 wt-%. These were chosen because of favourable anisotropy features for long and deep etching (mask layer etching speed is low enough). In each run 25 wafers were etched to approximately 127 μm pillar height from single side – 25 wafers was the standard etching batch in production. Rotational flow dynamic etching equipment was used. In the rotational flow bench, the parameters used were cassette rotation speed of 27 rpm, and the rotation direction was changed during the process every 15 min.

Direction <111> under etching and (111) and (100) planes etched surfaces were measured from etched silicon pillars from accelometer elements capping wafer. Etched pillars were photographed with optical microscope, and under SiO_2 mask the etched direction of <111> under-etching was measured from the picture using figure treatment software (Fig 67). Etched pillars on the (111) plane and the etched surface of the (100) plane were photographed with optical microscope.

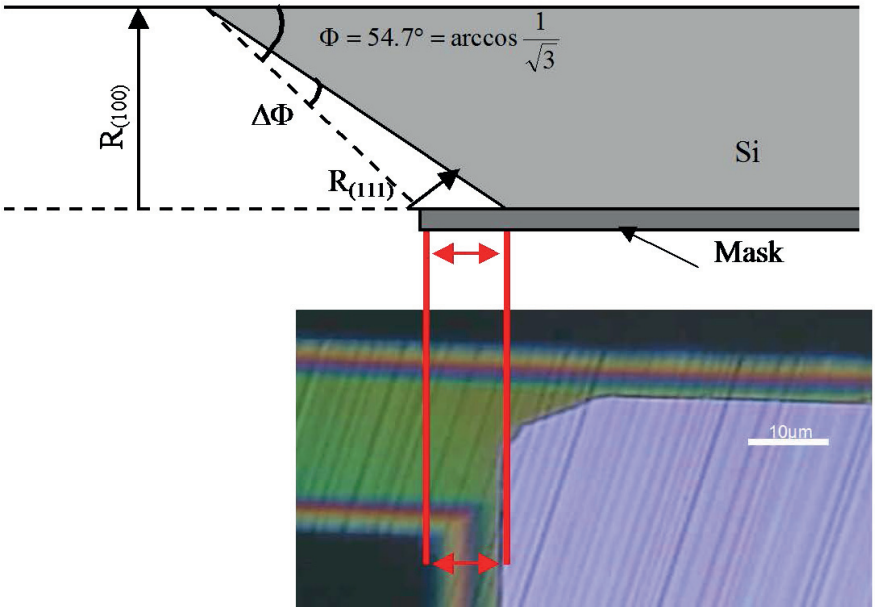


Fig 67. Schematic figure of direction <111> under etching and optical microscope photograph of etched pillar with direction <111> SiO_2 mask under etching.

Surface roughness was measured by Micromap 560 optical profilometer. Micromap 560 is an interference microscope that enables contactless measurement of surface micro-geometry in 3D. The height resolution of the tool is approximately 1 nm and the size of a surface measurement area was either 153 x 119 µm or 754 x 588 µm. The number of measurement pixels was 304 x 228.

Nanoindentation characterization for the test wafers for a surface / sub-surface damage investigation was done in Aalto University, Department of Materials Science and Engineering, by TriboIndenter® Nano-mechanical System.

7.2.1 Influence of grinding damage on etching results

Three kinds of wafers with the same test structure were etched in the same etch bath: fine ground, fine ground plus KOH dip, and polished prime wafers. Etching time was 225 min and etched depth 110 µm. Under-etching of the oxide mask was 9 µm in the

fine ground wafers. KOH dip reduced this to around 3 µm. This is similar to polished reference wafers. The results from 56 wafers etched are summarized in Table 13.

Table 13. Comparison between average mask undercut

Level	**Wafer type**	**N**	**Mean**	**StDev**
	Fine grinding + KOH-dip	18	2.8 µm	0.3 µm
	Fine grinding without KOH-dip	18	9.1 µm	0.9 µm
	Polished reference wafer	18	3.5 µm	1.2 µm

Mask undercut is shown in the optical micrographs of Fig 68. These pictures clearly show that the fine ground wafer with KOH dip shows the smallest under-etching (68a) and the fine ground wafer without KOH dip shows the largest under-etching (68b). Under-etching of reference polished wafer (68c) is intermediate.

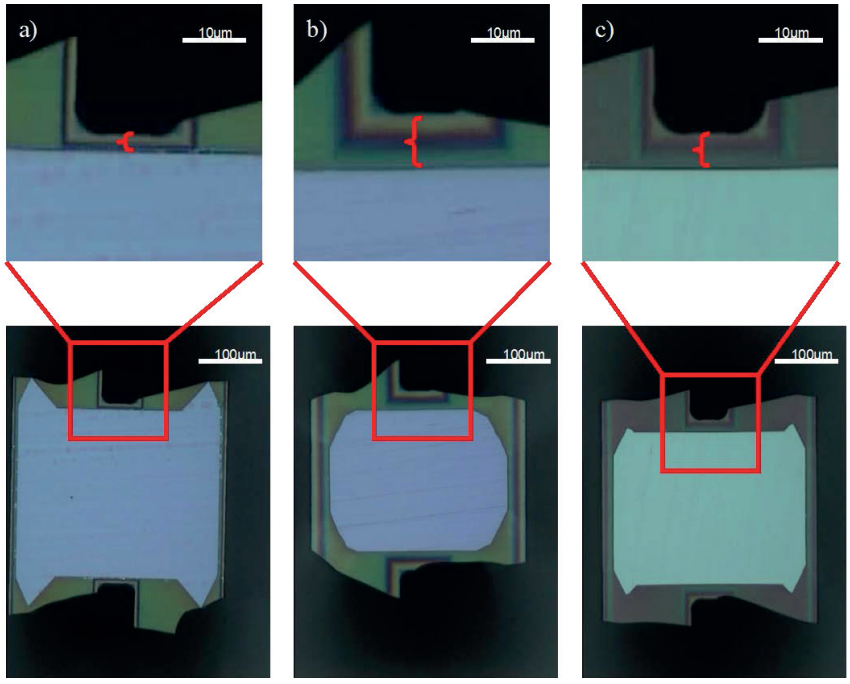


Fig 68. Optical micrographs of mask undercut: (a) fine grind wafer with 60 s KOH dip, (b) the fine ground wafer without KOH dip, (c) polished reference wafer.

An optical micrograph of the surface after 20 µm fine grinding and KOH-dip (75 °C and 40 wt-%) is shown in Fig 20. The cracks caused by coarse grinding are still visible and they were enlarged in KOH-dip. KOH etchant penetrated into the cracks and etched the surrounding silicon material because there are many crystal planes exposed to the etchant, and some of them etch faster than the (100) plane. A series of KOH etching runs was made to determine the needed material removal. Based on these results, the fine grinding depth was set to 30 µm to eliminate cracks caused by coarse grinding. This is somewhat deeper than proposed by Yang *et al.* [Yang Y 2008].

Even though the measured surface roughness after fine grinding was below 5 nm RMS, defects were visible to the naked eye. The explanation is that there are occasional deeper grooves which were not captured by the profilometer (scan area 0.4 mm^2). In Fig 69, one such groove is shown, about 4 µm deep (Peak-to-Valley, P-V value) and 5 µm wide.

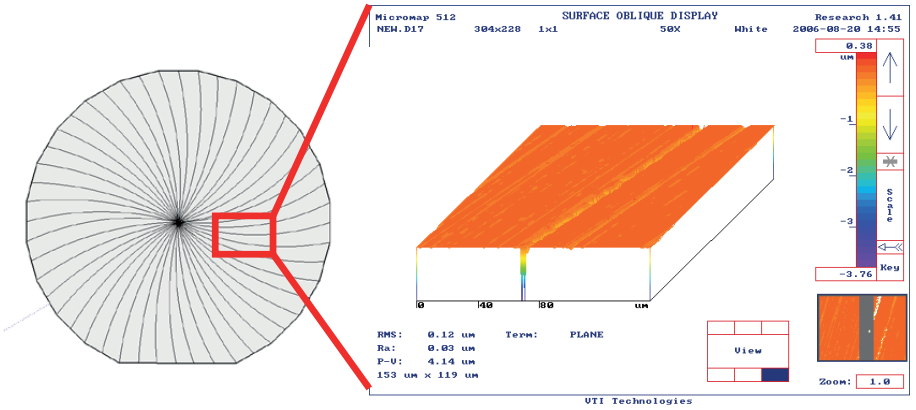


Fig 69. Optical profilometry map of a single deep groove after fine grinding and KOH dip. The depth is ca. 4 µm.

The optical micrograph of Fig 70a shows mask undercut for a ground wafer without KOH dip. The spherical depressions (pearl-chain/bamboo type defects) result from grinding grooves. In Fig 70b, the 9 µm mask undercut is to be seen. This extended undercut is a result of fast etching of the damaged surface layer. In Fig 70c, grooves

on the (111) etched surface are shown. The arrows point to the grinding grooves on the original surface. The (111) wall is very rough.

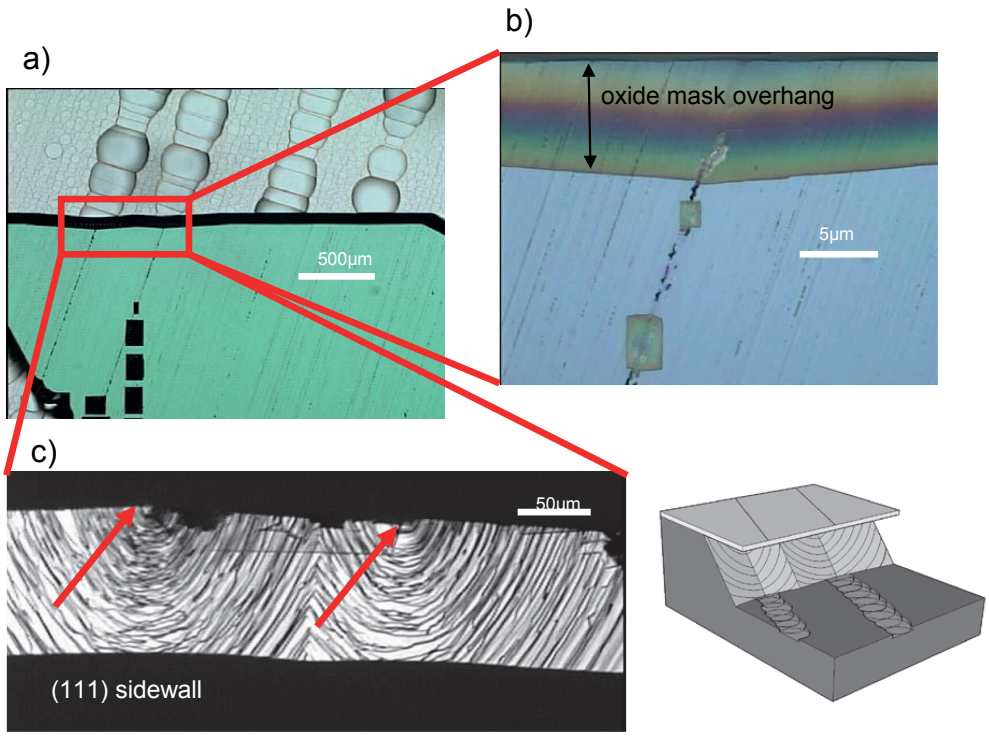


Fig 70. Ground wafer without KOH dip. Silicon etched 110 µm deep: (a) overview, (b) detail of mask undercut, (c) two large grooves result in rough (111) surface.

The optical micrographs for a KOH dipped wafer are shown in Fig 71. The spherical depressions are identical to the ground case, but the oxide undercut is greatly reduced. The KOH etched (111) plane is much smoother. The structures of the deeper grooves at the etched bottom surface were characterized by optical profilometry. Fig 72 shows data on the groove profile. The depth of the groove is about 3 µm. This is comparable to 4 µm depth measured for ground wafer. The width of the spherical depressions is from 200 µm to 300 µm. This is much wider than for the untreated case, and results from the deep KOH etching.

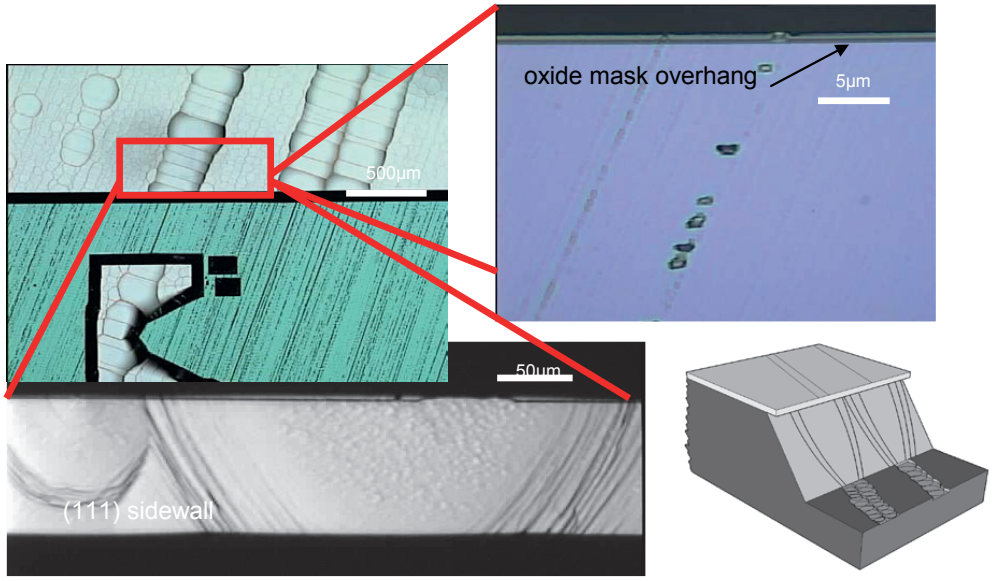


Fig 71. Greatly reduced undercutting and improved (111) surface smoothness in KOH-dipped ground wafer.

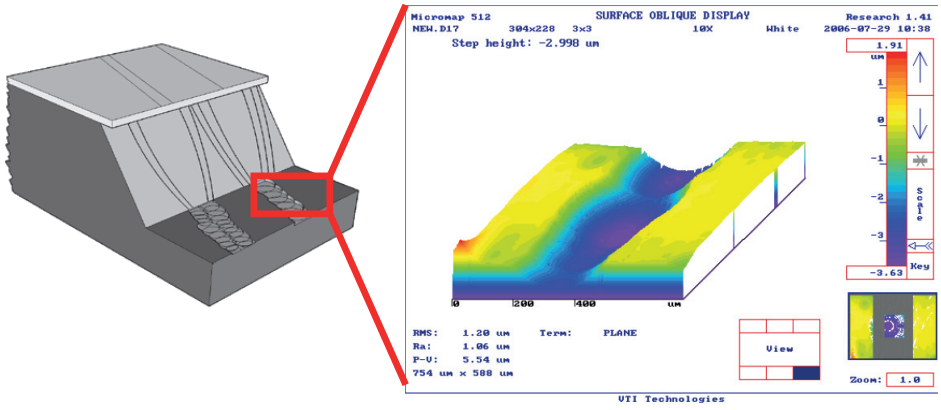


Fig 72. Optical profilometry map of a groove in the etched bottom (110 µm from the surface). Depth of the groove is about 3 µm. This is comparable to 4 µm depth measured for ground wafer. The width of the spherical depressions is from 200 µm to 300 µm. This is much wider than for the untreated case, and results from the deep KOH etching.

The spherical depressions seen in Figs 70 and 71 arise by preferential etching at certain points on the silicon (100) surface. The cause of this preferential etching can be traced to small edge dislocation loops which are associated with the mechanical grinding damage. KOH etchant penetrates into the cracks and, because there are many crystal planes open to attack in the crack, and some of them etch faster than the (100) plane, in [Haimi 2003] it has been shown that crystal defects can act as velocity sources in etching of the (100) silicon surface. Similarly, [van Veenendaal 2001 2] discussed that the fact that the depressions on the silicon (100) plane are spherical seems to imply that the (100) step velocity is isotropic. Monte Carlo simulations have shown that for a surface that is almost kinetically roughened, the step velocity is isotropic [van Veenendaal 2001 1].

The depth of the strain-inducing damage layer was studied by Haapalinna *et al.* [Haapalinna 2004]. Their results show that bow value goes to zero as the damaged layer is completely removed. This takes place at 0.2 µm removal for lightly damaged wafers while 0.6 µm is required for highly damaged wafers. The current study indicates that similar removal of the 0.6 µm damage layer is sufficient to achieve standard etch behaviour in KOH etching because KOH etches the damaged areas and damage spots very rapidly. The stressed grinding damage responsible for wafer bowing is also responsible for the high under-etch rate without removal.

Nanoindentation results of three wafers are collected in Table 14. In general, the treatments applied to the wafers induced little change in their mechanical properties. Indentation conditions were: Berkovich tip (130 nm nominal radius at top), three-segment indent cycle: Loading-holding-unloading in Load-control mode. No clear cut hardness or moduli results could be correlated with etch behaviour. This is probably due to the scale of the size of the defects which are smaller than the tip area. These indentation results also confirm that the ground wafers are mechanically very close to standard reference wafers.

Table 14. Nanoindentation characterization for the test wafers and reference wafer for a surface / sub-surface damage investigation from Aalto University, Department of Materials Science and Engineering.

	Contact depth (nm)	**Hardness (GPa)**	**Reduced modulus (GPa)**
Si-FG	51–104	11.0 ± 0.4	153.1 ± 3.9
Si-FGE	50–110	11.2 ± 1.0	157.3 ± 5.4
Si-R	50–100	11.4 ± 0.3	156.9 ± 8.0

Code	**Wafer state**	**Surface/sub-surface damage description**[1)]
Si-FG	Fine grinding / mid processing	Low surface roughness with sandwich damage layers down from top: amorphous Si (few nm) / Plastically deformed Si (~2µm) / elastically deformed (~2µm)
Si-FGE	Fine grinding + KOH etching / mid processing	Low surface roughness with sandwiched damage layers down from top: Plastically deformed Si (>1µm) / elastically deformed (~2µm)[2)]
Si-R	Reference wafer, Polished / ready for application	Very low surface roughness with unknown damage type and damage layer depth
Note	1) Damaged surface here refers to any surfaces in conditions other than as-grown / defect-free conditions 2) Assuming KOH etching removes completely the amorphous layer and about half of the plastically deformed layer	

7.2.2 Grinding damage elimination

It is shown that a short KOH dip can efficiently remove fine grinding damage. A stressed layer with grinding damage allows aqueous KOH to penetrate under the masking layer and local anomalies occur in the etching result. Removal of damaged layers by a surprisingly simple KOH dip results in wafers that are similar to prime polished wafers in their KOH etch behaviour. This includes both mask under-etching and (111) sidewall smoothness. However, it is possible to remove damage by thermal oxidation, too. If a thermal oxide 1.2 µm thick is grown, it consumes around 0.6 µm of silicon. When the oxide is etched away, a 0.6 µm damage layer is removed. However, this requires cleaning, long oxidation and wet etching.

Mechanically ground wafers have very good thickness control and very low TTV (total thickness variation) and in these respects they are even superior to polished wafers. This study indicates that, by simple removal of the damaged layer, ground wafers can replace polished wafers in certain MEMS applications where the quality of the etched bottom surface quality is not critical. This is highly beneficial since the production of mechanically ground wafers is simpler than the production of polished wafers. Both polishing tools and thickness sorting equipment can be eliminated.

7.3 Ultra Poligrind wafer as MEMS starting material

Ultra Poligrind wafers as MEMS starting material are used in this study. The result, when double side Ultra Poligrind wafer is processed to accelerometer seismic masses and spring beams, is shown here. Removal of grinding damage by a standard KOH etching mask oxidation process prior to MEMS structure etching and after MEMS structure etching is employed to recover high quality silicon. The results indicate that Ultra Poligrind grinding plus 1200 nm oxidation results in wafers comparable to polished wafers.

Double side grind (DSG) silicon wafers (300 µm thick) were used. Wafer diameter was 150 mm and type was P+(100) CZ silicon. DSG wafer grinding was made in two steps with a Disco DFG8540 grinding tool in Disco Hi-Tech Europe GMBH facilities in Munich, Germany. The starting material was 380 µm thick DSP wafers which were ground equally in both sides. In the first grinding step a Mesh 2000 grinding wheel (GF01-SD2000-V575-250 A2933) was used and grinding amount was 40 µm. In the second grinding step a Disco Ultra Poligrind wheel (PW08-UA0140-N0007) was used and the grinding amount was 10 µm. Wafer pretreatment was as described in 6.2 above.

KOH etching was carried out in multiple steps with the deepest and longest etching around 150 µm deep, taking about five hours. The target beam thickness was 18µm. Etching bath temperature and concentrations were accurately controlled to achieve required beam thickness control. Before KOH etching, the wafers were cleaned by SC1 cleaning process and rinsed in DI water. The etching solutions were mixed from

Honeywell PURNAL quality KOH and DI water. The temperature of the KOH solution was 65 °C and concentration 20 wt-%. These parameters were chosen because of high crystal plane anisotropy and low mask etch rate. In each run a full cassette of 25 wafers was etched. Rotational flow dynamic etching bath was used. In rotational flow bath, the cassette rotation speed of 27rpm and rotation direction change every 15 min were used. After KOH etching, the etched wafers and structures were oxidized by wet oxidation at 1050 °C. The thickness of the oxide was measured by ellipsometry to be approximately 1200 nm. Before anodic bonding 1200 nm wet oxide was removed in BHF etch step and rinsed and dried with IPA dip. The resulting seismic mass and beam are shown in Fig 1.

7.3.1 Grinding damage removal

A SEM picture of Ultra Poligrind wafer surface is shown in Fig 73, showing grinding lines and other scratches which, however, are very shallow. Particles on the surface are silicon and originated from the sample preparation.

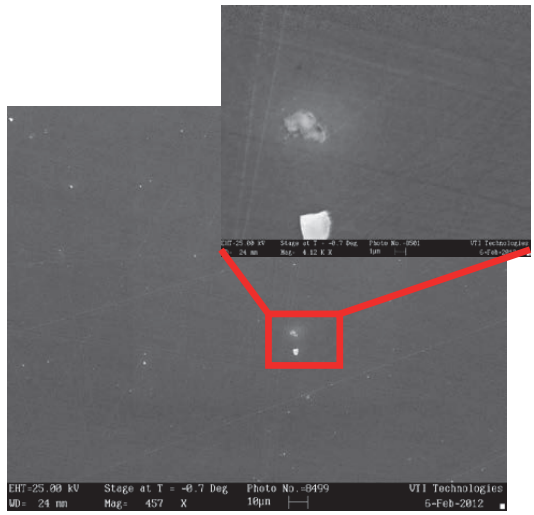


Fig 73. SEM picture of Ultra Poligrind wafer surface which shows shallow grinding lines and other shallow scratches.

AFM surface roughness analysis shows that the Ultra Poligrind surface roughness is about 4 nm Rq-roughness (about 3 nm Sa-roughness) in both 20 x 20 µm and in 10 x

10 µm measurement area. Fig 74 shows AFM 10 x 10 µm surface map and roughness analysis results.

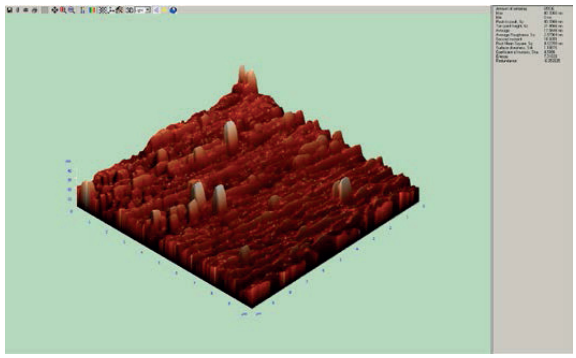


Fig 74. The Ultra Poligrind surface roughness is about 4 nm Rq-roughness (about 3 nm Sa-roughness) in 10 x 10 µm measurement area in the AFM analysis software tool, Nova map.

After about 1.2 µm oxidation process step and oxide removal, the AFM surface roughness analysis showed (Fig. 75) that the Ultra Poligrind surface roughness was decreased below 1 nm (in 10*10 µm measurement area Rq was 0.74*90 nm and Sa was 0.60 nm) in both 20 x 20 µm and in 10 x 10 µm measurement area.

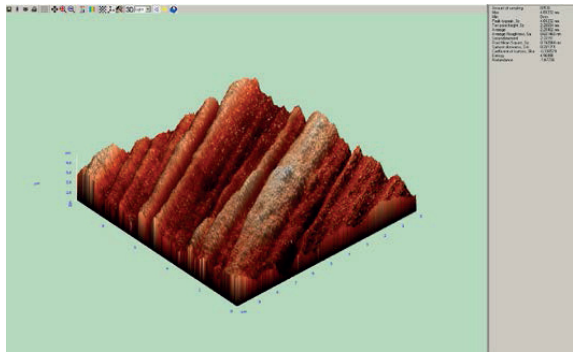


Fig 75. After about 1.2 µm oxidation process the Ultra Poligrind surface roughness is decreased below 1 nm in 10 x 10 µm measurement area in AFM analysis software tool, Nova map.

AFM surface roughness (Rq) measurement results of Ultra Poligrind grind wafers as a function of wet oxidation thickness are shown in Fig 76, which shows that the surface

roughness of Ultra Poligrind wafers decreases as a function of wet oxidation thickness. Surface roughness decreased from 4 nm (Rq) to below 2 nm (Rq) during 200 nm wet oxidation step. During the 1200 nm wet oxidation step, the surface roughness decreased from 4 nm (Rq) to below 1 nm (0.74nm Rq). The very same decrease in surface roughness value is seen when altogether 1400 nm wet oxidation is grown (200 nm WOX + 1200 nm WOX). The surface roughness of Ultra Poligrind wafer after 1400 nm wet oxidation was 0.71 nm (Rq).

AFM surface roughness (Rq) measurement results of two reference wafers are also shown in Fig 76. The first reference wafer was the wafer ground on the Disco Poligrind wheel, which is commonly used in the IC industry as ready IC wafers back side thinning before or after dicing. AFM measured surface roughness of the Poligrind wafer was about 9.3 nm (Rq). The second reference wafer was a CMP polished wafer, commonly used as a starting material in the IC industry. AFM measured surface roughness of the CMP polished wafer was 0.2 nm (Rq).

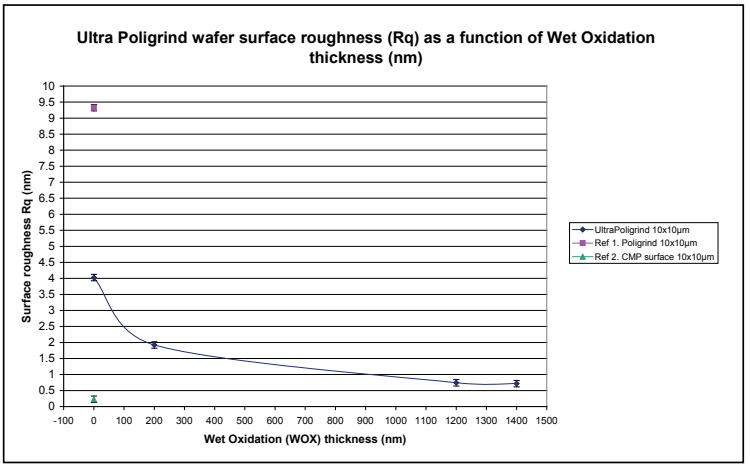


Fig 76. AFM measurement of surface roughness (Rq) of Ultra Poligrind ground wafers as a function of wet oxidation thickness. During the 1200 nm wet oxidation step the surface roughness decreases from 4 nm (Rq) to below 1 nm (0.74 nm Rq). The figure also shows the results of AFM measurement of surface roughness (Rq) of two reference wafers.

In the sensor element fabrication process, the KOH etching of the seismic masses and spring beams are made in three process steps. Fig 77 shows the etching results

beam dimensions (thickness, length and width) of these three process steps. The etching results for Ultra Poligrind wafers (Test) are compared with those for CMP polished wafers (Ref). The beam dimensions compared are the thickness, length and width of the beam. Comparison of the etching results shows that the performance of the Ultra Poligrind wafer is equal (within the error limits) to that of CMP polished wafers.

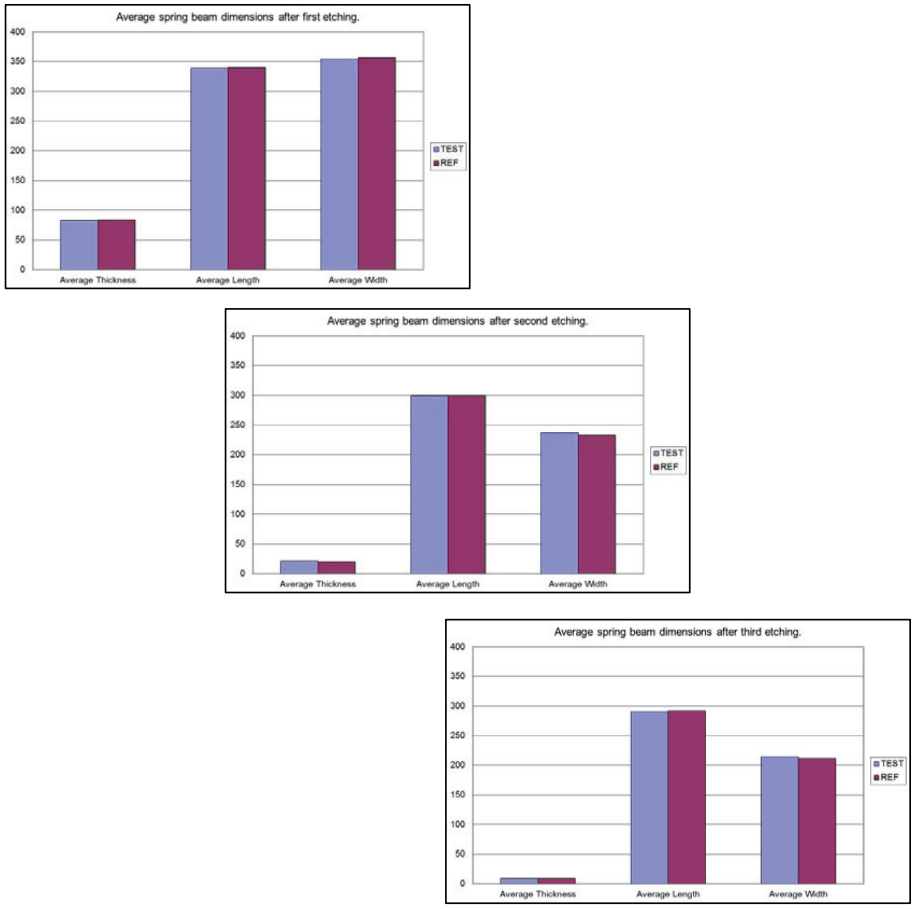


Fig 77. Etching results of Ultra Poligrind wafers (Test) compared with CMP polished wafers (Ref). Comparison of etching results shows that Ultra Poligrind wafers are equal (within the error limits) to CMP polished wafers.

After beam etching, the etched wafers and structures were oxidized by wet oxidation. The thickness of the oxidation was 1200 nm. Before anodic bonding, 1200 nm wet

oxide was removed in a BHF etch step and rinsed and dried with IPA dip. Figs 78a and 78b show anodic bonded Ultra Poligrind grind structure wafer which is bonded together with standard Murata Electronics Oy capping wafers. The bonded wafer was inspected by scanning acoustic microscope (SAM). Both bonded surfaces were inspected. Fig 78a shows the number 1 side bonded surface and Fig 78b shows the number 2 side bonded surface well bonded areas (dark grey) and non-bonded areas (white) can be seen in both figures. As the figure shows, non-bonded areas are in the sensor element cell and the outer edge of the wafers. All cell frames are well bonded as they should be when the bonding process is completed.

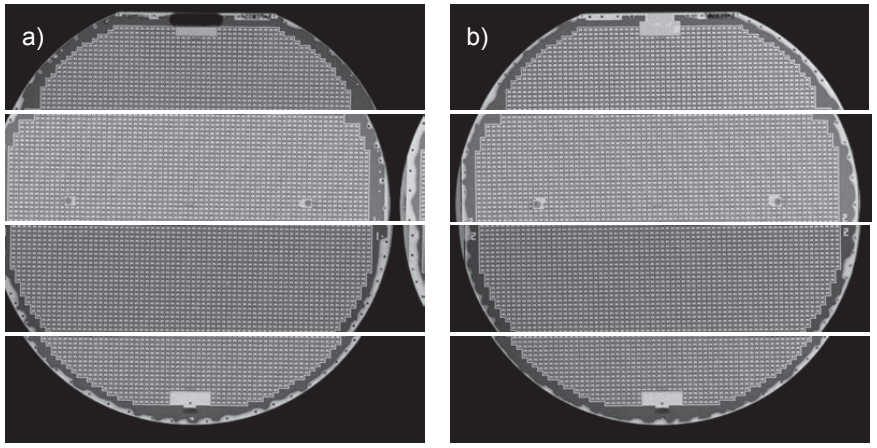


Fig 78. Scanning acoustic microscope images of the anodic bonded Ultra Poligrind grind structure wafer. (a) shows the number 1 side bonded surface and (b) shows the number 2 side bonded surface. Well bonded areas show as dark grey and non-bonded areas as white. As the figure shows, all cell frames are well bonded.

7.3.2 Grinding as replacement for polishing

It is shown that double sided Ultra Poligrind wafer is capable of being processed to make accelerometer seismic masses and spring beams. Removal of grinding damage by a standard KOH etching mask oxidation process prior to and after etching of the MEMS structures is employed to recover high quality silicon. The results indicate that Ultra Poligrind grinding plus 1200 nm wet oxidation results in wafers comparable to polished wafers. It is also shown that the results of etching MEMS structures onto Ultra Poligrind wafers are equal to those on CMP polished wafers. Furthermore, it is shown that the anodic bonding quality of an accelerometer structure wafer made from Ultra Poligrind starting material is equal to an accelerometer structure wafer made from CMP polished starting material.

Mechanically ground wafers have very good thickness control and very low TTV (total thickness variation), and in these respects they are even superior to polished wafers. This study indicates that Ultra Poligrind wafers can replace polished wafers in all MEMS applications where the highest standard of repeatability and device quality is demanded. An MEMS process flow with standard wet oxidation processes will transform the Ultra Poligrind wafer surface to equal that of a polished surface. This is highly beneficial since the production of mechanically ground wafers is simpler than the production of polished wafers. Both polishing tools and thickness sorting equipment can be eliminated.

8. Conclusions

Even though anisotropic KOH etching is well understood, there are slight differences in etch behaviour which arise from feature scale, wafer scale, batch scale and batch to batch variation. These differences in etching results cause a number of problems, like beam size and shape variation, leading to out-of-specification devices or, in the worst case, to non-functioning devices. By understanding and taking care of all the factors influencing silicon anisotropic etching in aqueous KOH solution, it is possible to achieve a stable and high performing process.

The present dissertation has introduced six different phenomena that influence the anisotropic etching of silicon in aqueous KOH solution. They are:

1) Etching temperature and KOH concentration
2) Etching equipment and agitation
3) Impurities in etching solution
4) Impurities in Si wafer
5) Surface finish of Si wafer and removal of defects - KOH dip
6) Surface finish of Si wafer and removal of defects - Ultra Poligrind

It is shown that the etch rate and anisotropy are extremely sensitive to detailed process conditions, process equipment and KOH flow. Rotational flow was shown to be superior to laminar flow in KOH etch bath. Without very careful control of temperature, KOH concentration and bath flow dynamics it is not possible to achieve stable etching results.

It is also shown that the etching rate and etching results are very sensitive to very small changes of Pb concentration (200 ppb to 300 ppb). After extended etching this seemingly minor difference in impurity level led to a 28 µm difference in beam length. Careful control of impurity levels in aqueous KOH, especially of Pb and also Cu, it is not possible to achieve stable etching processes.

The variation in anisotropy and etching results was studied as a function of oxygen level in crystalline silicon wafer. The results showed that the anisotropy, especially plane (111) etching rate and therefore the etching result, is very sensitive to the level

of oxygen in the crystalline silicon wafer. Change of oxygen level from 7 ppma to 15 ppma led to beam length change of 6%. Even more importantly, wafers with 10 ppma oxygen could not be used at all to make functioning devices because oxygen-originated crystal defects interfered with KOH etching so dramatically as to lead to incomplete etching.

A novel method for removal of grinding damage was presented and variation in etching results studied as a function of crystalline silicon surface finish. The results show that mechanically ground wafers with high accuracy of thickness and of total thickness variation (TTV) can be used as a starting material for KOH anisotropic etching to achieve high accuracy 3D structures. Use of mechanically ground wafers instead of standard polished wafers is potentially a major cost savings issue.

In the final study, double sided Ultra Poligrind ground wafers were processed to MEMS accelerometer seismic masses and spring beams. This study showed that Ultra Poligrind ground wafers can be used as a starting material for highly demanding MEMS structures. They were qualified both for KOH etching and we also demonstrated anodic bonding successfully. However, without Ultra Poligrind surface finish MEMS structures could not be bonded hermetically.

These six studies and the six different phenomena give comprehensive guidelines for silicon anisotropic KOH etching. They show that by using tightly specified variables it is possible to achieve the most uniform MEMS structures. The most reproducible MEMS structures at wafer level guarantee the most consistent MEMS device manufacturing. For example, in accelerometers this means that the temperature dependence or sensitivity to any torsion forces is similar in each device and the remaining minor differences can be adjusted by readout electronics.

Approaching the scale of NEMS structures, it is necessary to fully understand and control the process and material parameters, and the process equipment and material properties must be tailored. Evermore finer details need to be controlled. For example, surface roughness has to be kept very low in comparison to feature size. This optimization needs to address all other factors simultaneously, ranging from etchant purity to crystal orientation and defects. So far no attention has been paid to the issue

of oxygen concentration of the silicon wafer in NEMS fabrication. As shown by our experiments, this neglect can be fatal.

These six studies give a better understanding of different process parameters and information for MEMS material tailoring. These studies introduce the total control of KOH etching process and shows a way towards ultimate control in wet etch process. To succeed in process development or enhancement, it is crucial to be familiar with all the aspects of the process; materials, chemicals, equipment and costs. This dissertation provides a guidebook for silicon anisotropic KOH etching processes towards a total process control of bulk MEMS manufacturing.

It is time consuming and expensive to change the starting material or process equipment, or even an individual process step, for a product that is in production. Even though integrated sensors have not become as common as predicted, the fact that KOH presents a contamination danger for CMOS microelectronics, is limiting the use KOH. However, most of the results of this thesis can be applied directly to TMAH etching which is more acceptable in many fabs.

There are issues that were not covered in the thesis, but that could be further studied. Surfactants and alcohol additives could be beneficial for the production of a mirror surface finish, rectangular shapes without corner compensation, or even vertical grooves in (100) plane silicon wafers. It would also be interesting to automate KOH etching in order to reduce variation.

While existing products will benefit from the results presented in this thesis, alternative techniques like DRIE are promising when completely new devices are being developed. In some applications like comb-drives, KOH is not even an option. However, DRIE processes are not without limitations. There are steps that can be much cheaper using wet anisotropic etching, for instance, when the etchable area is large and DRIE rate is slow.

Wafers for new processes must fulfil a number of requirements. It is often difficult to introduce new materials because of limited supply. Ultra Poligrind approach

introduced in this work is attractive because it is fairly easy to implement, and applicable to almost all wafer types.

Last but not least, specifications for the levels of chemical impurities (Cu and Pb) in the KOH must be carefully specified. However, if this is not possible, one option is to purchase the etching chemical in larger amounts and to adjust the etching parameters to match the etching results from that particular chemicals batch.

9. References

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This dissertation explains the interactions between design rules, silicon wafer properties, process conditions and device performance. Central to the work is the study of batch etching of silicon wafers in KOH. This work gives guidelines for a highly uniform (across wafer, across batch and batch-to-batch) KOH etching process that is able to achieve the most identical MEMS structures in high volume manufacturing and even to approach the scale of NEMS structures (Nano Electro Mechanical Systems). In order to succeed in that kind of process development or enhancement, it is crucial to be familiar with all aspects of the process; materials, equipment and costs.

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