Department of Electrical Engineering and Automation

Effects of accelerated lifetime test parameters and failure mechanisms on the reliability of electronic assemblies

Jussi Hokka

Aalto University

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Effects of accelerated lifetime test parameters and failure mechanisms on the reliability of electronic assemblies

Jussi Hokka

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Abstract

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Abstract

This dissertation presents the results of accelerated reliability assessment methods employed on lead-free component board assemblies. Temperature cycling and mechanical shock tests are commonly used to assess the reliability of portable electronic products. Higher acceleration factors can be achieved by exposing the devices under test to higher loadings than those experienced in operation conditions or producing the loadings more frequently. Recently there has been an increasing interest towards the optimization of test parameters in order to minimize the time required for testing. However, if the effects of acceleration procedures, especially on solder interconnection microstructures, are not well-understood, misleading conclusions can be made that can lead to poor product reliability having disastrous consequences in the worst case.

The results of this work demonstrate that the highly accelerated test conditions can lead to excessive lifetime acceleration and misleading failure mechanisms. It is shown that relaxation of the residual stresses has a significant effect on the shock impact lifetime of component boards while the failure mechanism(s) do not change with the increased impact repetition frequency. Relaxation of the residual stresses in load bearing materials takes place during the time between the impacts. The extent to which they can operate affects the way how the stresses/strains in the solder interconnections develop during further impacts. Similarly, lifetimes and failure mechanisms of component boards under thermomechanical cyclic conditions are shown to be dependent on the accelerated test parameters. In the highly accelerated tests, the microstructural evolution (recrystallization) controls the propagation of cracks, while in the real-use conditions, significantly less microstructural evolution takes place and the rate of crack propagation through the solder is notably lower. Re-assessment of the standardised test parameters and lifetime prediction models is therefore necessary in order to achieve better correlation between test conditions and real-use conditions. This work discusses different ways of achieving this target.

Keywords electronic assembly, mechanical load, microstructure, recrystallization, shock impact test, solder interconnection, thermal cycling test, thermal load

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Tiivistelmä

Tässä väitöstyössä esitellään kiihdytettyjen luotettavuustestien vaikutuksia lyijyttömien kokoonpanojen luotettavuuteen. Lämpötilan vaihtelutestejä ja mekaanisia iskutestejä käytetään yleisesti kannettavien elektroniikkatuotteiden luotettavuuden arviointiin. Näiden testimenetelmien tarkoituksena on tuottaa samat vikamekanismit, jotka ilmenevät todellisissa käyttöympäristöissä, mutta huomattavasti lyhyemmässä ajassa. Suurempia kiihtyvyystekijöitä voidaan saavuttaa altistamalla testattavat kokoonpanot suuremmille rasituksille kuin mitä ne kokevat käyttöolosuhteissa tai tuottamalla rasitukset tiheämmin. Viime aikoina on ilmennyt kasvavaa kiinnostusta testiparametrien optimointiin, jotta voitaisiin minimoida aika, joka tarvitaan testien suorittamiseen. On kuitenkin huomioitava, että mikäli kiihtyvyystekijöiden vaikutuksia, erityisesti juoteliitosten mikrorakenteisiin, ei ymmärretä riittävän hyvin, voidaan tehdä harhaanjohtavia johtopäätöksiä, jotka voivat johtaa huonoon luotettavuuteen ja pahimmassa tapauksessa tuhoisiin seurauksiin.

Tämän työn tulokset osoittavat, että erittäin kiihdytetyt testiolosuhteet voivat johtaa liialliseen eliniän kiihtyvyyteen ja harhaanjohtaviin vauriomekanismeihin. Työssä on osoitettu, että jäännösjännityksillä on merkittävä vaikutus komponenttilevyjen elinikään iskumaisten kuormitusten alla vaikkakaan vauriomekanismi ei muutu toistotaajuuden muuttuessa. Jäännösjännitysten relaksaatio juotemateriaaleissa tapahtuu iskujen välisenä aikana. Se missä määrin relaksaatiota ehtii tapahtua vaikuttaa siihen miten rasitustilat juoteliitoksissa muuttuvat seuraavien iskujen kuluessa. Vastaavasti komponenttilevyjen eliniät ja vauriomekanismit ovat riippuvaisia kiihdytettyjen testiparametrien muutoksista termomekaanisten syklisten olosuhteiden alla. Erittäin kiihdytetyissä testiolosuhteissa mikrorakenteellinen evoluutio (uudelleenkiteytyminen) ohjaa vaurioiden etenemistä, kun taas todellissa käyttöolosuhteissa tapahtuu huomattavasti vähemmän mikrorakenteellista muutosta ja vaurioiden eteneminen juoteliitoksissa on huomattavasti hitaampaa. Standardoitujen testiparametrien ja elinikämallien uudellenarviointi on siten tarpeen, jotta voitaisiin saavuttaa parempi korrelaatio testiolosuhteiden ja todellisten käyttöolosuhteiden välille. Tämä työ käsittelee erilaisia tapoja tämän tavoitteen saavuttamiseksi.

Avainsanat elektroniikan kokoonpano, mekaaninen kuormitus, mikrorakenne, uudelleenkiteytyminen, iskutesti, juoteliitos, lämpökuormitus, lämpötilan vaihtelutesti

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Preface

This work has been conducted in the Electronics Integration and Reliability Unit under the Department of Electronics at Aalto University. The work was financially supported by two research projects, ‘Concurrent Reliability Testing’ and ‘Improved Methods for Reliability Assessment of Electronics’, which were funded by the Finnish Funding Agency for Technology and Innovation (TEKES), Academy of Finland, Efore, National Semiconductor, Nokia, Nokia Siemens Networks, NXP Semiconductors, and Salon Teknopaja.

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Leiden, the Netherlands, June 2014

Jussi Hokka

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List of Publications

This thesis consists of an overview of the following publications, which are referred to in the text by their Roman numerals.

I Hokka J., Mattila T. T., Li J., Teeri J., Kivilahti J. K., “A Novel Impact Test System for More Efficient Reliability Testing,” *Microelectronics Reliability*, 50, (2010), pp. 1125-1133.

II Hokka J., Li J., Mattila T. T., Paulasto-Kröckel M., “The reliability of component boards studied with different shock impact repetition frequencies,” *Microelectronics Reliability*, 52, (2012), pp. 1445-1453.

III Hokka J., Mattila T. T., Xu H., Paulasto-Kröckel M., “Thermal Cycling Reliability of Sn-Ag-Cu Solder Interconnections – Part 1: Effects of Test Parameters,” *Journal of Electronic Materials*, 42, (2013), pp. 1171-1183.

IV Hokka J., Mattila T. T., Xu H., Paulasto-Kröckel M., “Thermal Cycling Reliability of Sn-Ag-Cu Solder Interconnections – Part 2: Failure Mechanisms,” *Journal of Electronic Materials*, 42, (2013), pp. 963-972.

V Mattila T. T., Hokka J., Paulasto-Kröckel M., “The Reliability of Micro-Alloyed SnAgCu Solder Interconnections under Cyclic Thermal and Mechanical Shock Loading,” *Journal of Electronic Materials*, (2014), in print.

Author's contribution

Publications I-IV:

The research program was planned and the theoretical aspects were discussed by the author together with the co-authors. The experimental work was planned by the author and conducted by the author with help from research assistants. The author carried out the statistical analyses and the failure analyses. The theoretical explanations of the results were discussed in detail with the co-authors. The author wrote the manuscripts, which were then discussed in detail with the co-authors. The finite element modelling work in publications I and II was conducted by co-author Dr. Jue Li.

Publication V:

The author participated in the planning of the research, the failure analyses, interpretation of the results and preparation of the manuscripts. The main part of the manuscript was written by Dr. Toni Mattila.

Symbols and Abbreviations

AF	acceleration factor
BGA	ball grid array
CSP	chip scale package
CTE	coefficient of thermal expansion
CTF	cycles-to-failure
EBSD	electron backscatter diffraction
FBWS	full board width support
FE	finite element
FEA	finite element analysis
FEM	finite element method
FR-4	fiberglass-reinforced epoxy resin, flame retardant (type 4)
HVQFN	heatsink very-thin quad flat non-leaded
IMC	intermetallic compound
JEDEC	Joint Electron Device Engineering Council
MSM	magnetic shape memory
OSP	organic solderability preservative
PWB	printed wiring board
RT	room temperature (22°C / 295.15 K)
SEM	scanning electron microscope
SMA	shape memory alloy
SMD	surface mount device
SnAgCu	tin silver copper solder alloy
SnPb	tin lead solder alloy
TC	temperature cycle or thermal cycling
TEM	transmission electron microscopy
TS	thermal shock
TTF	time-to-failure

$\alpha_{package}$	CTE of package
α_{PWB}	CTE of PWB
ΔT	temperature difference between maximum and minimum temperatures
ε	normal strain

γ	shear strain
G	gravitational acceleration constant of earth (9.81 m/s^2)
h_{joint}	height of interconnection
h_{PWB}	height of PWB
L	distance from interconnection to centre of die
t	time
T	absolute temperature
T_H	homologous temperature
T_{mp}	melting point of the material
T_{use}	use temperature of the application

1. Introduction

The role of reliability engineering is generally somewhat unrewarding since it is invisible to most people and it does not very often get the credit it deserves. Reliability is usually noticed and getting attention only when a failure occurs and something goes wrong. Often this causes merely irritation to the user when for example a smartphone crashes, but in some cases reliability issues can have catastrophic consequences. A failure in automotive electronics can lead to life-threatening situations and a failure in spacecraft electronics can lead to the loss of equipment worth hundreds of millions. Financial damages are usually recoverable but human lives should not be risked due to poor reliability or disregard towards it. Consumers are also very conscious about reported reliability issues and companies can easily earn bad reputation that can persist for years or even decades leading to significant market losses. Boeing's 787 Dreamliner aircraft, for example, has suffered from reliability problems caused by its lithium-ion batteries, which has caused the company embarrassment and financial losses. Therefore it is extremely important that reliability assessments are conducted properly and that reliability results are well understood so that products will meet their reliability targets and expected lifetimes.

The functionality and performance of advanced electronic devices such as smart phones, laptops and tablet computers have increased significantly over the past few years. Customers demand constantly more versatile and more powerful devices which means that equipment manufacturers are forced to introduce new products on the market ever more frequently. This development has considerably decreased the time allowed for engineering and testing of new products. Electrical devices are frequently used in more challenging operation environments where devices can experience large changes in temperature, combined with mechanical shocks and vibrations. Therefore, to improve the reliability assessment of new technologies and electronic products the employment of more efficient testing methods has become ever more important [Mat10a, Kar12b]. Recently there has been an increasing interest towards the optimisation of test parameters to improve the test efficiency and to minimize the total testing time. For example, in thermal cycling tests the dwell-time can be easily altered in order to shorten

the test duration. However, too drastic changes in the parameters may cause fundamental changes in the failure mechanisms and, therefore, it is important to keep in mind that the failure modes and mechanisms should not change when the test parameters are changed to produce higher acceleration. Verifying the actual failure types is neglected in many studies and it is much too common to report only numerical results without detailed failure analyses.

There are many risks involved in accelerated reliability testing. The objective is to create the same failure modes that would occur under operation conditions but in a much shorter timescale. This is achieved by exposing the devices under test to higher loadings than those experienced in operation conditions or producing the loadings more frequently. It is highly important that the accelerated test conditions and test parameters are carefully defined so that they do not exceed the limits of the tested devices and materials producing unrealistic or misleading failure mechanisms and lifetimes. Many of the accelerated test methods are standardised and the test parameters have been formulated and established over the years. However, the shift from SnPb solders to lead-free solders has made comprehensive reliability reassessment necessary. The test parameters that have been determined and designed for eutectic SnPb solders might not be correct for lead-free solders and their reliability assessments. Re-evaluation of the test parameters and lifetime prediction models has consequently become necessary. In addition, it has become more and more common to tailor the solder composition for specific applications and operating conditions. For example, by lowering the silver content of the widely used Sn3.0Ag0.5Cu solder or by adding minor alloying elements, such as nickel or bismuth, reliability improvements can be sought either from decrease of the strength and elastic modulus of the solder or from modification of the properties of intermetallic layers. Therefore, gaining a wider understanding of the failure mechanisms under different loading conditions and what kind of solutions work for the extreme conditions is one of the primary objectives of the work to be discussed.

The focus of this dissertation is on clarifying the effects of (i) shock impact repetition frequencies on the lifetimes and failure mechanisms of high-density component boards and (ii) identifying the effects of thermal cycling test parameters to develop more efficient and meaningful methods of reliability assessment for electronic products (see Fig. 1). A novel shock impact test system is introduced in Publication I in order to have means to study the time dependency of shock impact lifetimes and failure modes. In Publication II the developed test system is used to study the effects of impact repetition frequencies (as defined in terms of the number of impacts per

second) on the lifetimes and failure mechanisms of high-density component boards. In publications III and IV the focus is on identifying the effects of (i) temperature difference (ΔT), (ii) lower dwell temperature and lower dwell-time, (iii) mean temperature, (iv) dwell-time and (v) ramp-rate on the lifetimes and failure mechanisms of ball grid array (BGA) component boards. In publication V the objective is to develop a better understanding of the commonly encountered failure mechanisms of portable electronic products and how the different solder compositions can lead to different lifetimes under the given loading condition. Attention is placed to the failure mechanisms under thermal cycling conditions and mechanical shock impact loading, and the reliability governing principles are investigated from the perspective of microstructures and mechanical properties of solder interconnections.

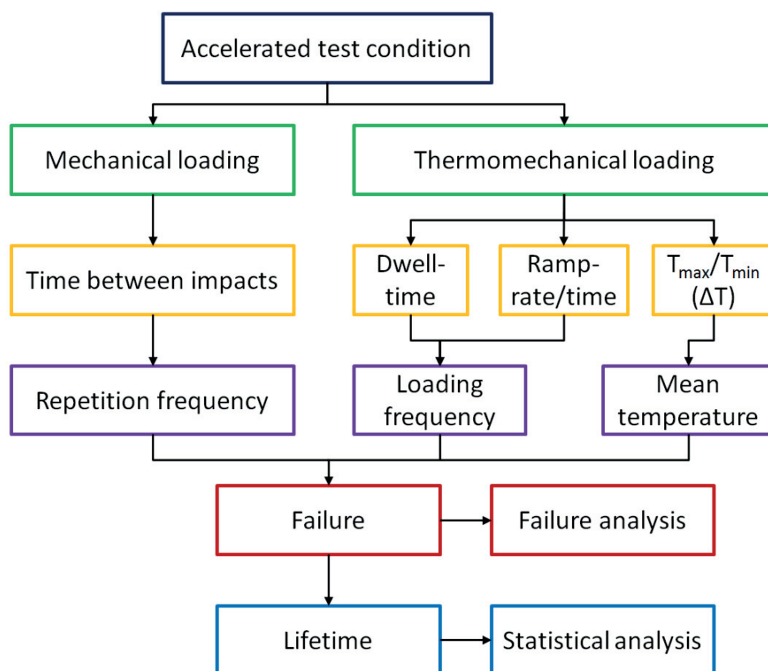

Figure 1: The studied effects of acceleration of shock impact and thermal cycling tests.

This dissertation is organised as follows. Section 2 gives an overview of shock impact reliability assessment methods (board-level and product-level conditions) and discusses the developed shock impact test method. Thermomechanical loading conditions are discussed in Section 3 with emphasis on the effects of thermal cycling parameters and the evolution of solder microstructures in the course of thermal cycling tests. Section 4 discusses the effects of minor alloying elements on mechanical properties of SnAgCu sol-

ders. Section 5 presents the main findings of the studies. Finally, Section 6 presents the conclusions and gives reasoning to the presented theses.

Based on the results and the accompanied analyses presented in this work, the following two theses are made:

1) **Drop impact reliability of component boards is time-dependent.** Even though the very high strain rate inherent in the drop tests strengthens the solder interconnections significantly, some plastic deformation takes place in the solder interconnections and leaves residual stresses in them (when the vibration has dampened and the board is at rest). Relaxation of the residual stresses in load bearing materials takes place during the time between the impacts and the extent to which they can operate affects the way how the stresses/strains in the solder interconnections develop during further impacts.

2) **Standardised thermal cycling tests can create failure mechanisms that are not seen in conditions representing real-use operation.** In addition to the growth and coarsening of intermetallic compound (IMC) particles and the primary tin cells, there are microstructural changes (produced by recovery and recrystallization) that are driven by the plastic deformation of solder interconnections. The significance of the microstructural changes depends on how much driving force (energy stored in the form of lattice defects) is produced under different thermal cyclic loading conditions. The onset of recrystallization and the kind of microstructural changes take place depend on how much of this stored energy is released by recovery and how much by recrystallization. Recrystallization is initiated only if the cyclic accumulation of stored energy is faster than its release by recovery. Under conditions representing real-use operation, the accumulation of stored energy is relatively low (modest plastic deformation of solder) and recovery releases majority of this energy while recrystallization is not initiated. On the other hand, under highly accelerated test conditions (significant plastic deformation) the driving force is accumulated faster than it is released by recovery, and therefore, recrystallization is initiated to assist the release of the stored energy. However, the initiation of recrystallization has significant consequences for the lifetime of solder interconnections, since the recrystallized microstructures fail more easily.

2. Mechanical Shock Impact Reliability

Modern portable electronic products experience various loadings in ordinary daily use but accidental drops are encountered perhaps most commonly. Over the past decade, the drop reliability of electronic assemblies has been studied by means of the travelling table test apparatuses described in the JESD22-B111 drop test standard (see [Jes03] for more details). Since equipment manufacturers introduce new products to the market more and more frequently, the time allowed for the designing and testing has considerably reduced. In order to improve the shock impact reliability assessment of new technologies and electronic products the employment of more efficient testing methods has become ever more important. However, while trying to achieve this target it is important to pay attention to how much reliability tests can be accelerated without producing misleading lifetime statistics or irrelevant failure modes and mechanisms. Therefore, in this work the effect of the shock impact repetition frequency on the reliability of electronic component boards was studied (see Publication II for details of test execution). Three shock impact repetition frequencies (0.01 Hz, 0.1 Hz, and 1.6 Hz) were employed to study the sensitivity of component boards lifetime to the time between the shock impacts and effects on their failure mechanisms.

2.1 Methods of shock impact reliability assessment

The loading conditions caused by drop of real products and those caused by accelerated reliability tests must be well understood. It is important to correlate the product-level drop test results with board-level drop test results. Product-level drop tests are, however, difficult to standardise due to different product designs and poor repeatability of tests. Therefore different commercial products have been studied in order to define the most important parameters that affect drop impact reliability. Based on these studies certain generalisations have been made and standardised test conditions that simulate real-use strains and stresses as realistically as possible have been defined.

2.1.1 Product-level loading conditions

Drop impact studies carried out with commercial portable electronic products have shown that impact forces generated when products are dropped onto the ground (causing a strong deceleration pulse) are transmitted through the product casing to the component boards and make the boards bend and vibrate at relatively high-frequencies of several hundred Hertz [Lim02a, Lim03, Mat14a, Ong03, Sea02, Tan05]. The high-frequency bending induces strains at the solder interconnections at very high strain rates. The loading conditions experienced by products are, however, highly dependent on factors like drop height, weight distribution, impact orientation, strike surface and design of their casing [Lim02a, Lim03, Ong03, Par09, Tan05]. Even though the shock impacts create highly complex bending motion of the component boards, recent investigations have shown that certain generalisations can be made on the impact forces, strains and accelerations. Studies by Lim et al. have shown that both vertical and horizontal impact orientations result in much larger impact forces (transmitted to the component boards inside the product casings) as compared to other drop orientations [Lim02a, Lim02b, Lim03, Tan05]. This is demonstrated in Figure 2, which shows a plot of impact force against impact angles for a portable device. In a vertical impact, the centre of mass of the product lies along the same vertical axis as the point of impact. When the impact forces are not in-line with the centre of mass (product falls on one of its corners), the device is not absorbing the full impact of the drop and the device has a tendency to rotate causing further collisions. This results in a lower impact force value, as well as, lower internal board acceleration. It is important to note that vertical orientations cause the highest impact force but horizontal impacts causes the most severe bending strains on component boards [Lim03, Tan05, Xu08]. The bending effect on the component board is most severe when the impact angle is 0° (see Fig. 2) causing the largest board deflection. This is one of the most important findings of the product-level tests and also the reason why many of the board-level shock impact tests are performed horizontally. Another important observation is that the first fundamental vibration mode of the board is critical in defining the loading conditions since the higher frequency modes and bending amplitudes dampen quickly [Tan05, Won05]. The results from product-level tests have been used to develop board-level drop test standards such as the widely employed Joint Electron Device Engineering Council (JEDEC) standard JESD22-B111, “Board level drop test method of components for handheld electronic products” [Jes03].

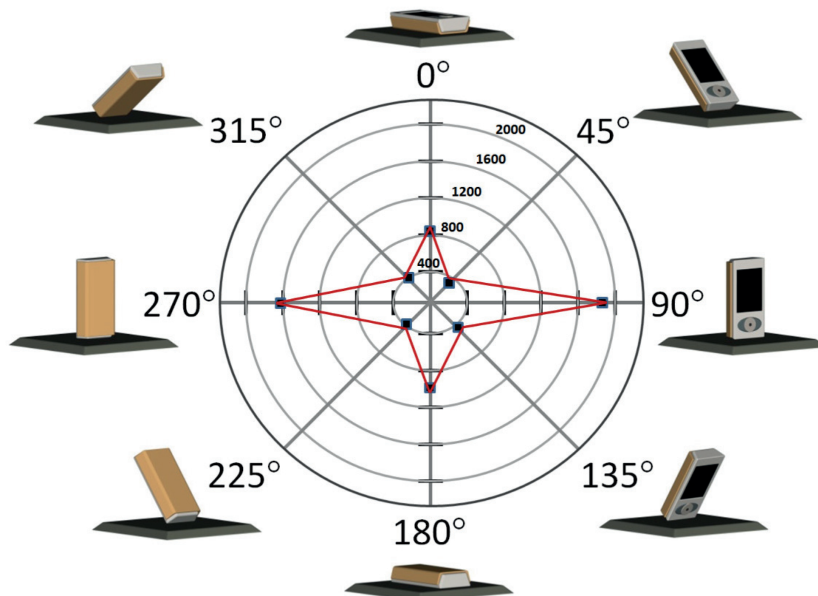

Figure 2: Plot of impact force (N) against impact angles for a portable device (adapted from [Tan05]).

In a study by Karppinen et al. [Kar12a] the correlation between board-level drop testing and actual drops of a modern handheld mobile device was investigated. The test results showed that, even though the test board design and supporting design method have a marked influence on the strain conditions and lifetime of solder interconnections, the primary failure mode and mechanism under the product-level drop tests is comparable to that typically encountered in the standard JESD22-B111 board-level drop tests. Their analyses suggested that the comparability of the shock impact loading conditions affecting solder interconnections can be characterized using three metrics: (1) the maximum component board strain rate, (2) the maximum board strain amplitude and (3) the damping of the component board. Therefore, it is suggested that the board-level drop test can be used as a suitable alternative to the product-level drop tests for handheld devices employing similar construction technologies and materials.

Figure 3 demonstrates the acceleration and strain histories of a mobile phone PWB after a product-level drop impact from 1.2 m height. The device was dropped horizontally display side downwards against a rigid strike surface (see [Mat14a] for details of the experiment). The acceleration measured from the top of the component board shows a primary pulse of ~6 000 G followed by two smaller secondary pulses (~1 000 G). The strain response of the component board is dampened by an order of magnitude within a few milliseconds after the impact. This timeline can be divided into two stages, which can be characterized as (i) forced bending and twisting of the com-

ponent board at the moment of the impact and (ii) free (resonance) vibration of the component board as initiated by the drop impact (see Fig. 4). The first stage is characterized by highly localized deformations near contact regions, where the device covers hit the ground and internal parts collide (e.g. the component board hits the battery or the display inside the device covers). The second stage is characterized by more uniform bending of the component board as dictated by the natural mode shapes and frequencies of the component board (the device bounces back and vibrates freely in the air). Strains caused by the forced bending during stage (i) are typically much higher and shorter in duration than those caused by the natural vibration of the board during stage (ii). The stress/strain conditions produced in the interconnection level of the component board under the high maximum strains and strain rates characteristic to the stage (i) are more likely to produce failures in the intermetallic layers of the solder interconnections, where as those characteristic to stage (ii) are more likely to produce bulk solder failures. Typically there is a significant difference in the expected lifetime of the solder interconnections depending on which one of these two failure modes is produced. The faster failure rate of the intermetallic layer cracking makes it a more critical failure mode and therefore it is also more preferred that board-level tests produce this type of failure.

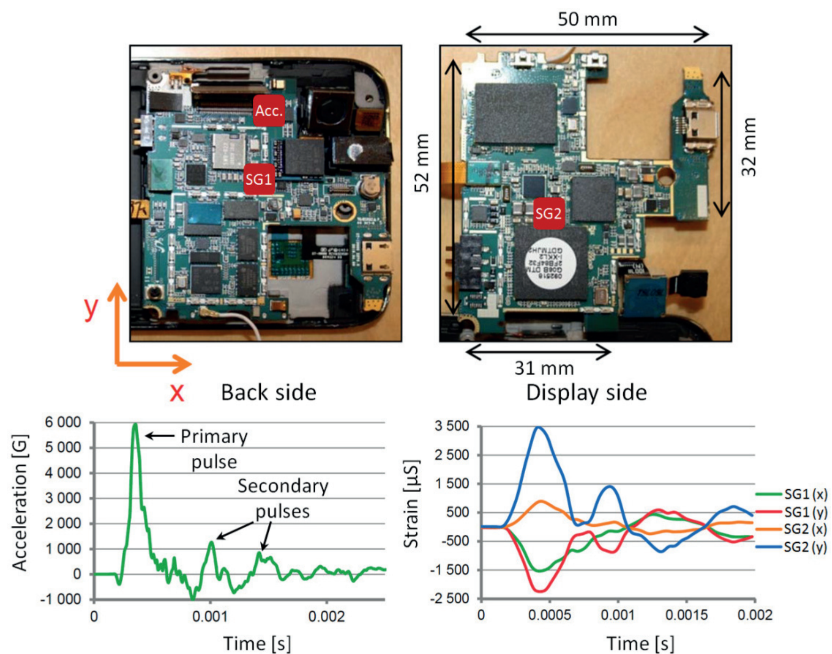

Figure 3: Acceleration and strain histories measured from a handheld device PWB under a product-level drop from 1.2 m height [Mat14a, Mat14b]. Accelerometer and strain gauge locations on the component board are indicated with the red squares.

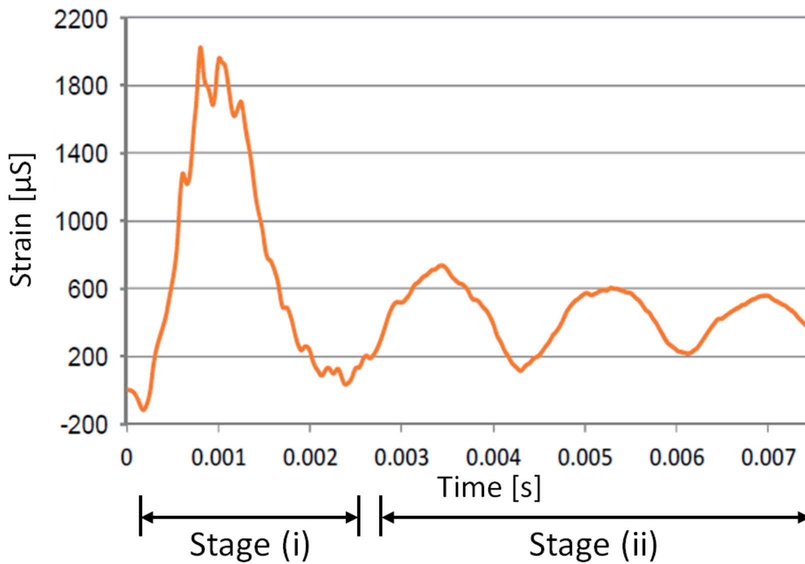

Figure 4: Measured component board strain response after a product-level drop impact divided in two stages: (i) forced bending and twisting of the component board at the moment of the impact, and (ii) free (resonance) vibration of the component board as initiated by the drop impact.

2.1.2 Accelerated board-level test methods

The reliability of electronic assemblies under shock impact loading conditions has been studied extensively by employing the JEDEC standardised drop test [see e.g. Lai06, Mat06, Won08, Won09]. This method aims to evaluate and compare drop performance of electronic components at the board-level in an accelerated manner without considering the effects of device covers or other adjacent structures. The method is widely employed because it was the first method to create a common drop test procedure for the consumer electronics industry. There are, however, many shortcomings related to the method of drop testing. First of all, lifetime assessment of component boards can be very laborious, because especially small components can last several hundred drops before a failure is recorded. This means that testing can be very time-consuming because of the inherently low impact repetition frequency (as defined in number of drop impacts per second) characteristic of the travelling table approach. In addition, the peak deceleration amplitude can vary from one drop impact pulse to another because packages placed at different locations on the component board experience dissimilar loading conditions, and thus the lifetime of a particular location can vary significantly from one board to another.

To avoid drawbacks related to the board-level drop test, some alternative approaches have been developed. Marjamäki et al. introduced a test method based on continuous harmonic vibration at the (lowest) resonance frequency of the component board [Mar06]. It has been shown that the method of vibration testing can initiate the same failure mechanism and produce the same failure modes as the previously described drop test method [Mat08, Mar07]. However, the correlation between the vibration cycles-to-failure and the drops-to-failure is still unclear. This is primarily related to the fact that vibration testing causes continuous harmonic vibration (constant amplitude) whereas drop testing causes quickly attenuating bending after which the board is at rest before the consecutive impact. Other accelerated board-level approaches include a high-speed cyclic bend test method in which the cyclic bending is performed at a frequency that is comparable to that experienced by the component board assembly in a typical portable electronic device [Sea06]. The benefits of this approach are that it offers a better reproducibility of the sinusoidal pulse and higher test throughput rate than the board-level drop test method. However, this method does not produce the gradually decaying oscillation which is experienced in drop impacts of electronic devices.

In order to produce discrete shock impacts on electronic assemblies and to overcome shortcomings of the JEDEC drop test method, the pneumatic shock impact test was introduced recently (see Publication I for details of the developed method). The essential advantage of this method is that one can control the impact repetition frequency of the tests and produce shock impacts with better repeatability as compared to the currently used drop test method. The control of the impact repetition frequency is needed in order to study how much one can accelerate the drop testing without producing misleading statistics and/or failure modes. The development of the pneumatic test method is discussed in the next chapter.

2.2 Development of a novel shock impact test method

As explained earlier, it had been previously shown that the failure mechanism, which takes place under the drop tests, can be initiated by harmonic vibration of the component board [Mar06, Mar07]. There are, however, a few aspects to consider related to the employment of the method: a) the significantly shorter testing time is a major advantage of the vibration test method but the correlation between the vibration cycles-to-failure and the drops-to-failure is still unclear, b) under certain circumstances, especially in cases where the weight of the package is relatively high, the inertia forces

of the component board can become significantly high, and c) tests carried out at elevated temperatures are a concern because even the ten-second period between the drop impacts (required to lift the travelling drop table) may allow a significant reduction of the stresses in the interconnections caused by faster creep relaxation at elevated temperatures [Mat08, Mat12a]. Therefore the development of a novel test method became the starting point for this dissertation since it was a much needed tool for the studies of sensitivity of lifetime on the impact repetition frequency. In addition, the new tool was desired to enable more efficient and cost effective reliability assessment of component boards. In the end, two alternative methods of implementation were considered: (a) acceleration method (executed with smart actuators) and (b) collision method (executed with either pneumatic actuators or linear motors).

The implementation of method (a) consists of four small actuators that would be placed on a rigid substrate and attached to the component board on the four corners. A simultaneous release of these four actuators would cause the load displacements (as in the collision based method of JESD22-B111 drop testing). Different type of actuators (see Fig. 5) that can produce motion and force with high repetition frequency were considered. Shape memory alloy (SMA) actuators are characterised by their ability to return to their original shape after heating to their transformation temperature. This is caused by a change in the crystalline structure during the transition from the martensitic phase to the austenitic phase. Magnetic shape memory (MSM) materials offer a similar way to produce motion and force. MSM materials produce a change in dimensions, shape or stress due to an applied magnetic field. However, the displacements of the currently available actuators were not close to the desired displacement range of about 4 – 6 mm. This range could be achieved with the help of displacement expanders but it was concluded that the force output of the actuators with the displacement extenders was not high enough for the intended purpose. Thus, the collision based method (b) was adopted instead and the pneumatic solution was the most suitable option to be implemented. This option is low-cost, robust, easy to use and easily maintainable. Main reasons for the rejection of the other alternatives were: smart actuators are expensive, their availability is still poor, and they are not yet advanced enough technique. Linear motors, on the other hand, are costly, the strike impact may destroy the motor, and they require frequent service.

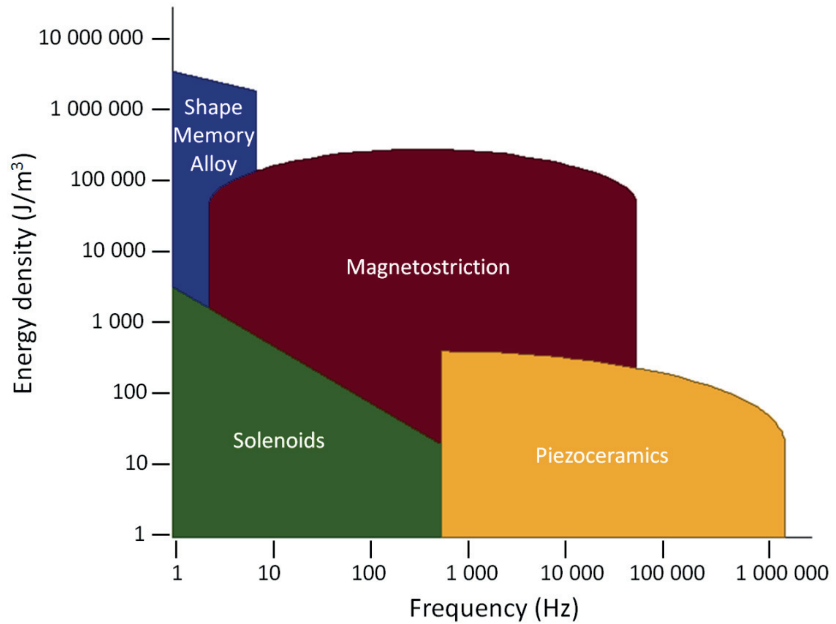

Figure 5: The alternative actuators that were considered for the acceleration method (a).

The pneumatic test system (see Fig. 6) consists of a pneumatic cylinder (1) with a piston (2) equipped with a shock absorber, a lightweight component board holder (800 g) (3), and a framework made of aluminium profile (4) attached to the top of a rigid strike surface (5). To stabilise the structure and to reduce excess vibration, the top plate of the framework (6) was made out of granite, and the side pillars (7) were drilled through the top and bottom stones. In order to achieve the desired shock pulse the strike surface was covered with a foam rubber sheet (8). A lightweight accelerometer (9) was attached on the surface of the component board holder to measure deceleration. The test system is operated with a control unit (10) that operates a valve and a pressure chamber (11) that controls the air flow and air pressure. A high-speed data acquisition system (12) is used to monitor the daisy-chain resistance of the component boards and to record the number of shock impacts to failure.

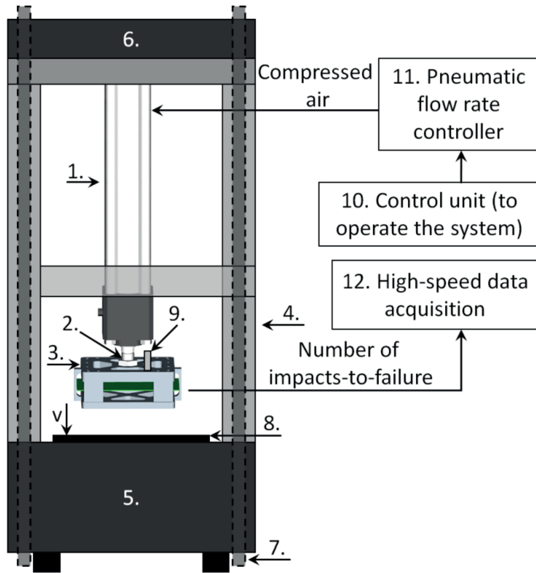

Figure 6: Schematic of the operating principle of the pneumatic test system.

Natural vibration modes of the test system were calculated with the help of finite element modelling (Abaqus). The six computational cases that were modelled are presented in Figure 7. The modelling results (see Table I) were used to modify the structure of the tester in order to shift the lowest natural frequencies of the tester as far away as possible from the frequency range of the 0.5 ms half sine impact pulse (1 kHz) and the printed wiring boards natural frequency (~ 220 Hz). The results showed that the most significant causes of vibration are related to bending of the top plate and bending of the support posts (see Fig. 8).

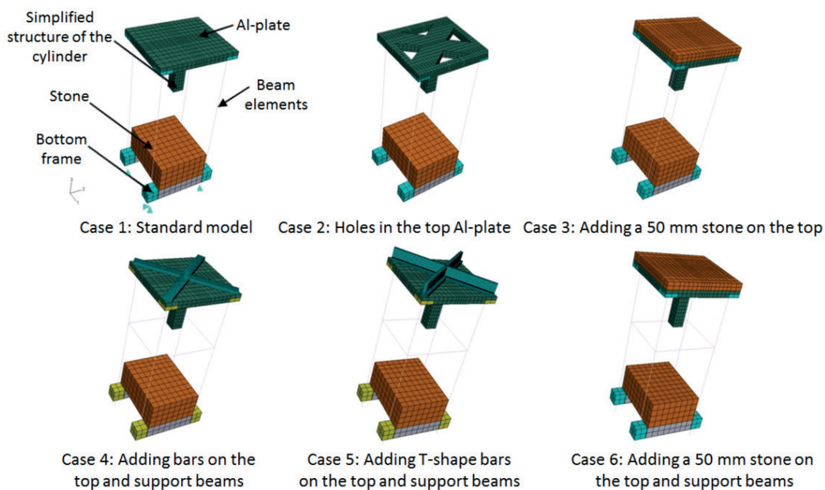

Figure 7: The six computational cases that were studied.

Table I: Results of the computational case studies.

Case study	Description	1st natural mode [Hz]	2nd natural mode [Hz]	3rd natural mode [Hz]	4th natural mode [Hz]
1	Standard model	298	440	446	559
2	Holes in the top Al-plate	280	440	446	555
3	Adding a 50 mm stone on the top	384	442	446	633
4	Adding bars on the top and support beams	314	558	715	1045
5	Adding T-shape bars on the top and support beams	346	581	652	1058
6	Adding a 50 mm stone on the top and support beams	380	633	1200	1383

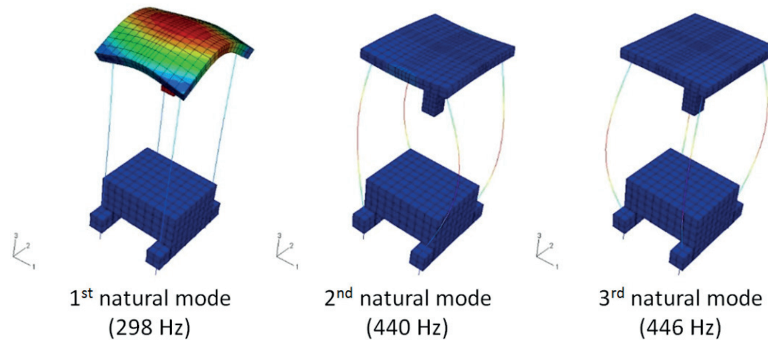

Figure 8: The most significant sources of vibration.

The tester can be set to produce the half-sine deceleration pulse as defined by condition B of the JESD22-B111 standard with a peak value of 1 500 G and a pulse width of 0.5 ms. The highest measured peak deceleration produced with the system was approx. 100 000 G. Figure 9 shows a measured shock impact pulse with a peak deceleration of about 35 500 G. The minimum time between the shock impacts is 0.63 s which equals to 1.6 Hz impact repetition frequency, as demonstrated in Figure 10.

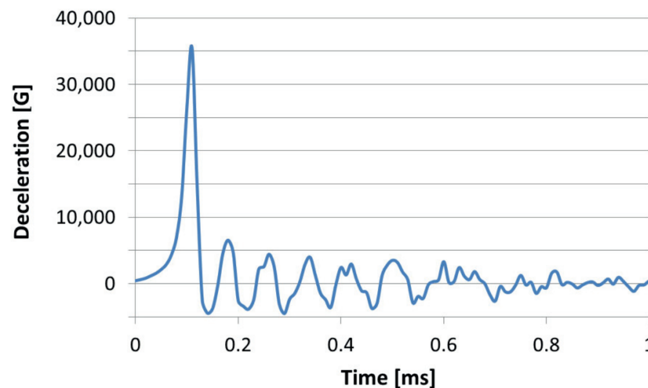

Figure 9: A measured shock impact pulse with a peak deceleration of about 35 500 G.

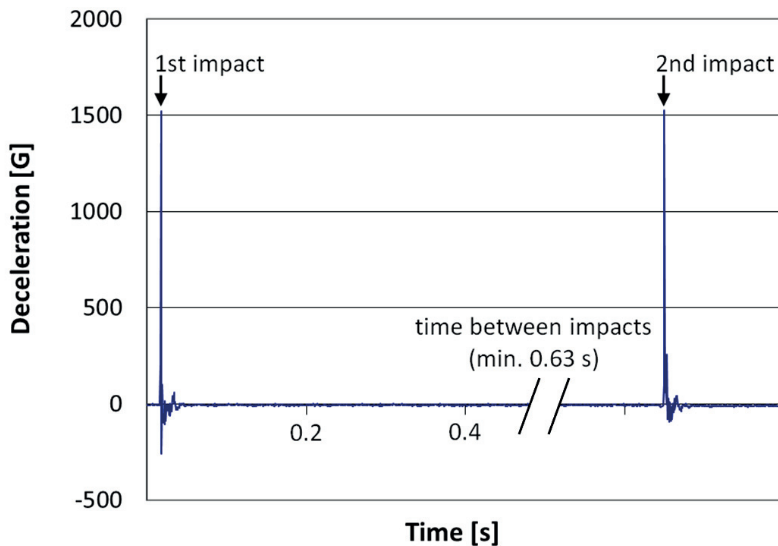

Figure 10: Two measured consecutive shock impacts.

2.3 Bending of component board and loading of solder interconnections

At the moment of shock impact the component board bends downward forced by inertia and oscillates with rapidly decreasing bending amplitude. Since the component board is allowed to bend freely, the total bending consists of several vibration modes and each of these modes vibrates at a characteristic frequency [Mar06]. The natural modes describe the shape in which the board bends, and the natural frequency describe how fast the bending takes place. The vibration modes and frequencies are determined by dimensions, materials, weight distribution and support of the component boards as well as the impact location and the force-time pulse. JEDEC-compliant component boards typically have their first natural frequency close to 200 Hz. The vibratory bending generates strains and stresses in the solder interconnections between the components and the printed wiring boards (PWB) and, thus, causes failures of the solder interconnections. Figure 11 shows an example of the measured longitudinal strain on the JESD22-B111 component board induced with a 1 500 G shock impact pulse (0.5 ms pulse width).

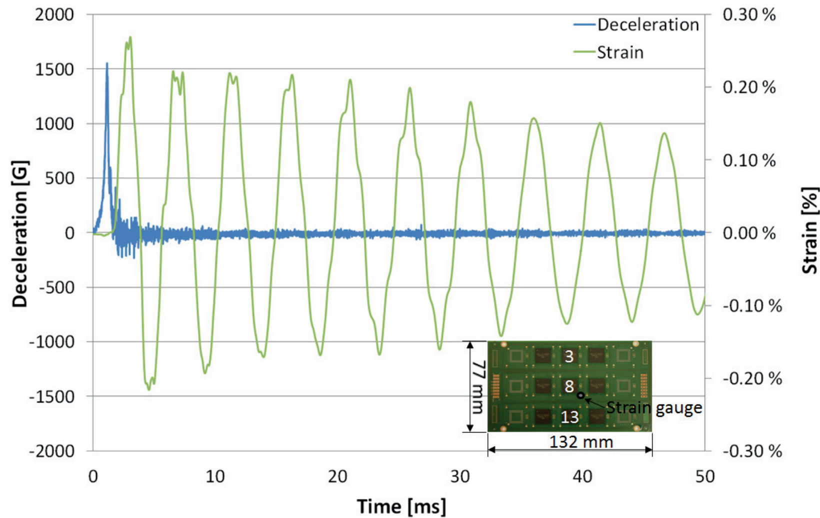

Figure 11: Measured deceleration and longitudinal strain at the centre location (8) on the JEDEC-compliant component board.

The shapes of the natural modes depend on the support structure of the component board. The total bending of the component board is the sum of the simultaneously vibrating natural modes that each vibrates at their characteristic frequency. In the JEDEC drop test (condition B) the duration of the acceleration pulse is about 0.5 ms, which corresponds to about 1 kHz frequency. Therefore, if the natural frequency of a mode is about 1 kHz or less, the mode is expected to affect the strain on the board after the drop impact [Mar07]. The natural modes with higher frequencies have usually a negligible effect to the measured longitudinal strains on the board since their participation factors (effective mass) are relatively small. The bending of the component board after the impact load (being supported from the four corners as described in the JESD22-B111 standard) is very complex due to the simultaneous action of the different vibration modes. This means that the strain distribution and the location of the highest stress in the solder interconnections change very rapidly. Therefore packages at different locations on the PWB experience highly unequal loading conditions. Figure 12 shows the two most effective natural modes of the JESD22-B111 printed wiring board (highest effective mass) calculated with the finite element method for the standard 4-point support conditions.

In order to simplify the component board bending during drop testing, the component board attachment based on full board width support was introduced in Publication I. The finite element calculations shows that under the full board width support conditions only one effective natural mode of vibration is initiated below 1 kHz. The calculated frequencies and the two most effective natural modes are presented in Figure 12. Note that the char-

acteristic frequency of the 1st effective mode is closely similar to the lowest effective mode under the 4-point support conditions but the frequencies of the remaining effective modes are much higher. Because vibration modes with higher frequencies are suppressed by the board supports, the strains and stresses in the solder interconnections of the components at different locations on the PWB are also more uniform. The experimental measurements showed that the lowest fundamental frequency is approximately 215 Hz under the full board width support conditions, and that that the differences between the strain values at different component locations are much smaller as compared to the 4-point support conditions.

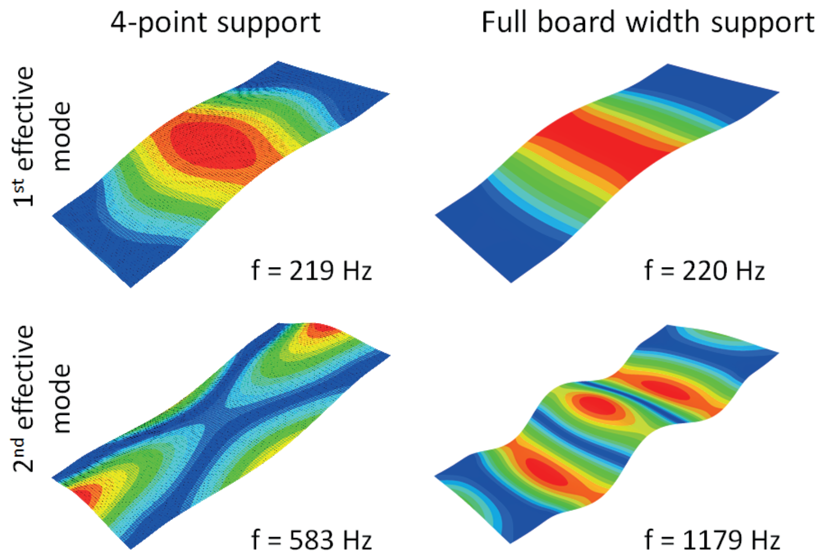

Figure 12: Two most effective natural modes of the component board as supported by the 4-point support and the full board width support. Contours represent vertical displacement. (See Publication I for more details)

Figure 13 illustrates bending of the component board when it is placed under shock impact loading. The bending causes displacement between the board and the component package inducing strain and stresses in the solder interconnections. The inertia forces of packages are typically negligible due to their relatively light weight (~0.3 g vs. ~3 mm^2 of contact surface to solder interconnections) and, therefore, the inertia of the components does not have a significant effect on the stresses at the interconnection level. The inertia of the entire component board is responsible for the vibrating motion after the shock impact. Under vibratory bending the solder interconnections on the package perimeters experience higher tensile than shear stresses. The relation between the shear deformation and the elongation of the edge interconnection is defined as

$$\frac{\gamma}{\varepsilon} = \frac{3}{2}\frac{h_{PWB}}{L} \tag{1}$$

where γ is the shear strain, ε is the normal strain, h_{PWB} is the height of the PWB, and L is the distance from the interconnection to the centre of the die [Mat11].

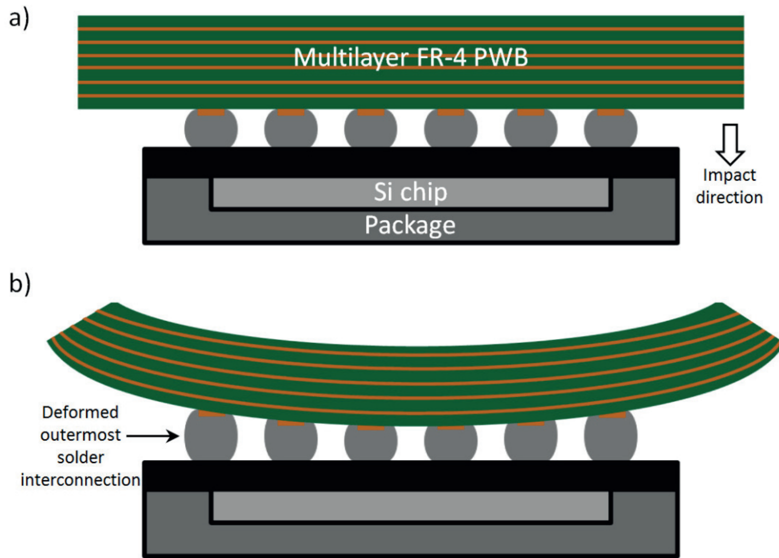

Figure 13: a) Component board at rest and b) displacements caused by bending of the PWB (after the shock impact).

2.4 Failure physics

One important difference between shock impact tests and thermal cycling tests is the deformation rate. Shock impact tests are typically conducted at room temperature, which is relatively high as compared to the melting point of the commonly used SnAgCu solders (0.6 in terms of homologous temperature). At high homologous temperatures ($T > 0.4\ T_{mp}$) the plastic behaviour of the solder is strongly strain rate dependent. Because the strength of solders increases strongly with increasing strain rate and decreases strongly with increasing temperature [Ama12, Dar92], the stress levels in solder interconnections are significantly higher in drop tests than in thermal cycling tests. Due to the increase in the stress levels the IMC layers will experience significantly higher stresses. The increase in the stress levels leads to the observed differences in the crack paths since the tensile strength of the solder increases above the fracture strength of the IMC

which makes the cracks propagate mostly in the IMC layers. Strains and stresses concentrate at the corner regions of the interconnections where fractures propagate through the Cu_6Sn_5 reaction layer. In thermal cycling, on the other hand, the strain rates are relatively low. Cyclic thermomechanical loading generates plastic deformation, which leads instead to propagation of fatigue cracks through the bulk of the solder interconnections. [Mat05, Mat06] Figure 14 shows a common failure mode observed in a shock impact tested BGA component board.

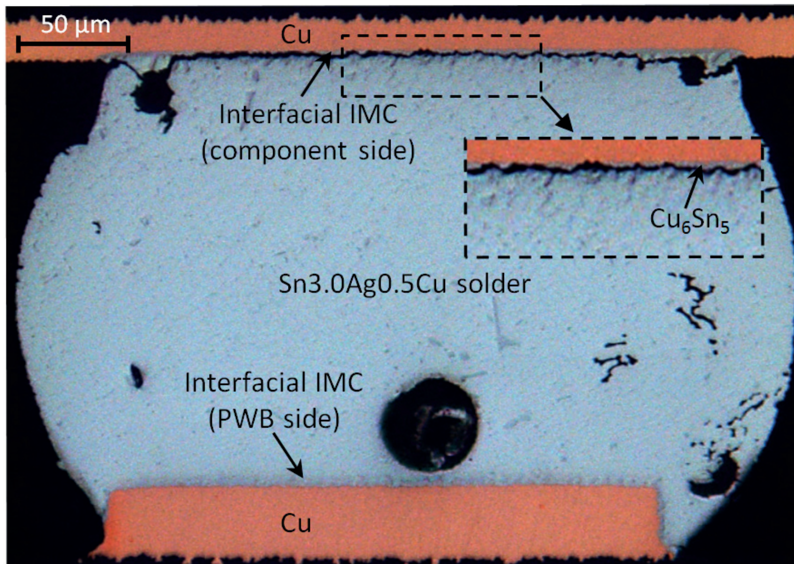

Figure 14: A common failure mode in a shock impact tested BGA solder interconnection in which the crack propagates through the Cu_6Sn_5 reaction layer.

Thus, when the shock impact reliability of solder interconnections is being studied, it is of extreme importance that testing conditions are close to those of the loading conditions of real products: loading magnitude, temperature, and loading rate. Otherwise the mechanical behaviour of solders in tests may differ from that in use, and the loading may be overestimated (or underestimated) producing misleading lifetime statistics and/or failure modes. This specific problem has been studied in Publication II. The time between shock impacts was varied between 0.63s and 100s in order to clarify the effects of impact repetition frequency on the lifetime and failure mechanisms of electronic component boards. The time between impact values were chosen to represent three different conditions; 0.63s represents the shortest possible time between impacts producible with the pneumatic test system, 10s represents the typical time between impacts of the JEDEC standardised drop testers, and 100s represents the longest realisable (from a practical point of view) time between impacts where time-dependent mechanisms are expected to be effective.

3. Thermomechanical Reliability Assessment

Electronic devices experience significant changes in temperature during normal operation due to changes in both their internal temperature (heat dissipation) and the ambient temperature. As component boards are exposed to temperature changes, strains and stresses are concentrated in the solder interconnections due to the mismatch of coefficients of thermal expansion (CTE) of the various component board materials. Thermomechanical reliability is typically characterized by performing standardised thermal cycling tests in which various parameters such as dwell-times, ramp-rates and temperature extremes are used to accelerate the loadings that electronic devices experience during normal operation. However, it is of extreme importance that failure modes and mechanisms observed under accelerated conditions are realistic and correspond with those seen in normal operating conditions.

3.1 Thermomechanical loading conditions

The standard thermal cycling tests extend the temperature range of electronic devices under normal operating conditions in order to accelerate the accumulation of failures. The extreme temperature ranges are typically between -45°C and +125°C but in some of the standards even between -60°C and +150°C [e.g. Iec09, Ipc07, Jes04, Jes05, Mil02]. Thermal cycling is a typical example of a strain-controlled cyclic loading, where the temperature range and the CTEs of adjoining materials dictate the level of stresses produced in a structure. CTE of the most commonly used printed wiring board (PWB) material, FR-4, is about 16-17 x 10^{-6}/°C [Coo01], whereas that of silicon is 2.5 x 10^{-6}/°C [Tou75]. As the component boards are exposed to changes in temperature, strains and stresses are concentrated in the solder interconnection between the packages and the PWB, as the natural expansion/contraction of the PWB is restricted by the packages (see Fig. 15).

In order to simplify the analysis for this work, it is assumed that the thermomechanical loads are mainly shear loads. In addition there are im-

portant bending modes (warping) and different expansion coefficients in different joints due to anisotropic crystallographic effects. This complexity will be neglected to simplify the analysis, but it would make an important topic for a future study.

Since the package and board expand by different amounts, the amount of shear strain (γ) can be approximated by the equation

$$\gamma = \Delta T \left(\alpha_{PWB} - \alpha_{package}\right)\frac{L}{h_{joint}} \quad (2)$$

where ΔT is the difference between the extreme temperatures, $\alpha_{package}$ and α_{PWB} are the CTEs of the package and the PWB, h_{joint} is the height of the interconnection, and L is the distance from the interconnection to the centre of the die.

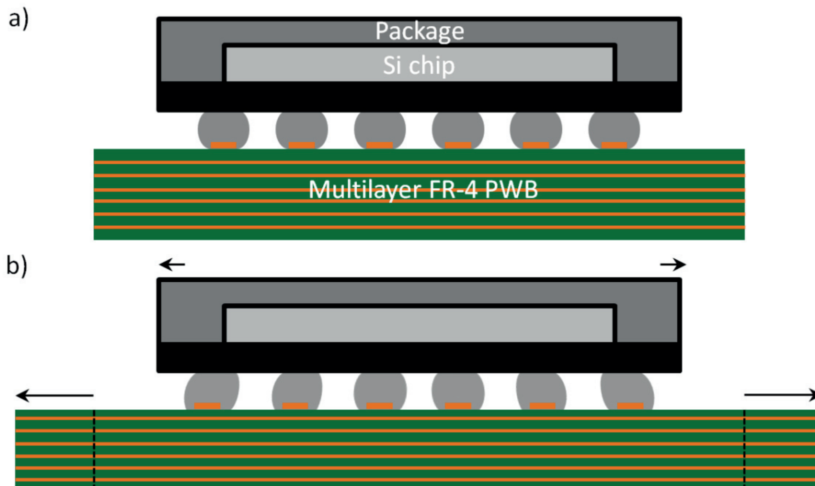

Figure 15: a) Component board at rest and b) displacements caused by thermal cycling.

The mechanical properties of materials are temperature-dependent. This is extremely important for solder interconnections since thermomechanical strains and stresses concentrate in the interconnections and deform the solder. The temperature range of operation is relatively high in many electronic devices (e.g. 25°C – 100°C [Kar10]), which equals to 0.60 – 0.76 homologous temperature ($T_H = T_{use}/T_{mp}$ in Kelvin) of SnAgCu solders. This means that creep processes will contribute to plastic deformation of solder interconnections during thermal cycling. Since creep rate of solder interconnections is temperature dependent, the amount of plastic deformation in solder interconnections depends on the temperature region of a thermal cycle. At low homologous temperatures the cyclic stress / strain relation-

ship forms a symmetric hysteresis loop as demonstrated in Figure 16. The area of the hysteresis loop represents the plastic work done on the material, the width of the loop represents plastic strain range, and the elastic strain range is given by the difference between the total strain and the plastic strain. At high homologous temperatures the strength of solder interconnections is lower and the creep is much more efficient. This means that the shape of the hysteresis loop changes. In standardised thermal cycling tests, the extreme temperatures are typically set at -45°C and +125°C, which equals to 0.5 – 0.8 in terms of homologous temperature. The difference in the yield strength and creep rate of solder interconnections is notably different at each extreme temperature. As a result the hysteresis loop becomes asymmetric with the maximum stress values at high temperatures being significantly smaller than those at low temperatures. Therefore, more plastic deformation takes place in the high temperature part of the cycle and bending of the PWB is less significant compared to bending at low temperatures. The plastic deformation in the most highly stressed regions of solder interconnections results in localised evolution of solder microstructures which ultimately leads to cracking through the bulk of the solder interconnections.

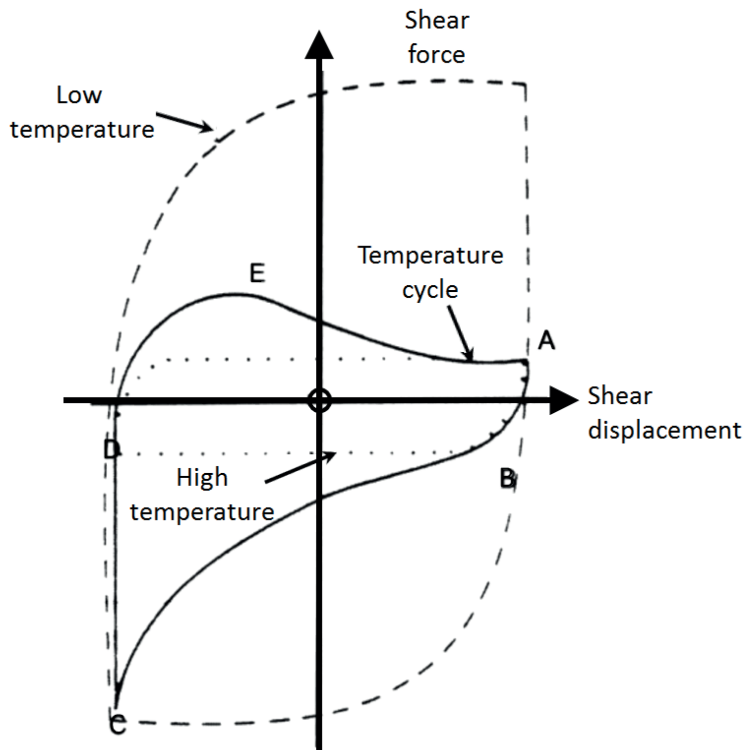

Figure 16: Stress–strain hysteresis loop of solder interconnections under isothermal cyclic loading and at thermal cycling [Hal84].

3.2 Effects of thermal cycling parameters

Accelerated thermal cycling tests are most commonly used to study the effect of thermal changes to assess the reliability of electronic products. Several different combinations of temperature differences (ΔT), extreme temperatures, dwell-times, and ramp-rates are used to control the acceleration factor of the thermal cycling tests. Figure 17 shows the dependency of different setup parameters. However, many of the standards and guidelines that define these test parameters have been formulated over several decades ago for SnPb solders, and they may not be applicable to today's small scale lead-free solder interconnections. It is worth considering, for example, if there is a need to use different extreme temperatures in lead-free thermal cycling tests since for SnAgCu the 0.5 homologous temperature equals about -28°C whereas for SnPb it equals about -45°C. This value is typically used as the lower temperature in thermal cycling tests. Similarly other test parameters might need revision as well. Thermal cycling tests are also costly to execute because of the direct expenses related to testing and as a result of the increased time to market of new products because of the time-consuming execution of the tests. Therefore, updates to the currently employed thermal cycling tests have become ever more essential.

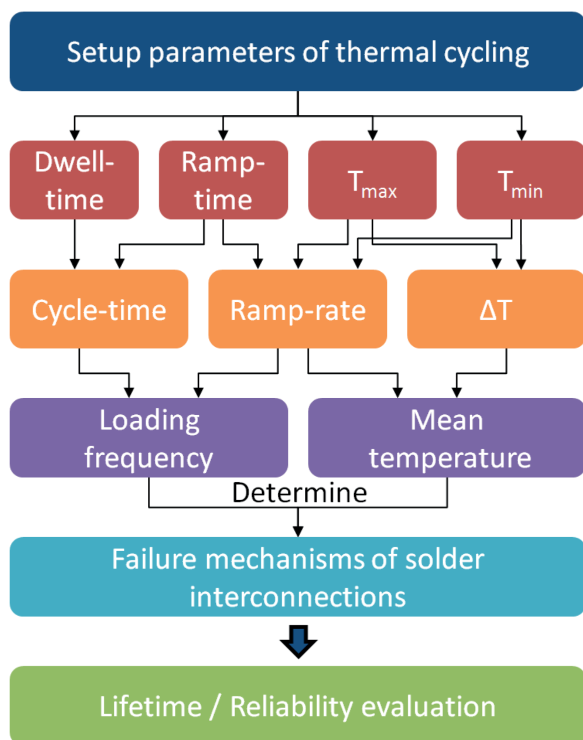

Figure 17: Dependence relationship of thermal cycling parameters.

Figure 18 shows the test matrix that was used to evaluate the effect of thermal cycling parameters on solder joint reliability (see Publications III and IV for more details). Table II presents details of each of the studied profiles. It is noteworthy that a wide range of thermal cycling profiles are needed to study the effect of each parameter individually since almost any change in one parameter (e.g. ramp-rate, dwell-time, ΔT) produces a change in a profile characteristic.

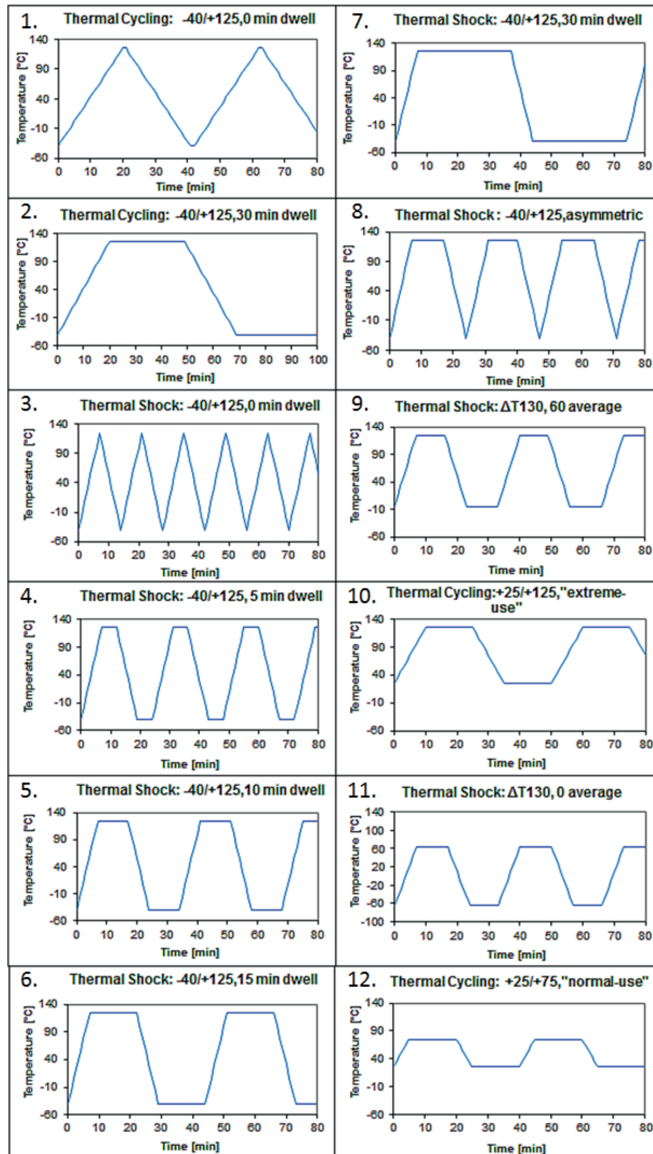

Figure 18: Test matrix that was used to study the effects of thermal cycling parameters. Table II indicates details of each profile.

Table II: Thermal cycling conditions that were used study the effects of test parameters. The different profiles are identified with codes that indicate the test condition: 1) ramp-rate [TC for temperature cycling (< 20°C/min) and TS for thermal shock (>20°C/min)], 2) temperature difference between the two temperature extremes [ΔT], 3) time-weighed temperature of the cycle, and 4) dwell-time.

Thermal profile	Lower dwell [°C]	Upper dwell [°C]	Dwell-time upper / lower [min]	Ramp-rate up / down [°C/min]	Total cycle time [min]
1. TC165-42.5C-D0	-40	125	0 / 0	8 / -8	42
2. TC165-42.5C-D30	-40	125	30 / 30	8 / -8	102
3. TS165-42.5C-D0	-40	125	0 / 0	24 / -24	14
4. TS165-42.5C-D5	-40	125	5 / 5	24 / -24	24
5. TS165-42.5C-D10	-40	125	10 / 10	24 / -24	34
6. TS165-42.5C-D15	-40	125	15 / 15	24 / -24	44
7. TS165-42.5C-D30	-40	125	30 / 30	24 / -24	74
8. TS165-76C-D10/0	-40	125	10 / 0	24 / -24	24
9. TS130-60C-D10	-5	125	10 / 10	26 / -26	30
10. TC100-75C-D15	25	125	15 / 15	2 / -2	130
11. TS130-0C-D10	-65	65	10 / 10	26 / -26	30
12. TC50-54C-D24/14	25	75	24 / 14	4 / -2	75

3.2.1 Dwell-time

Results reported in the literature often compare dwell-times with large time differences, e.g. 10-minute dwell-times are compared to above 30-minute dwell-times [Bat05, Sha02]. Comparisons of shorter dwell-times or smaller differences between the studied dwell-times are mostly available from studies carried out with SnPb solder [Hu06, Pan05]. It is also noteworthy that materials and packages vary a lot between different studies and therefore results of experimental investigations with comparable materials are scarcely available. The review to the published literature showed, however, that the conclusion on the effect of dwell-time is not unanimous. In Clech's study [Cle05] the optimum dwell-time of 10 minutes was suggested for SnAgCu BGA assemblies. The optimum dwell-time was based on simulations looking for the highest damage rate. Zhai et al. [Zha03] recommends 8-10 min dwell-time at the high temperature of 125°C based on their experimental and modelling results. They also state that with dwell-times beyond 20 min the effect on the acceleration factor becomes insignificant since the dwell-time is long enough for the stresses to stabilise. Some studies [Fan05, Man08, Sah03] on the other hand have suggested that increasing the dwell-time will decrease the lifetime. Sahasrabudhe et al. [Sah03] reported that their results revealed a strong dwell-time dependency on the initiation of failures with longer dwell-times leading to earlier failures than shorter dwell-times. Similarly Fan et al. [Fan05] reported that the fatigue life of

solder balls decreases significantly when the dwell-time increases from 15 minutes to 30 minutes. They state that the longer dwell-time cause more creep in the solder interconnection, and thus, the fatigue life is significantly decreased. Manock et al. [Man08] compared 10, 30 and 60 dwell-times with 10 minute ramps between the temperature extremes (0 ºC / 100 ºC). They reported that increasing the dwell-time leads to a decreasing characteristic lifetime in cycles-to-failure. However, the effect of the dwell-time is opposite when their results are expressed in hours-to-failure. In that case, the lifetime increases significantly with the increasing dwell-time. Therefore, conclusions should be made carefully since the used structure / geometry of the package, PWB and solder composition affect the results significantly.

3.2.2 Ramp-rate

A review to the published literature related to studies on the effects of ramp-rate [Cle05, Dus05, Fan05, Gha01, Lau05, Qi06] revealed that some disagreement exists about the effects of ramp-rates but majority of authors seem to agree that increased ramp-rate decreases the number of cycles-to-failure. The differing opinions are mostly related to the significance of the effect. Qi et al. [Qi06] observed in their study that the higher ramp-rate (95°C/min) caused more damage per cycle than the lower ramp-rate (14°C/min). Ghaffarian [Gha01] observed in his study that the thermal shock conditions (10 to 15°C/min) required considerably less cycles-to-failure than the temperature cycling conditions (2 to 5°C/min). Lau et al. [Lau05] reported consistent findings indicating that the number of cycles-to-failure under the thermal shock conditions is smaller than that under the temperature cycling conditions. This difference is explained by the larger change in the maximum creep strain energy density per cycle under the faster ramp-rate conditions.

3.2.3 Mean temperature

Studying the effects of different thermal cycling parameters can be can be problematic due to the fact that almost any change in one parameter (e.g. ramp-rate, dwell-time, ΔT) produces a change in a profile characteristic (e.g. load reversal frequency / cycle-time or average temperature) that influence the failure mechanism or accumulation of failures (see Fig. 17). However, effects of the mean temperature can be studied without changing the profile characteristics. For some reason, mean temperature effects are

not widely studied or these results are reported scarcely. Some results have, however, been reported in the literature and they indicate that test conditions with higher mean temperatures leads to significantly shorter lifetimes than test condition with lower mean temperatures (e.g. [Bou08, Sch03]). The significant difference in the lifetimes is related to the effect of temperature on the mechanical properties of solder. The stress/strain hysteresis loops of the solder interconnections produced by changes in the mean temperatures are also different. Under the higher mean temperature the strain range (loop width) is higher but the stress range (loop height) is smaller as demonstrated in Figure 19. Since the strain and stress ranges evolve in opposite directions it is most likely that the area of the hysteresis loop (accumulated strain energy density) is different in different mean temperatures. Since the strain and stress ranges evolve in opposite directions at different rates, it is possible that there exists a maximum for some intermediate value of mean temperature at which solder interconnection lifetime is minimised. Clech [Cle05] has studied the mean temperature effects with a fixed temperature difference of 70°C in a stress/strain analysis for solder joints hysteresis loops (see Fig 19). The mean temperatures varied between -15°C and 85°C. Clech suggests that a minimum lifetime for the SnAgCu solder interconnections exists when the mean temperature of a thermal cycling profile falls in the range of about 50°C to 65°C.

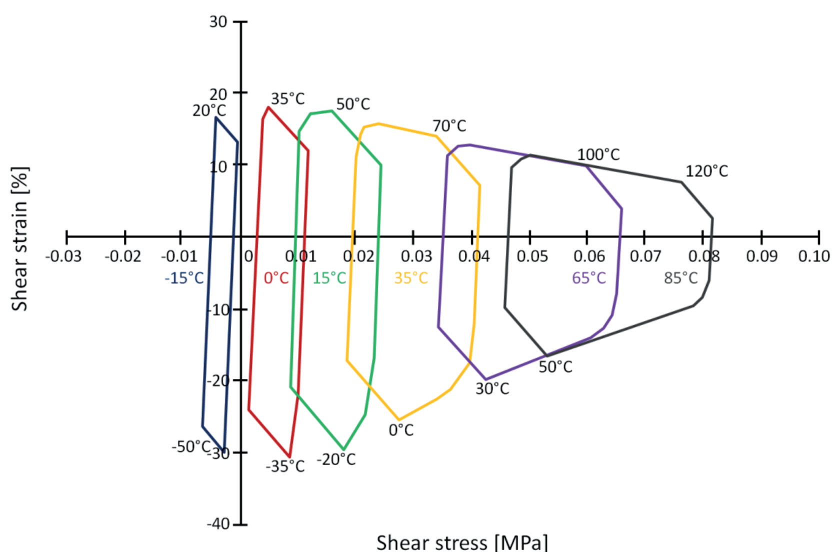

Figure 19: SnAgCu solder joints hysteresis loops for increasing mean temperature (fixed ΔT = 70°C, 30 minute cycle, 10 minute dwells) (adapted from [Cle05]).

3.2.4 Extreme temperatures

It has often been suggested that the lower dwell temperature of thermal cycling tests should be reconsidered. The reasons for the adopted lower temperature of -40°C is related to properties of SnPb solder. The 0.5 homologous temperature of SnPb solder is -45°C and therefore thermal cycling takes place within a region where time-dependent mechanism of plastic deformation (creep) is effective. The transition from SnPb to lead-free solders has increased the melting temperature of solders and, thus, the value of 0.5 homologous temperature has increased from -45°C to -28°C. Knowing that creep contributes significantly to the failures of solder interconnections, it is often speculated that the lower dwell temperature should be increased so that the creep would still have the same contribution to failure mechanisms throughout the thermal cycles. This would also lead to energy savings since the need for effective cooling systems would be reduced. However, the upper dwell temperature cannot be increased in order to maintain the same ΔT due to the glass transition temperature of FR-4 PWB material. This means that any change in the lower temperature would be accompanied by an unavoidable reduction in the ΔT and, subsequently, the acceleration factor of thermal cycling conditions. So, within the given physical limitations one cannot conduct an experiment where the lower dwell temperature would be varied without a change in the ΔT. However, if one is interested purely on the effect of the change in the lower dwell temperature on the acceleration factor of the tests, it can be studied.

Some authors have suggested that the lower dwell phase would be insensitive to duration of the phase because during the lower temperature dwell, there is a minimal amount of viscoplastic strain accumulated [Cla03, Mor91]. Syed, on the other hand, suggests that the dwell-time at lower temperature is a significant contributor to the failure mechanism if accumulated creep strain is used as the indicator of damage during thermal cycling [Sye10]. Syed also notes that placing emphasis only on the high-temperature dwell might be misleading since it is generally the lowest contributor to accumulated creep strain.

3.3 Evolution of SnAgCu solder microstructures

The reliability of solder interconnections has been studied for several decades, but the shift from SnPb solders to lead-free solders has made comprehensive reliability re-assessments necessary. It is well known that under thermomechanical loading cracking of solder interconnections are strongly

influenced by the microstructures formed during soldering and their evolution during operation. It has been observed earlier that the microstructural changes in Sn-rich lead-free solders are markedly different from those observed in SnPb solders. In tin-lead solders failures takes place as a result of the heterogeneous coarsening of tin and lead phases and eventually cracks propagate through the bulk solder (see e.g. [Fre92, Jon08]). The microstructural observations of failed Sn-rich lead-free solder interconnections have indicated that a different mechanism, namely recrystallization, changes the microstructures and assists cracking (see e.g. [Mat04, Mat07]). It is agreed that recrystallization significantly enhances crack propagation but it is still unclear under which conditions recrystallization assisted cracking takes place. It is also unclear how recrystallization assisted cracking correlates with real-use failures. Otherwise there is a risk of over acceleration and creating misleading failure mechanisms that are not seen in real operational products.

3.3.1 As-solidified microstructures

The tin-silver-copper solder alloy is the most commonly used lead-free solder in the electronics industry. In addition to the three major alloying elements, solder alloys with minor alloying elements such as nickel, bismuth, indium or antimony are also available. The solidification and generated microstructures of the near-eutectic SnAgCu alloys (more than 95 wt-% Sn) are most significantly influenced by the solidification of the tin-rich phase. The as-solidified microstructures of tin-rich solder interconnections are composed of few large solidification colonies of relatively uniformly oriented β-Sn cells distinguished by high-angle boundaries [Leh04, Mat04]. Figure 20 shows an example of a cross-section of a SnAgCu solder interconnection in the as-solidified condition. The cellular (or dendritic) structure is clearly distinguishable as the cells are surrounded by secondary and tertiary eutectic regions composed of uniformly distributed fine Cu_6Sn_5 and Ag_3Sn particles in the β-Sn matrix. It is noteworthy that the dissolution of the contact pads or pad metallizations of packages and PWBs during reflow changes the composition of the molten solder and the interconnection microstructures (see e.g. [Cha00, Mat04]). The influence of contact metallizations depends primarily on the dissolution rate and reactivity of the metallizations. The as-solidified microstructures on copper pads can show large amounts of primary Cu_6Sn_5 tubes or rods in the microstructure and large Cu_6Sn_5 particles embedded at the boundaries between the tin cells. The increased copper content in the solder interconnections can influence the

evolution of microstructures. It is known that the non-coherent high-angle boundaries between the Cu_6Sn_5 crystals and tin matrix provide good nucleation sites for recrystallization. The microstructures formed during solidification are, however, not stable and they will change notably in the course of thermal cycling.

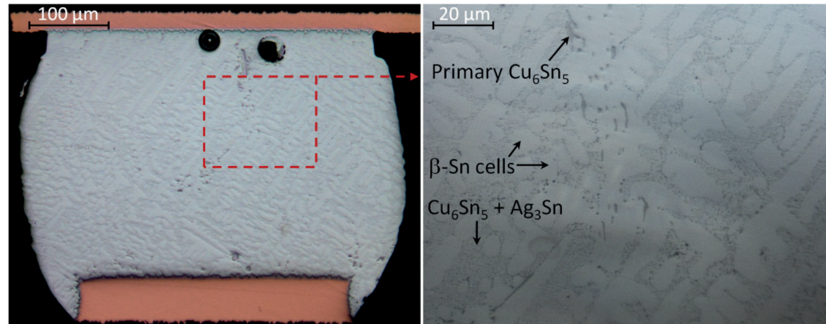

Figure 20: The as-solidified microstructure of a near-eutectic SnAgCu interconnection. Sn cells are surrounded by uniformly distributed Cu_6Sn_5 and Ag_3Sn particles. Nominal composition of the solder was Sn3.0Ag0.5Cu and the Cu pads of the PWB were coated with organic solderability preservative (Cu|OSP).

3.3.2 Effects of recovery and recrystallization

The thermomechanical stresses formed in solder interconnections under standard thermal cycling temperature conditions (e.g. -45°C to 125°C) are high enough to cause instantaneous plastic deformation of the commonly used near-eutectic SnAgCu solders [Li09]. This temperature range is above the 0.3 - 0.4 homologous temperature of the solder above which time-dependent deformation becomes significant. Time spent at either high or low temperatures allows diffusion creep processes to transform the elastic part of the total strain into inelastic strain. The energy stored during deformation acts as the driving force for the evolution of microstructures. The initiation of microstructural changes in solder interconnections is localized because of the highly non-uniform distribution of strains/stresses inside the solder interconnections. Figure 21 shows the calculated principal stress distribution of the corner most solder interconnection of the component board assembly (see Fig. 15). The inelastic deformation is more extensive on the package side regions where changes in the microstructure are observed first.

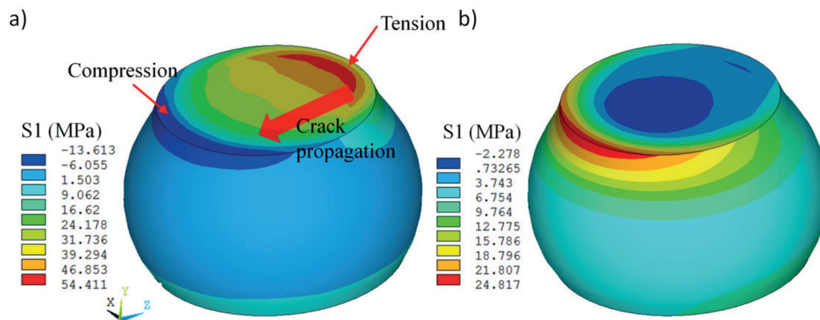

Figure 21: Calculated principal stress distribution of the corner most solder interconnection at a) the low temperature stage and b) the high temperature stage [Li11]. The positive and negative stress values denote tensile and compressive stresses, respectively.

Recrystallization is the formation of a new grain structure in a deformed material by the formation and migration of high angle grain boundaries driven by the stored energy of deformation [Doh97]. Recovery, on the other hand, can be defined as all annealing processes occurring in deformed materials that occur without the migration of a high angle grain boundary. The driving force of recovery and recrystallization is the energy stored (in the form of defects) in the crystal structures during plastic deformation. The microstructural changes are dependent on how much of this stored energy is released by recovery and how much by recrystallization, which are competing restoration processes. Recovery is the rearrangement of dislocations and, therefore, it occurs relatively quickly while recrystallization starts after an incubation period. Thus, recrystallization is initiated only if cyclic accumulation of stored energy is faster than its release by recovery. The degree of restoration by recovery depends on the stacking fault energy of the solder. Recovery is very effective in high stacking fault energy materials as a result of the efficient annihilation of dislocations by cross slip and climb. Previous studies carried out with pure tin have indicated that stacking fault energy of tin is high [Har61]. Since near-eutectic SnAgCu solder contains more than 95 wt-% tin, recovery is expected to be effective also in high-tin solder alloys. Therefore, recovery can reduce the driving force of recrystallization and recrystallization may not initiate or the incubation period can be very long. However, it has been widely observed that near-eutectic SnAgCu solder interconnections experience recrystallization under dynamic loadings caused by changes in temperature (e.g. between -40°C and +125°C) [Che11a, Dun04, Hen04, Mat04, Sun08, Ter04, Yin12]. Figure 22 shows a recrystallized microstructure of a thermally cycled solder interconnection taken with optical microscopy and cross-polarized light. Recrystallization can be seen on the package side and the PWB side of the interconnection.

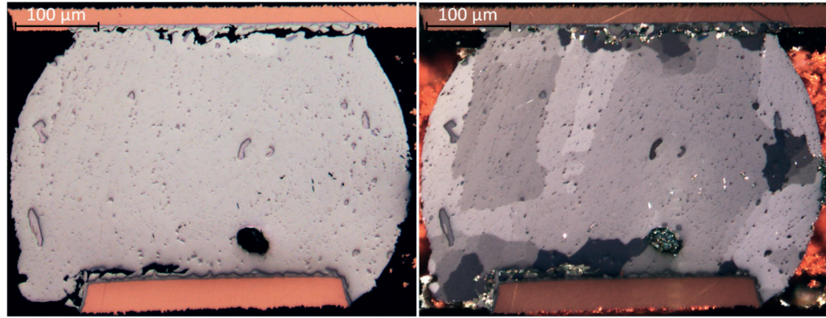

Figure 22: Recrystallized microstructure of a thermally cycled solder interconnection taken with bright light (left) and cross-polarized light (right) optical microscopy.

It has been observed earlier that under standard accelerated test conditions there are two different stages of evolution that cause the observed changes of microstructures in the stress concentration regions: first coarsening of the IMC particles and tin cells is accompanied by the gradual rotation of small volumes by recovery and, later on, by the change of microstructures by recrystallization [Mat12b]. In the strain concentration regions the tin cells begin to rearrange by the gradual coalescence of the tin cells and coarsening of the intermetallic particles. The eutectic regions around the tin cells disappear gradually, and in the course of thermal cycling a network of low-angle boundaries produced by recovery emerges [Mat10b, Mat12b]. The aforementioned microstructural evolution proceeds until the microstructures are transformed discontinuously by recrystallization. The solidification colonies are transformed into an equiaxed grain structure with a network of high-angle grain boundaries surrounding the recrystallized grains. It is also notable that the coarsening of the intermetallic particles is strong in the regions near the high-angle grain boundaries, while the regions near the low-angle boundaries still include finer particles, comparable to the bulk of the solder. This can be expected as the diffusion is much faster along the high-angle boundaries than it is along the low-angle boundaries.

The formation of the networks of grain boundaries by recrystallization influences the propagation of cracks (see Fig. 23). After the initiation of recrystallization, the recrystallized volume gradually expand from the initial strain concentration regions over the interconnections, and cracks follow the expansion of the microstructurally changed volumes (as cracks grow the distribution of stresses/strains evolve and recrystallized volume expands) [Mat12b]. It can be seen that intermetallic particles have been left at the grain boundaries as the recrystallized grains of Sn have nucleated and grown. The networks of the grain boundaries provide favourable paths for cracks to propagate intergranularly. It has been observed that the failures

exhibit globular surfaces as a result of the intergranular crack propagation between the recrystallized grains (see Publication IV for more details). Fatigue striations have also been observed on the surfaces of the recrystallized grains [Xu13].

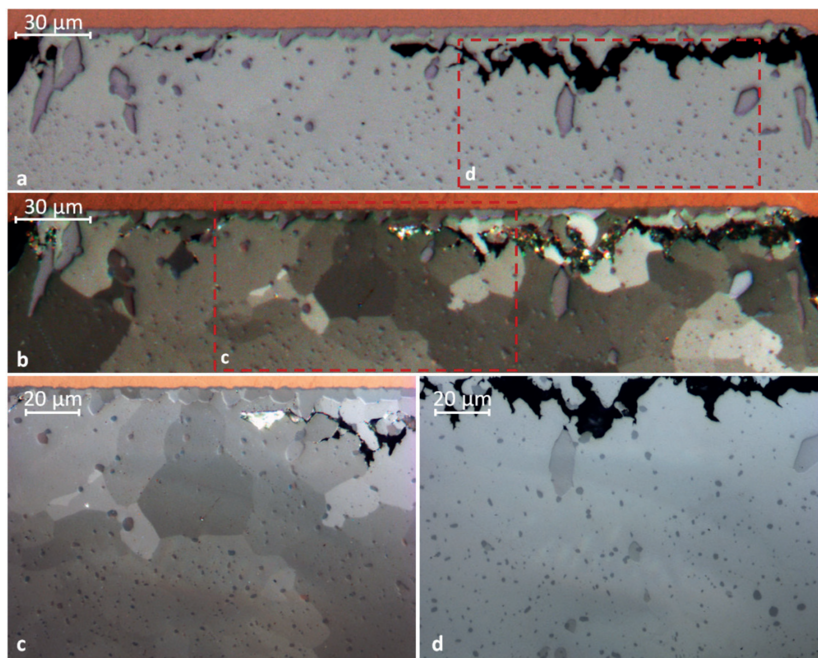

Figure 23: Optical micrograph showing a) crack propagation (package side interface) in a solder interconnection caused by thermal cycling, b) a cross-polarized light image showing the recrystallized structure of the same location, c-d) magnifications of the regions indicated in images a-b.

3.3.3 Fatigue

Solder interconnections that are subjected to repeated cyclic loading can fracture even at stress levels below the yield strength due to fatigue. Classical fatigue failures occur suddenly and unexpectedly because observable (macroscopic) plastic deformation does not occur before failure. However, fatigue failures observed under thermomechanical loading differs from the classical fatigue failures because plastic deformation precedes crack nucleation and propagation as demonstrated in Figure 24. Fatigue failure is a three–stage process involving i) crack nucleation, ii) crack propagation, and iii) crack growth leading to a final failure. The lifetime of an solder interconnection is mainly during stages I and II. Fatigue cracks nucleate preferentially at locations such as scratches, notches or dents, i.e. locations where stresses can concentrate on the surface of a material. If suitable crack nucleation sites are not available, plastic deformation will produce intrusions and extrusions on the surface of the material. The crack nucleation stage is

considered complete when the crack growth is no longer dependent on the structure of the deformed surface. Tensile stress produces a plastic zone at the tip of the crack and makes the crack tip stretch plastically by a finite length. The following compressive cycle closes the crack, making the new surface fold forward. This is repeated on every cycle and the crack propagates on each cycle until the interconnection fails completely. The crack growth rate can be enhanced by small particles causing voiding in the plasticized zone ahead of the crack tip. When the crack grows by a small amount each cycle, striations characteristic for fatigue failure are produced on the fractured surfaces. At a certain stage in the growth of a fatigue crack, the area of the uncracked cross–section will be reduced to a point where the stress acting on the remaining surface reaches a level at which an ordinary brittle or ductile fracture can occur.

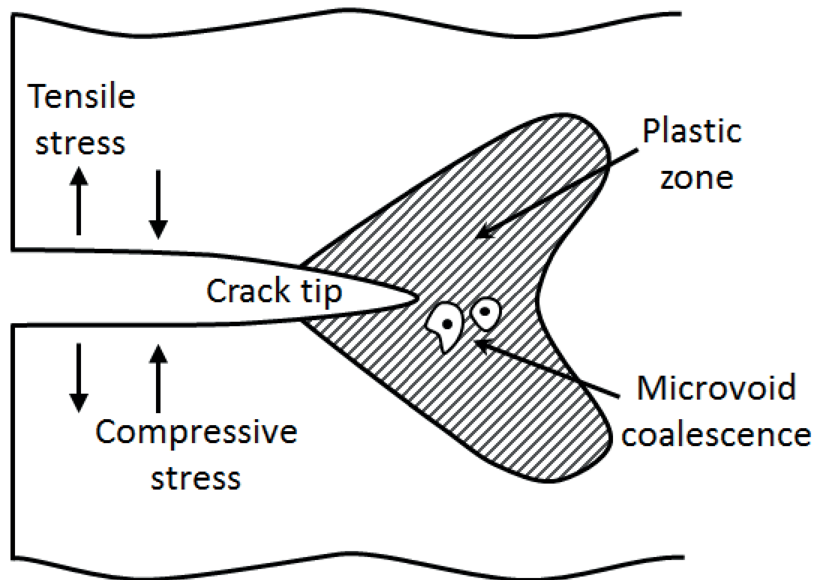

Figure 24: Schematic of a plastic zone ahead of a crack tip (adapted from [Ya009]). Tensile stress opens the crack and compressive stress squeezes the crack shut. Microvoid coalescence can increase the crack growth rate.

4. Effects of Minor Alloying Elements on Mechanical Properties of SnAgCu Solders

As discussed in the previous chapters, both mechanical properties of the bulk solder as well as those of the interfacial intermetallic layers determine the reliability of electronic component boards. Depending primarily on the elasticity and strength of the solder, the solder interconnections can fail either from the solder bulk or from the intermetallic layers. When an interconnection fails from the bulk, a solder composition with a higher strength is expected to provide better performance. However, in the case when intermetallic failures are encountered, reliability improvements could be sought either from decrease of the strength and elastic modulus of the solder or from modification of the properties of intermetallic layers.

Today the most commonly used solder joint composition is the Sn3.0Ag0.5Cu (wt-%). It is well-known that Ag is a very effective strengthener of Sn and, therefore, reducing the Ag content provides an easy way to reduce the strength of the SnAgCu solder interconnections. However, increase in the strength of solder by increasing the Ag content from the 3.0 wt-% is not desirable due to the change of the primary phase and subsequent effects on the onset of recrystallization under thermomechanical fatigue. The increase in the strength is therefore better performed by minor alloying elements that do not introduce new intermetallic compounds and do not change the solidification sequence of the intermetallic phases. Bismuth is one such element and thus it was selected to be used in this study. It is also known that the addition of Ni in the SnAgCu solder should be beneficial for the drop reliability performance when the Ni concentration is kept low (at about 0.1 wt-%). In the following, the effects of these two minor alloying elements (Bi and Ni) and changes in the Ag content on the SnAgCu solders microstructures and mechanical properties will be summarized.

4.1 Effects of Bi on mechanical properties of SnAgCu solders

Bi has been an avoided element in soldering due to the low melting temperature phases (ternary eutectic reaction at about 96°C) in the presence of Pb in SnBi solders [Moo01, Zen03]. Since majority of today's electronics production is Pb-free, Bi as a minor alloying element should be reconsidered. The addition of Bi into the near-eutectic SnAgCu solders does not have a significant effect on the microstructures formed due to the relatively high solubility of bismuth in Sn. Bi does not react with Sn and microstructural investigations of Xiao et al. by employing transmission electron microscopy (TEM) have indicated that Bi does not dissolve in Ag_3Sn or Cu_6Sn_5 phases and, thus, it stays in the tin phase solid solution [Xia00]. Therefore it can be assumed that addition of Bi into SnAgCu solders affects the mechanical properties mainly by solid solution strengthening. However, it has been reported by several authors that increased Bi concentration effectively increases the ultimate tensile strength of Sn but decreases elongation to fracture, e.g. [Hwa04, Zha04]. Due to the opposite trends of strength and ductility with changed Bi content, it has been recommended that the Bi content in SnAgCu solders should not be increased above about 3 wt-% [Kar98, Tat00]. Besides increase in Bi content above about 3 – 5 wt-% does not influence strength notably anymore, which is most likely related to the fact that at about this composition range Bi reaches the saturation in Sn and above it Bi precipitates [Li08]. Xiao et al. observed in their TEM investigations small Bi containing particles in the Sn3.4Ag4.8Bi (wt-%) [Xia00]. Based on this it can be assumed that with Bi concentrations above about 5 wt-% the strengthening is enhanced by precipitation hardening but, as noted above, further increase in strength with increased Bi content quickly saturates.

Tensile strength, elongation and hardness of Bi bearing SnAgCu solders have shown superior stability with aging compared to SnAgCu solders [Zha04]. However, it seems that the associated decrease in ductility with increase in Bi concentration of SnAg(Cu) solders decreases the mechanical fatigue (at room temperature) properties as studied by Kariya and Otsuka: they increased Bi content in Sn3.5Ag systematically up to 10 wt-% and discovered that increased Bi concentration decreased the fatigue life of the solder interconnections significantly [Kar98]. This result was confirmed by Kanchanomai et al. a few years later [Kan02]. Yu and Shiratori made the same observation also after isothermal ageing of the specimens at 150˚C for 200 hours [Yu05]. Finally, Yu and Shiratori studied isothermal mechanical fatigue life of BGA interconnections and concluded that the assemblies having the Sn3.5Ag5.0Bi composition of interconnections had their fatigue life

about half of that of the assemblies with Sn3.5Ag0.75Cu composition over the entire strain range of the study (0.0015 – 0.008 mm/mm). However, perhaps surprisingly, increase in thermomechanical fatigue life of SnAg with Bi additions was reported by Tateyama et al. who compared the thermal cycling reliability of T-BGA board assemblies with interconnections having the composition of Sn3.5Ag0.7Bi or Sn3.5Ag3.0Bi and, furthermore, they found out that the alloy with higher Bi content performed better [Tat00]. As final remarks about the effects of Bi it can be pointed out that addition of Bi in the SnAgCu solder has been observed to decrease the thickness and growth rate of the Cu_6Sn_5 intermetallic layers when soldered on Cu pads [Riz06] and that Bi seems to suppress the formation of the Cu_3Sn intermetallic layer [Hod11]. Other recognized effects of Bi as an alloying element in solders are related to its ability to effectively mitigate the tin whisker growth and to contribute to the improvement in wetting ability of copper surfaces [Via99, Hwa03].

4.2 Effects of Ag on mechanical properties of SnAgCu solders

Nearly all of the solder compositions used in the electronics industry, such as the composition of Sn3.0Ag0.5Cu, have Ag and Cu concentrations below the eutectic concentration of approx. Sn3.4Ag0.8Cu wt-% [Moo00, Pen01]. Ag concentrations below the eutectic has been adopted in order to avoid the formation of the primary Ag_3Sn phase, which commonly takes the form of large plate-like crystals [Hen02, Rei08, Kel11]. The large primary Ag_3Sn plates are considered undesirable because the adhesion between the Ag_3Sn and the Sn matrix seems weak [Zen11] and cracks are often observed to propagate along the interface between these crystal plates and the Sn matrix (see e.g. [Hen02, Rei08, Zen11]). The Ag content has still been kept quite high, between 3.0 and 3.4 wt-%, in order to provide adequate strength for the alloy, and to keep both the liquidus temperature as low as possible. However, over the past few years, the Ag content of SnAgCu solders has gained much attention because it has been shown that the low silver content SnAgCu interconnections perform better under mechanical shock and drop loading conditions as compared to the near-eutectic SnAgCu compositions (see e.g. [Suh07, Zhu08, Sna12]).

The effects of Ag concentration on the mechanical properties of SnAgCu solders have been studied extensively. It has been shown that the reduction in Ag concentration from 3 wt-% down to 1 wt-% decreases the elastic modulus, yield stress (0.2% proof stress) and ultimate tensile strength (UTS) but increases ductility, which can all be attributed to the changes in the

amount of fine Ag_3Sn precipitates in the secondary and tertiary phases [Che08a, Che11b]. Furthermore, all of the listed characteristics increase with increased strain rate [Che08a].

Chen and Dutta compared the creep rate of low Ag solder (Sn1Ag0.5Cu) with that of higher Ag composition (Sn4Ag0.5Cu) and found out that the steady state creep rate of the lower Ag content was about an order of magnitude higher over the entire temperature range of 50 - 150°C (the values of creep rate at different temperatures were about two orders of magnitude apart for both alloys) [Che08b]. Kariya et al. studied the isothermal (room temperature) cyclic fatigue of SnxAg0.5Cu, where x = 1, 2, 3 or 4 wt-% under constant share strain rate of 10^{-2} s^{-1} [Kar04]. They found out that the fatigue life of 3 and 4 wt-% Ag compositions are equal but that of 2 wt-% Ag is almost one third of that over the entire 0.1 – 10 % plastic strain range. However, the 1 wt-% Ag alloy differs from the others: under the high strain regime the fatigue life is equivalent to the high Ag alloys but under the low strain regime it performs the poorest. This can be understood based on the results of Chen and Dutta because we can expect the cumulative contribution per cycle of instantaneous plastic deformation (to the total damage of the solder interconnections) to be smaller under the low strain and, therefore, the dependency on the creep rate becomes stronger.

Lee and Subramanian have studied the evolution of shear strength of Sn4Ag0.5Cu and Sn2.5Ag0.5Cu0.5Ni solder compositions as a function of cyclic thermal ageing. For the Sn4Ag0.6Cu solder joints, the residual shear strength dropped about 20% within the first 250 cycles but the rate of decrease stabilized to about 35% total decrease within 1 000 cycles [Lee07]. The decrease in the strength was even larger under faster rates of temperature change. The low Ag solder showed initially lower shear strength but the rate of decrease was only about 10 % within the 1 000 cycles and it was not dependent on the rate of temperature change during cycling. Thus, it seems that reduction in Ag content leads to decreased thermal cycling reliability but the significance of the reduction depends on the amount of inelastic strain produced in the interconnections.

4.3 Effects of Ni on mechanical properties of SnAgCu solders

It is commonly agreed that the minor addition of Ni in the SnAgCu solders affects the intermetallic layers in two distinct ways: (1) the thickness of the Cu_3Sn layer is reduced as the function of increasing Ni content and (2) the grain size of the Cu_6Sn_5 layer becomes smaller [Ama08, Wan09a, Lau10, Ham13]. However, the effect of Ni addition on the thickness of the interme-

tallic layers are not uniform: with the addition of about 0.1 wt-% Ni in a near eutectic SnAgCu solder, the thickness of both the Cu_3Sn and Cu_6Sn_5 layer is reduced to about half [Tsa03, Vu007]. However, further increase in the Ni concentration decreases the thickness of the Cu_3Sn layer but increases the thickness of the Cu_6Sn_5 layer. Thus, from the perspective of this thesis the addition of Ni in the SnAgCu solder should be beneficial for the drop reliability but the Ni concentration should be kept low, preferably at about 0.1 wt-% [Tan06, Zha08, Wan09b]. At these concentrations, all Ni is bound in the Cu_6Sn_5 phase and therefore the effect of Ni is significant in the interfacial intermetallic layers but influences on the bulk microstructures are insignificant.

5. Results

In the following, the main findings of the five appended publications are presented and discussed. The section has been divided into two parts based on the two different loading types.

5.1 Mechanical loading

Publication I, entitled **“A Novel Impact Test System for More Efficient Reliability Testing”** presented a new method that is based on the use of a pneumatic cylinder to produce the desired shock pulses, for example those defined in the JESD22-B110A and JESD22-B111 standards. The measurements showed that the pneumatic test system is capable of producing peak deceleration well above the maximum (2 900 G) stated in the JESD22-B110A. More importantly, a testing time an order of magnitude shorter was achieved by increasing the drop impact repetition frequency; an impact repetition frequency of 1.6 Hz was achieved with the pneumatic shock impact tester as shown in Figure 10. Two improved component board attachments based on the support of the full board width were designed in order to simplify the bending motion of component boards. Both the finite element calculations and the experimental results showed that under the full board width support conditions the bending of the component board is more uniform and different component locations experience more equal strains as compared to bending under the conventional 4-point support conditions. The reliability tests that were performed verified that the full board width support produces the same failure modes and that the lifetimes of packages at different locations on the printed wiring board are more comparable with each other with the full board width support than they are with the conventional 4-point support. The benefits of the pneumatic tester that was developed are related to the time needed for testing, the stability of the impact pulse over long periods of time, and the more consistent lifetime statistics achieved by the simplified bending of the component board during testing.

Publication II, entitled **“The Reliability of Component Boards Studied with Different Shock Impact Repetition Frequencies”** studied the effects of impact repetition frequency on the lifetime and failure mechanisms of electronic component boards. Three shock impact repetition frequencies (0.01 Hz, 0.1 Hz, and 1.6 Hz) were used to study the sensitivity of component board lifetime to the time between the shock impacts. The results showed that the impact repetition frequency has a significant effect on the average lifetime of the studied packages: the average number of impacts-to-failure increased with increased impact repetition frequency. A change in the impact repetition frequency did not, however, change the primary failure mode and the failure mechanism. In order to explain this observation, the formation of residual stresses in the solder interconnections from shock impacts and their relaxation during the time between the shock impacts were evaluated by employing FEM, which showed that at room temperature the stress relaxation by creep of solder is significant even at less than 10 second time frame. The effect of the stress relaxation on the lifetime of the component boards was studied experimentally by repeating the impact tests at elevated temperature with the intention of influencing rate of stress relaxation. The results showed that the relaxation of the residual stresses has a significant effect on the component boards shock reliability (at less than 1% risk level). The results indicate that the impact repetition frequency should be taken into account, especially when reliability assessments are being carried out with different testers, since the interval between the shock impacts varies from one test system to another.

5.2 Thermomechanical loading

Publication III, entitled **“Thermal Cycling Reliability of Sn-Ag-Cu Solder Interconnections – Part 1: Effects of Test Parameters”** focused on identifying the effects of thermal cycling test parameters on the lifetimes of BGA144 component boards. The effects of (i) temperature difference (ΔT), (ii) lower dwell temperature and lower dwell-time, (iii) mean temperature, (iv) dwell-time and (v) ramp-rate were evaluated. Based on the characteristic lifetimes, the thermal cycling profiles were categorized into three lifetime groups (see Table III): i) highly accelerated conditions (red), ii) moderately accelerated conditions (yellow), and iii) mildly / non-accelerated conditions (green). Most of the studied profiles fell into the highly accelerated group, even though the differences in the acceleration factors within this group were large. However, decreasing the ΔT or lowering the mean temperature led to less accelerated conditions. The “normal-

use" profile (12.) and the 0°C mean temperature profile (11.) were clearly less accelerative than the "standard" profiles (1. – 9.). The acceleration factor of the "extreme-use" profile (10.) was between these two lifetime groups (moderately accelerated conditions). Thus, one might be tempted to use the highly accelerated profiles to produce lifetime statistics as quickly as possible. However, to do this one needs to know that the failure mechanisms do not change from one group to another and that the failure mechanisms correlate with real-use failures. Therefore, in part 2 of the study the focus was on the failure mechanisms and the microstructural changes took place in the three lifetime groups.

Table III: Thermal cycling profiles divided into three lifetime groups: (i) highly accelerated conditions (red), (ii) moderately accelerated conditions (yellow), and (iii) mildly/nonaccelerated conditions (green).

Thermal profile	Weibull η (cycles)	Weibull η (hours)	Weibull β	AF (cycles)	AF (hours)
1. TC165-42.5C-D0	7 388	5 172	4.1	1.84	5.71
2. TC165-42.5C-D30	8 797	14 956	3.3	1.55	1.97
3. TS165-42.5C-D0	5 117	1 194	9.6	2.66	24.73
4. TS165-42.5C-D5	8 498	3 399	7.1	1.60	8.69
5. TS165-42.5C-D10	4 436	2 514	6.3	3.07	11.74
6. TS165-42.5C-D15	3 617	2 652	3.1	3.77	11.13
7. TS165-42.5C-D30	6 970	8 596	5.7	1.95	3.43
8. TS165-76C-D10/0	8 673	3 469	6.9	1.57	8.51
9. TS130-60C-D10	8 312	4 156	2.4	1.64	7.10
10. TC100-75C-D15	13 626	29 523	4.9	1.00	1.00
11. TS130-0C-D10	32 345	16 173	3.5	0.42	1.83
12. TC50-54C-D24/14	>> 21 000	>> 26 250	-	<< 0.65	<< 1.12

Publication IV, entitled **"Thermal Cycling Reliability of Sn-Ag-Cu Solder Interconnections – Part 2: Failure Mechanisms"** explained the observed differences in the component board lifetimes by studying the failure mechanisms and the microstructural changes that takes place in the three groups of loading conditions. Figure 25 shows the primary failure modes from different thermal cycling profiles (see Table III/Figure 18 for more details). Optical bright light images show the crack paths and the cross-polarized light micrographs the microstructural changes associated with each of the cracks. It was observed that under the standardised thermal cycling conditions (highly accelerated conditions) the networks of grain boundaries formed by recrystallization provided favourable paths for cracks to propagate intergranularly. It is noteworthy that the coarsening of inter-

metallic particles was strong in the recrystallized regions (cellular structure had disappeared completely in the crack region). However, under the real-use conditions (mildly /non-accelerated conditions) recrystallization was not observed in the solder interconnections and cracks had propagated transgranularly in the bulk solder or between the IMC layer and the bulk solder. The real-use conditions showed slight coarsening of the microstructure close to the crack region but the solder bulk still included finer IMC particles and β-Sn cells characteristic of the as-solidified microstructures. These finding suggests that standardised thermal cycling tests that are used to assess the reliability of lead-free solders are creating failure mechanisms that are not seen in conditions representing real-use operation.

Publication V, entitled **"The Reliability of Micro-Alloyed SnAgCu Solder Interconnections under Cyclic Thermal and Mechanical Shock Loading"** compared the reliability of the BGA solder interconnections of three different compositions (Sn3.1Ag0.5Cu, Sn3.0Ag0.5Cu0.2Bi, or Sn1.1Ag0.5Cu0.1Ni) under the mechanical shock and the cyclic thermal loading. The reliability of the component boards was dependent on the solder composition in both the tests but the results were opposite: the interconnection composition whose reliability under the mechanical shock loading was the best (SnAgCuNi) performed the weakest in the thermal cycling test. The results suggest that the lower strength of solder interconnection can be beneficial for drop reliability but detrimental to thermal cycling reliability. Modification of the intermetallic layers, for example by the introduction on minor amounts of Ni in the SnAgCu solders, change the morphology of the interfacial reaction layers and, thereby, can make them less susceptible to failure in the drop tests. The relatively low amount of Bi does not affect the microstructure of the solder interconnections but increases their strength as compared to the near eutectic SnAgCu. The lower Ag content of the SnAgCuNi interconnections, on the other hand, makes the interconnections lower in strength as compared to the near eutectic SnAgCu. The results point out that the choice of solder composition for particular applications should be made on the basis of typical operation conditions of the product. It is suggested that the SnAgCuNi solder is suitable for applications that experience mostly mechanical shocks such as drops but not significant changes of temperature, while the SnAgCuBi alloy is a more suitable alternative for applications that experience mainly thermomechanical loads. The SnAgCu, out of the three compositions studied, showed to be a good general purpose solder alloy for applications that experience thermal as well as mechanical loads.

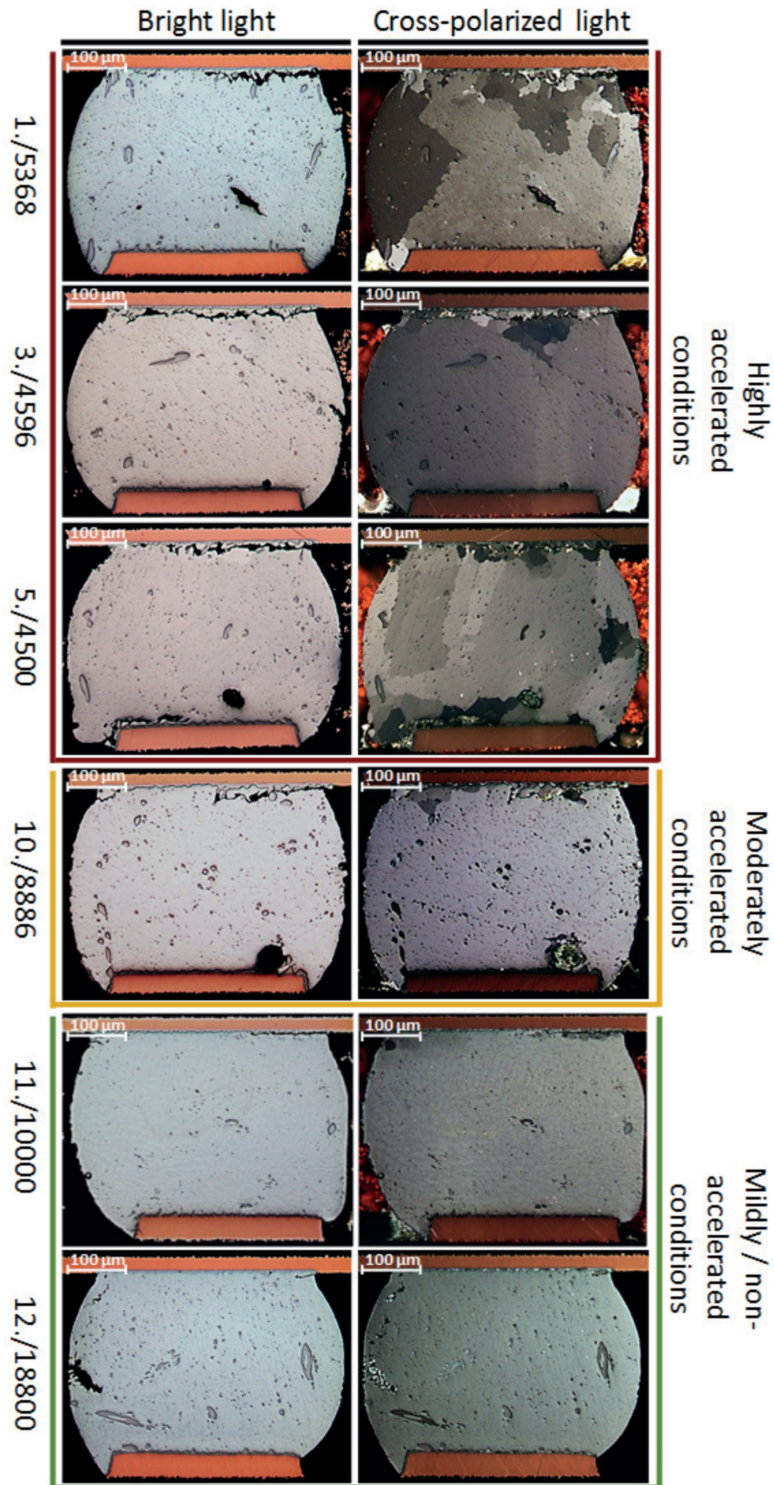

Figure 25: A bright light image (left) and a cross-polarized light image (right) showing the primary failure modes and the microstructural changes associated with the crack growth of the three lifetime groups. Numbering on the left side indicates the thermal profile and the number of cycles before failure analysis.

6. Conclusions

In the following, reasoning of the two theses presented in the Introduction chapter will be given.

1) **Drop impact reliability of component boards is time-dependent.**

After the shock impact the component board bends downwards forced by the inertia and oscillate at a high frequency for about 20–30ms. Bending causes displacements between the PWB and the package and deforms the solder interconnections. The plastic deformation during the shock impact causes residual stresses that are relaxed during the time between the shock impacts. The FEM was employed to investigate (a) how much residual stresses are formed during the shock impact, and (b) to what extent the residual stresses are released during the time between shock impacts (investigated time frame of 0.63–100 s). In order to study the effect of stress relaxation in solder interconnections during the time interval between the shock impacts, two consecutive impacts were simulated and the residual stresses and the accumulated creep strains were estimated/calculated by FEM. The results indicate that: (i) an increase in the time interval between the shock impacts increases the creep strain in the solder interconnections significantly even at room temperature (after 0.6 s of the first impact the creep strain increased from 2.23E-07 to 7.88E-07 which equals an increase of about 253%; after 100 s the creep strain has increased about 34 000%), (ii) stress relaxation is more significant with an increase in the time interval between the shock impacts (after 0.6 s of the first impact the stress decreases from 19.6 MPa to 19.4 MPa which equals an decrease of about 1%; after 100 s the stress has decreased about 8%), and (iii) the elevated temperature increases the creep strain when compared with the corresponding values at room temperature.

Since the FEA results showed that the creep of solder can reduce the residual stresses in the interconnections notably within relatively short time frame, the effect of stress relaxation on the lifetime of component boards needed further investigation. Since the creep rate is dependent on tempera-

ture, an increase in the temperature of the component boards accelerates the relaxation of the residual stresses. The temperature of 100°C was considered high enough to have an effect on the creep rate of the solder interconnections but low enough not to change the mechanical properties of the interconnections and the PWB too much (100°C is well below the glass transition temperature). Because stress relaxation by creep of solder is dependent on time and temperature, its effect is reflected in the difference of the relative change in the average number of impacts-to-failure when frequency is changed in one temperature as compared to the same change in frequency in another temperature. The fact that the relative increase in lifetime at the elevated temperatures (where the rate of stress relaxation is higher) is smaller indicates that the formation of residual stresses during impacts and their relaxation between the impacts is largely responsible for the observed dependency between lifetime and impact repetition frequency.

2) **Standardised thermal cycling tests that are typically used to assess the solder interconnection reliability of component boards can create failure mechanisms that are not seen in conditions representing real-use operation.**

Lifetimes and failure mechanisms of solder interconnections under cyclic conditions were found to be dependent on the parameters of the thermal cycling tests. Test conditions representing normal changes of temperature (e.g. inside modern portable electronic products) induced much longer lifetimes as well as failure mechanisms that differed greatly from those observed under the highly accelerated test conditions. In the accelerated tests, the microstructural evolution (recrystallization) controlled the propagation of cracks, while in the real-use conditions, significantly less microstructural evolution took place and the rate of crack propagation through the solder was notably lower. Under the standardised thermal cycling conditions (highly accelerated conditions), the networks of grain boundaries formed by recrystallization provided favourable paths for cracks to propagate intergranularly. It is noteworthy that the coarsening of intermetallic particles was strong in the recrystallized regions (the cellular structure had disappeared completely in the crack region). However, under the real-use conditions (mildly/non-accelerated conditions), recrystallization was not observed in the solder interconnections and cracks had propagated transgranularly in the bulk solder. The real-use conditions showed slight coarsening of the microstructure close to the crack, but the solder bulk still included finer IMC particles. Therefore, it is reasonable to assume that the failure mechanism caused by the highly accelerated conditions does not

reproduce the same failure mechanism that is produced under real-use conditions. However, it is essential to bear in mind that the geometry of the package, PWB structure and solder composition affects significantly the stress/strain conditions formed in the solder interconnections and thus the lifetime results and failure mechanisms are affected as well. As discussed in Publication V, higher solder strength is beneficial for thermal cycling reliability because the stored energy i.e. the driving force of recrystallization is reduced with increasing strength. On the other hand, increased strength will compromise drop reliability due to the fact that increased stresses in the solder interconnections make them more prone for intermetallic cracking.

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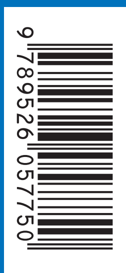
Electrical devices are frequently used in challenging operation environments where devices can experience large changes in temperature, combined with mechanical shocks and vibrations. Recently, there has been an increasing interest towards the optimisation of test parameters to improve the test efficiency and to minimize the total testing time. This work focuses on identifying the effects of test parameters on the reliability of electronic assemblies under two different loading types, namely mechanical shock loadings and thermomechanical loadings. The results provide understanding about the correlation of real-use conditions and highly accelerated test conditions. It is shown that highly accelerated test conditions can produce lifetimes and failure mechanisms that differ significantly from those seen in conditions representing real-use operation. Re-assessment of the standardized test parameters and lifetime prediction models is therefore necessary in order to achieve better correlation between test conditions and real-use conditions.



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