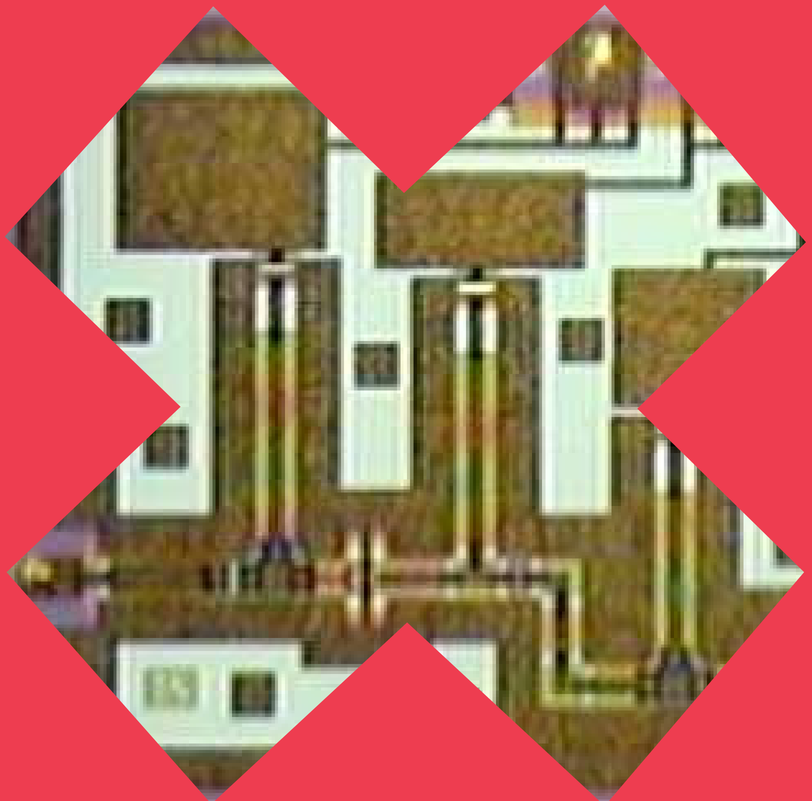
Department of Micro- and Nanosciences

# Design and characterization of monolithic millimeter-wave integrated circuits for receiver front-ends

Mikko Kärkkäinen



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# Design and characterization of monolithic millimeter-wave integrated circuits for receiver front-ends

**Mikko Kärkkäinen**

A doctoral dissertation completed for the degree of Doctor of Science (Technology) to be defended, with the permission of the Aalto University School of Electrical Engineering, at a public examination held at the lecture hall TU1, TUAS house, Otaniementie 17, Espoo, 18 September 2014 at 12.

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**Electronic Circuit Design**

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# Abstract

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**Abstract**

This dissertation focuses on millimeter-wave front-ends and technologies and, especially, on integrated circuits operating at millimeter-wave frequencies. Several issues concerning millimeter-wave circuits are discussed, such as transmission lines and transistor models for small-signal simulations and noise characterization. The applications for these circuits vary from 60-GHz high-speed radio links to atmospheric precipitation measurement systems operating up to the water molecule resonance frequency of 183 GHz.

In chapter 3, the transistor model is calculated from measured data using saturation measurements only. The de-embedding is obtained using open and short coplanar waveguide structures. By calculating the extrinsic parasitics using linear regression, the small-signal parameters of the transistor model can be calculated and then simulated up to 110 GHz. The noise model is calculated based on the measured V-band (50–75 GHz) noise parameters and the corresponding noise matrices related to the open and short structures as well as the extrinsic parasitics. The values obtained for the noise sources and their correlation make wideband simulations of the transistor noise characteristics possible. The small-signal model, including the noise sources, can be used to simulate three different realized amplifiers and the results are compared to the measured data. These simulations show a very good agreement between the measured data and the simulated values.

Certain select design principles related to millimeter-wave, low-noise amplifiers and mixers are presented as well. This includes front-end system aspects as well as transistor selection issues. Chapter 5 discusses the issues related to millimeter-wave measurements in detail. The losses of different parts of the measurement setup, such as the back-to-back probe loss from two separate measurements and harmonic mixer, are shown. The noise measurements at these frequencies require special attention since the setup requires downconversion of the noise signal either within the device under test or externally with a separate measurement mixer. Empirical results are presented for both compound semiconductor and silicon -based circuits, namely GaAs HEMT and CMOS technologies. The measured results for the low-noise amplifiers are presented at operating frequencies of 94, 155, and 183 GHz. The 183 GHz amplifier achieved a gain of 16 dB and a 7.4-dB noise figure. In addition, two receiver front-ends are presented. One is realized with 150-nm GaAs PHEMT and the other with 65-nm CMOS technology. The GaAs receiver front-end consists of a three-stage, low-noise amplifier and an image-rejecting resistive mixer, while the silicon-based circuit has a balanced active mixer integrated with a five-stage amplifier.

**Keywords** low-noise amplifier, millimeter-wave receiver, transmission lines

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# Tiivistelmä

**Tekijä**
Mikko Kärkkäinen

**Väitöskirjan nimi**
Mikropiirien suunnittelu ja karakterisointi millimetriaaltoalueen radiovastaanottimiin

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**Tiivistelmä**

Tämä väitöskirja käsittelee millimetriaaltoalueen radioetupään suunnittelua ja toteutusta erilaisilla mikropiirien valmistusteknologioilla. Erityisesti käsitellään millimetriaaltoalueen piireihin liittyviä asioita, kuten siirtojohtoja ja transistorimalleja piensignaalisimuloinneissa sekä kohinan mallintamista. Näille piireille löytyy useita erilaisia sovelluksia, kuten esimerkiksi nopeat 60 GHz:n radiolinkit ja ilmakehän kosteuspitoisuusmittaukset vesimolekyylin resonanssitaajuudelle 183 GHz:iin asti.

Transistorimalli on laskettu mitatusta datasta käyttäen hyväksi ainostaan saturaatiossa saatuja tuloksia. Transistorin ominaisuuksien laskemisessa käytetään myös koplanaariseen siirtojohtoympäristöön suunniteltuja avointa ja oikosuljettua testirakennetta. Ulkoiset parasiittiset ominaisuudet lasketaan lineaarisen regression avulla ja niiden vaikutuksen poistamisen jälkeen lasketulla piensignaalimallilla simuloidaan transistorin ominaisuuksia 110 GHz:iin asti. Kohinamalli perustuu V-alueen (50-75 GHz) kohinaparametrimittauksiin sekä avoimen ja oikosuljetun testirakenteen kohinamatriiseihin. Näin saatujen kohinalähteiden ja niiden korrelaation avulla voidaan simuloida transistorin kohinaominaisuuksia laajalla kaistalla. Lisäksi kohinalähteet sisältävän piensignaalimallin avulla simuloidaan kolmea erilaista vahvistinta ja tuloksia verrataan mitattuihin arvoihin. Nämä simulaatiot vastaavat erittäin hyvin mitattuja tuloksia.

Kirjassa käsitellään myös muutamia millimetriaaltoalueen vähäkohinaisiin vahvistimiin ja sekoittimiin liittyviä suunnitteluperiaatteita. Niitä ovat etupäähän liittyvät järjestelmänäkökohdat sekä transistorin valintaan liittyvät asiat. Mittaustekniikkaa esittelevässä kappaleessa esitellään muutamia millimetriaaltoalueen mittauksiin vaikuttavia erityispiirteitä yksityiskohtaisemmin. Mitttauslaitteiston eri osien, kuten mittakärkien ja harmonisen sekoittimen, aiheuttamia häviöitä tutkitaan. Millimetriaaltoalueen kohinamittaukset vaativat erityistä huomiota, koska mittauslaitteistoon täytyy liittää alassekoitus, joko toteutettuna mitattavalla piirillä itsellään tai ulkoisen harmonisen sekoittimen avulla. Empiirisiä tuloksia esitellään niin yhdistepuolijohde- kuin pii-piireiltä mitattuina tuloksina, erityisesti GaAs-HEMT- ja CMOS-teknologioilla toteutetuista piireistä. Tuloksia esitetään vähäkohinaisista vahvistimista 94, 155 ja 183 GHz:n taajuusalueille. 183 GHz:n vahvistin saavuttaa 16 dB vahvistuksen ja 7,4 dB kohinaluvun. Lisäksi kaksi 60 GHz:n radioetupäätä on toteutettu ja mitattu. Toinen on valmistettu 150 nm GaAs PHEMT -teknologialla ja toinen 65 nm CMOS-teknologialla. GaAs-radioetupää sisältää 3-asteisen vahvistimen ja peilitaajuutta vaimentavan sekoittimen, kun taas piillä toteutettu radioetupää koostuu balansoidusta aktiivisekoittimesta ja 5-asteisesta vahvistimesta.

**Avainsanat** vähäkohinainen vahvistin, millimetriaaltoalueen vastaanotin, siirtojohdot

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# Preface

The work for this dissertation was carried out in the Department of Micro- and Nanosciences at Aalto University. The work was done in connection with several projects, including the Lalamo, Nastec, Brawe, and Beams projects, funded by the Finnish Funding Agency for Technology and Innovation (Tekes), and several companies, such as Nokia Research Center, Nokia Siemens Networks, Elektrobit, DA-Design, and Elisa. The amplifiers at operating frequencies of 94, 155, and 183 GHz were developed for millimeter-wave projects funded by the European Space Research and Technology Centre (ESTEC). Moreover, the work was supported by the Academy of Finland as a part of the Millimono, Uncmos, and Famos projects as well as by the Centre of excellence SMARAD and SMARAD-2 programs.

I would like to express my gratitude to the Department of Micro- and Nanosciences for giving me the opportunity to work on various projects and also do research in the field of microelectronics. I wish to thank the Jenny and Antti Wihuri Foundation and the Ulla Tuominen Foundation for their financial support.

I also wish to thank the former head of department, Professor Kari Halonen, for acting as supervisor and superior. I warmly thank Dr.-Ing. Michael Schlechtweg and Professor Markus Törmänen for reviewing my thesis. I wish to thank both Professor Kari Halonen and emeritus Professor Veikko Porra for the opportunity to work on this interesting research area.

I am also grateful to several colleagues, Dr. Mikko Varonen, Dan Sandström, Jan Riska, and Dr. Pekka Kangaslahti, for their co-operation, support, and stimulating discussions. During the project work, I was also able to co-operate with Fraunhofer IAF as a part of the ESTEC funded projects and, thus, I am thankful to Dr. Matthias Seelmann-Eggebert and Axel Tessmann for this opportunity. I had lively and fruitful discussions with Tapani Närhi from ESTEC during many project meetings. I want to thank Petri Jukkala and Ari Alanne from DA-Design Oy for discussions and support. In addition, I want to thank Jan Riska, Tero Tikka, Dr. Ville Saari,

Pasi Juurakko, Ali Vahdati, and Dristy Parveg for sharing the office with me.

Furthermore, I wish to thank my friends for pleasant leisure time as well as refreshing badminton games, which gave me an excellent break from work. I wish to thank my mother Päivi, in 2010 passed away father Matti and my sister Matilda for encouragement and support during the entire time it took to complete this dissertation. I am also grateful to Miia for support during the writing of this dissertation.

Espoo, August 2014

Mikko Kärkkäinen

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# List of publications

This dissertation consists of an overview and of the following publications.

**I** M. Kärkkäinen, D. Sandström, M. Varonen, and K. A. I. Halonen, “Transmission Line and Lange Coupler Implementations in CMOS,” in *Proc. of the European Microwave Integrated Circuits Conference*, Paris, France, Sept. 2010, pp. 357-360.

**II** M. Kärkkäinen, M. Varonen, D. Sandström, T. Tikka, S. Lindfors, and K. A. I. Halonen, "Design Aspects of 65-nm CMOS MMICs," in *Proc. of the European Microwave Integrated Circuits Conference*, Amsterdam, the Netherlands, Oct. 2008, pp. 115-118.

**III** D. Sandström, M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, "W-Band CMOS Amplifiers Achieving +10 dBm Saturated Output Power and 7.5 dB NF," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3403-3409, Dec. 2009.

**IV** M. Kärkkäinen, M. Varonen, P. Kangaslahti, and K. Halonen, ”Integrated Amplifier Circuits for 60 GHz Broadband Telecommunication,” *Analog Integrated Circuits and Signal Processing*, vol. 42, no. 1, pp. 37-46, Jan. 2005.

**V** M. Varonen, M. Kärkkäinen, M. Kantanen, and K. A. I. Halonen, ”Millimeter-Wave Integrated Circuits in 65-nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, pp. 1991-2002, Sept. 2008.

**VI** D. Sandström, M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, “60 GHz amplifier employing slow-wave transmission lines in 65-nm CMOS,” *Analog Integrated Circuits and Signal Processing*, vol. 64, no. 3, pp. 223-231, Sept. 2010.

**VII** M. Varonen, M. Kärkkäinen, J. Riska, P. Kangaslahti, and K. Halonen, ”Resistive HEMT Mixers for 60-GHz Broad-Band Telecommunication,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 4, pp. 1322-1330, Apr. 2005.

**VIII** M. Kärkkäinen, M. Varonen, M. Kantanen, T. Karttaavi, R. Weber, A Leuther, M. Seelmann-Eggebert, T. Närhi, and K. A. I. Halonen, ”Coplanar 94 GHz Metamorphic HEMT Low Noise Amplifiers,” in *IEEE Compound Semiconductor IC Symposium Technical Digest*, San Antonio, TX, Nov. 2006, pp. 29-32.

**IX** M. Varonen, M. Kärkkäinen, M. Kantanen, M. Laaninen, T. Karttaavi, R. Weber, A. Leuther, M. Seelmann-Eggebert, T. Närhi, J. Lahtinen, and K. A. I. Halonen, ”W-band low-noise amplifiers,” *Proceedings of the European Microwave Association*, vol. 3, no. 4., pp. 358-366, Dec. 2007.

**X** M. Kantanen, M. Kärkkäinen, M. Varonen, M. Laaninen, T. Karttaavi, R. Weber, A Leuther, M. Seelmann-Eggebert, T. Närhi, J. Lahtinen, and K. Halonen, “Low noise amplifiers for D-band,” *Proceedings of the European Microwave Association*, vol. 4, no. 4., pp. 268-275, Dec. 2008.

**XI** M. Kärkkäinen, M. Kantanen, S. Caujolle-Bert, M. Varonen, R. Weber, A. Leuther, M. Seelmann-Eggebert, A. Alanne, P. Jukkala, T. Närhi, and K. A. I. Halonen, “MHEMT G-Band Low-Noise Amplifiers,” *IEEE Transactions on Terahertz Science and Technology*, vol. 4, no. 4, pp. 459-468, Jul. 2014.

**XII** M. Varonen, M. Kärkkäinen, J. Riska, P. Kangaslahti, and K. Halonen, ”Up- and Downconverter MMICs for 60-GHz Broad-Band Telecommunication,” in *IEEE MTT-S International Microwave Symposium Dig.*, San Francisco, CA, Jun. 2006, pp. 1501-1504.

**XIII** M. Kärkkäinen, M. Varonen, D. Sandström, and K. A. I. Halonen, “60-GHz Receiver and Transmitter Front-Ends in 65-nm CMOS,” in *IEEE MTT-S International Microwave Symposium Dig.*, Boston, MA, Jun. 2009, pp. 577-580.

# Author’s contribution

**Publication I: “Transmission Line and Lange Coupler Implementations in CMOS”**

This publication was the result of a collaborative effort. The author designed various transmission line structures in 65-nm CMOS technology. The author also measured and analyzed the results. The Lange coupler presented in the study was designed and implemented by Dan Sandström and Mikko Varonen.

**Publication II: “Design Aspects of 65-nm CMOS MMICs”**

This publication was the result of a collaborative effort. The author was responsible for writing most of the paper. The author contributed to the design and analysis of the transmission line structures and also designed and analyzed the transistor’s test structure. The transistor’s layout was designed by Tero Tikka.

**Publication III: “W-Band CMOS Amplifiers Achieving +10 dBm Saturated Output Power and 7.5 dB NF”**

This publication was the result of a collaborative effort. The author was mainly responsible for the de-embedding of the transistor data model and the custom capacitor design for the 100 GHz amplifier. The slow-wave shield was designed by Mikko Varonen.

**Publication IV: “Integrated Amplifier Circuits for 60 GHz Broadband Telecommunication”**

This publication was mainly contributed by the author. The author was responsible for writing the manuscript. The author designed the low-noise amplifier and fitted the transistor noise model to the measured noise data. The measurements of the amplifier and transistor’s test structure were

carried out at the Millimetre Wave Laboratory of Finland. The sections concerning the transistor's characterization and the low-noise amplifier were written by the author.

**Publication V: "Millimeter-Wave Integrated Circuits in 65-nm CMOS"**

This publication was the result of a collaborative effort. The author has contributed to the analysis of the transistor and capacitor measurement data and de-embedding. The author has also contributed to the development of the coplanar waveguide structure on silicon. The measurements were carried out at the Millimetre Wave Laboratory of Finland. The section concerning the transistor's characterization was written by the author.

**Publication VI: "60 GHz amplifier employing slow-wave transmission lines in 65-nm CMOS"**

This publication was the result of a collaborative effort. The author was mainly responsible for the de-embedding of the transistor data model.

**Publication VII: "Resistive HEMT Mixers for 60-GHz Broad-Band Telecommunication"**

This publication was the result of a collaborative effort. The author has been involved in the image rejection mixer measurements in co-operation with M. Varonen, designed and analyzed one of hybrids and contributed to the writing of this article.

**Publication VIII: "Coplanar 94 GHz Metamorphic HEMT Low Noise Amplifiers"**

This publication was the result of a collaborative effort. The author designed one of the amplifiers and contributed to the writing of the paper. The measurements were carried out at the Millimetre Wave Laboratory of Finland.

**Publication IX: "W-band low-noise amplifiers"**

This publication was the result of a collaborative effort. The author designed one of the amplifiers and contributed to the writing of the paper.

The measurements were carried out at the Millimetre Wave Laboratory of Finland.

**Publication X: "Low noise amplifiers for D-band"**

This publication was the result of a collaborative effort. The author designed one of the amplifiers and contributed to the writing of the paper. The measurements were carried out at the Millimetre Wave Laboratory of Finland.

**Publication XI: "MHEMT G-Band Low-Noise Amplifiers"**

This publication was the result of a collaborative effort. The author designed one of the amplifiers and wrote the paper. The author was also involved in designing the second-run, 183-GHz amplifier and drew the layout for it. The circuit simulations for the second-run amplifier were carried out by Sylvain Caujolle-Bert. The different variations of the second-run simulations were suggested by Matthias Seelmann-Eggebert. The transistor simulations and analysis presented at the beginning of the paper were the work of the author. DA-Design Oy developed the split block package and handled the chip assembly. The measurements were carried out at the Millimetre Wave Laboratory of Finland.

**Publication XII: "Up- and Downconverter MMICs for 60-GHz Broad-Band Telecommunication"**

This publication was the result of a collaborative effort. The author designed the three-stage low-noise amplifier for the receiver front-end and helped develop the measurement setup and do the measurements. The resistive mixer was designed by Jan Riska. The section concerning the receiver front-end was written by the author.

**Publication XIII: "60-GHz Receiver and Transmitter Front-Ends in 65-nm CMOS"**

This publication was the result of a collaborative effort. The author designed the active downconversion mixer for the receiver front-end. The five-stage amplifier and spiral balun were designed by Mikko Varonen. The measurements were carried out partly by the Millimetre Wave Laboratory of Finland and partly by the author. The section concerning the receiver front-end was written by the author.

# List of abbreviations

| | |
|---|---|
| AC | alternating current |
| AD | analog-to-digital converter |
| ADS | Advanced Design System (simulation software from Agilent) |
| BB | baseband |
| $BB_I$ | in-phase baseband signal |
| $BB_Q$ | quadrature baseband signal |
| CE | common emitter |
| CG | common gate |
| CMOS | complementary metal-oxide semiconductor |
| CPU | central processing unit |
| CPW | coplanar waveguide |
| CPWCS | cut shield coplanar waveguide |
| CPWSW | slow-wave coplanar waveguide |
| CS | common source |
| dB | decibel |
| D-band | frequency band from 110 to 170 GHz |
| dBm | decibels relative to one milliwatt |
| DC | direct current |
| DSB | double sideband |
| E-band | frequency band from 60 to 90 GHz |
| F | noise factor |
| FET | field-effect transistor |
| GaAs | gallium arsenide |
| G-band | frequency band from 140 to 220 GHz |
| GCPW | grounded coplanar waveguide |
| GHz | gigahertz |
| GND | ground |
| GSG | ground-signal-ground probe configuration |
| HBT | heterojunction bipolar transistor |
| HEMT | high electron mobility transistor |
| Hz | Hertz |
| IC | integrated circuit |

| | |
|---|---|
| ICP | intercept point |
| IF | intermediate frequency |
| IN | input |
| InP | indium phosphide |
| IQ, I/Q | in-phase/quadrature-phase signal |
| IRR | image rejection ratio |
| $IRR_{dB}$ | image rejection ratio in decibels |
| $J_d$ | drain current density |
| l | length (also electrical length) |
| LNA | low-noise amplifier |
| LO | local oscillator |
| LRRM | line-reflect-reflect-match calibration method |
| LSB | lower sideband |
| mA | milliampere |
| MAG | maximum available gain |
| MHEMT | metamorphic high electron mobility transistor |
| MilliLab | Millimetre Wave Laboratory of Finland |
| MIM | metal-insulator-metal |
| mm | millimeter |
| $mm^2$ | square millimeter |
| MMIC | monolithic microwave integrated circuit |
| MOSFET | metal oxide semiconductor field effect transistor |
| MS | microstrip line |
| MSG | maximum stable gain |
| mW | milliwatt |
| NF | noise figure |
| nm | nanometer |
| NMOS | n-type metal-oxide semiconductor |
| OUT | output |
| PGA | programmable gain amplifier |
| pH | picohenry |
| PHEMT | pseudomorphic high-electron-mobility-transistor |
| PLL | phase locked loop |
| PS | phase shifter |
| QVCO | quadrature voltage-controlled oscillator |
| RF | radio frequency |
| RX | receiver |
| s, (s) | simulated value |
| SiGe | silicon germanium |
| SiGe:C | silicon germanium carbon |
| SOI | silicon-on-insulator |

| | |
|---|---|
| TRL | thru-reflect-line calibration method |
| USB | upper sideband |
| V, v | voltage |
| V-band | frequency band from 50 to 75 GHz |
| $V_{bias}$ | bias voltage |
| VCO | voltage-controlled oscillator |
| VDD | supply voltage |
| VGA | variable-gain amplifier |
| W | watt |
| W-band | frequency band from 75 to 110 GHz |
| WG | waveguide |
| W-HDMI | wireless high definition multimedia interface |
| WLAN | wireless local area network |
| X-band | frequency band from 8 to 12 GHz |

# List of symbols

| | |
|---|---|
| $A_{IM}$ | amplitude of the signal at the image frequency |
| $A_{LO}$ | amplitude of the signal at the local frequency |
| $A_{mix,x}$ | signal coming from a mixer (amplitude), branch x |
| $A_{RF}$ | amplitude of the signal at the radio frequency |
| B | bandwidth |
| $C_A$ | noise correlation matrix |
| $C_{db}$ | drain-bulk capacitance |
| $C_{ds}$ | drain-source capacitance |
| $C_{gs}$ | gate-source capacitance |
| $C_{si}$ | drain-bulk network capacitance |
| $F_{cas,min}$ | noise factor (or figure) of infinite number of cascaded transistors matched to optimum noise measure |
| $f_{MAX}$ | maximum frequency of oscillation |
| $F_X$ | noise factor of block number x |
| $g_m$ | transconductance |
| $G_X$ | gain of block number x |
| $i_d$ | drain noise current |
| $i_g$ | gate noise current |
| Im | imaginary part |
| j | imaginary unit |
| $J_d$ | drain current density |
| k | Boltzmann's constant, also Rollett's stability factor |
| L | length of transistor gate |
| $L_d$ | drain inductance |
| $L_g$ | gate inductance |
| $L_s$ | source inductance |
| $M_{OPT}$ | optimum noise measure matching |
| $N_f$ | number of transistor fingers |
| $N_{IN}$ | input noise power |
| $N_{OUT}$ | output noise power |
| $P_0$ | phase of the 0-phase signal branch |
| $P_{90}$ | phase of the 90-phase signal branch |

| | |
|---|---|
| $P_{180}$ | phase of the 180-phase signal branch |
| $P_{270}$ | phase of the 270-phase signal branch |
| $P_{IM}$ | signal power on the image frequency |
| $P_{RF}$ | signal power on the radio frequency |
| $R_d$ | drain resistance |
| $R_{ds}$ | drain-source resistance |
| Re | real part |
| $R_g$ | gate resistance |
| $R_{gs}$ | gate-source resistance |
| $R_n$ | noise resistance |
| $R_s$ | source resistance |
| S | gap width of a coplanar waveguide, also scattering parameter(s) |
| $s_{xx}$, $S_{xx}$ | s-parameter |
| T | noise temperature |
| $T_d$ | noise temperature of the drain resistance |
| $T_g$ | noise temperate of the gate resistance |
| $T_a$ | ambient temperature |
| $V_g$ | gate voltage |
| $V_d$ | drain voltage |
| W | center conductor width of a coplanar waveguide, also width of transistor gate |
| w | angular frequency (also $\omega$) |
| WR-*NN* | waveguide band, waveguide package with *NN*-band size connectors |
| $W_f$ | finger width of a transistor gate |
| $Z_0$ | characteristic impedance |
| $z_{00}$ | z-axis crossing point |
| $y_{xx}$, $Y_{xx}$ | y-parameter |
| $z_{xx}$, $Z_{xx}$ | z-parameter |
| | |
| $\Gamma_{opt}$ | optimum reflection coefficient |
| $\Delta A$ | amplitude difference |
| $\theta$ | phase difference |
| $\lambda$ | wavelength |
| $\omega$ | angular frequency, also w |
| $\Omega$ | ohm(s) |

# 1. Introduction

The demand for high-speed, short-range wireless data transfer has increased as high definition video and other digital multimedia content have become more widely available. Other prospective millimeter-wave applications include collision avoidance radar for a car, 60-GHz data communication, 71–86 GHz point-to-point networks, and security scanners, as well as medical and industrial sensors. As an example, a high data rate system is needed if one wants to send a high-definition video stream wirelessly from a media server to a flat-screen television hanging on opposite wall of a living room. The 60-GHz range has garnered a great deal of interest as a possible frequency for high data rate systems since a wide bandwidth is available license free worldwide [1][2]. Some possible millimeter-wave applications are presented in figure 1. A millimeter-wave radio system can also be a solution when the use of more crowded lower frequencies is not desired. However, this means that the millimeter-wave transceiver has to be manufactured in a cost-effective manner. Traditional millimeter-wave systems have been constructed from bulky and expensive waveguide parts, which are not suitable for portable and low-cost consumer applications. The millimeter-wave system should not consume much energy and it should not contain multiple parts that have to be manufactured with high levels of precision. The first microwave integrated circuit (MMIC) was introduced in 1976, which presents an integrated X-band amplifier [3].

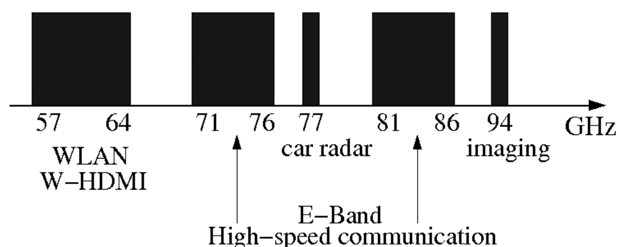



Fig. 1. Some possible millimeter-wave applications [4].

Previously, millimeter-wave-integrated circuits were manufactured using compound semiconductor technologies, such as gallium arsenide (GaAs) or indium phosphide- (InP) based high electron mobility transistors (HEMT). These technologies are now only rarely used in regular consumer applications and the wafer diameter can be 6 inches or even less. Digital memory, computer central processing units (CPU), digital signal processing, and so forth, are mostly integrated using complementary metal-oxide semiconductor (CMOS) technology. This means that there are obvious benefits to integrating millimeter-wave front-ends on the same microchip. The absence of bulky and cost-inefficient off-chip interconnections is one of the advantages of CMOS integration. Despite the fact that it is a promising technology, there may be challenges related to the manufacturing yield of highly integrated, large communication systems and to the low resistivity silicon substrate, which can introduce high noise levels and also be difficult to model accurately. Millimeter-wave CMOS circuits began to be developed between the years 2002 and 2007. One of the first circuits was a 51-GHz CMOS VCO [5]. Active and passive component modeling in particular was an issue; the 60-GHz band was of particular interest in 2004 [6], and in 2007 a 104-GHz CMOS amplifier was first developed [7]. Recently, good results from millimeter-wave amplifiers have been obtained with 45-nm SOI CMOS technology as well [8].

Outside the mass market millimeter-wave applications, there are scientific instruments that require the best possible performance regardless of yield, cost, and size or, sometimes, they require an optimum trade-off between these characteristics. For example, one scientific millimeter-wave application is atmospheric remote sensing of the Earth using radiometric instruments in a satellite. To understand the behavior of the Earth's atmosphere with ever greater precision, temperature and humidity profiling are of great interest. A humidity profile can be obtained from measurements of the water molecule absorption frequencies at 23 and 183 GHz. These results will be compared to radiometric data obtained from the atmospheric window frequencies of 90, 130, and 166 GHz. To improve the sensitivity of these profiling radar receivers, it is possible to use a high-performance, low-noise amplifier as the first component after the antenna, if such an amplifier can be designed and manufactured [9][10].

## 1.1 Objectives and contents of this dissertation

The objective of this dissertation is to present the design, analysis and results of millimeter-wave-integrated circuits. These circuits have been realized in various technologies, such as GaAs pseudomorphic and metamorphic HEMT and CMOS. The operating frequencies range from 60

to 183 GHz. Most of the work concentrates on low-noise amplifiers, although two different 60-GHz radio front-ends are also discussed in the study. The analysis section concentrates on silicon transistor small-signal modeling issues and transmission line structures on silicon and compares them to similar structures on GaAs. The transistor noise is characterized as well. The transistor model is verified by comparing it to the measured results obtained from three different amplifiers operating at 60 and 100 GHz.

The first part of the dissertation discusses the design issues and questions related to transmission lines. Then, small-signal transistor modeling is presented. Some system and design issues as well as the applied measurement techniques are likewise discussed. Subsequently, experimental results from several integrated circuits are presented and compared to previously published results. The conclusions are summarized and issues related to future work are discussed. In the second part of the dissertation, the published papers are presented.

# 2. Passive components

In millimeter-wave circuits, passive components, such as transmission lines and capacitors, can be used for matching purposes. Transmission lines are necessary for signal transfer as well. The passive components, which were available in the design kit, were not modeled at millimeter-wave frequencies and they may have large and unpredictable parasitics. In CMOS integrated circuits, it may not be obvious how to create the layout and model the behavior of these components. In the following section, transmission lines and capacitors are discussed in more detail.

## 2.1 Transmission lines

For high frequency circuit applications a transmission line structure can be used. Transmission lines are inherently scalable in length and once properly characterized, these lines can be used in many circuit blocks for signal transfer and matching purposes [11][Publication I][Publication II]. The transmission line structures are of particular interest for millimeter-wave CMOS circuits, because the losses caused by the substrate, metals, and dielectrics may increase attenuation to infeasible or unpractical levels. Figure 2 shows an example of a transmission line structure. This structure has been designed for CMOS technology and it fulfills the metal density requirements even when no dummy metal fillings are allowed inside the structure. The downward-extended ground planes are drawn with lower metal layers to fulfill the metal density requirements of the manufacturing technology. A floating shield consisting of narrow strips drawn using the lower metal layers can be realized perpendicular to the current flow in the CPW center conductor [12][13]. This type of a line creates a slow-wave CPW (CPWSW) structure, which has a longer electrical length than a conventional CPW with the same geometrical length. Although the slow-wave CPW has a higher self-resonance quality factor, it also has a more limited range of feasible characteristic impedances compared to a conventional coplanar waveguide. This is because the capacitance per unit length is increased, whereas the inductance is approximately the same as

for a conventional CPW having the same W and S [14]. For a high-impedance slow-wave CPW line the signal-to-ground spacing can be increased or the width of the signal line can be decreased. However, the signal-to-ground spacing is limited by the design rules while the width of the center conductor is limited by metallic losses [Publication I].

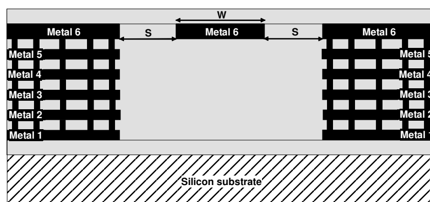



Fig. 2. A simplified CPW structure realized on silicon. (© 2010 EuMA, with permission from [Publication I]).

In this work, a third type of CPW type was developed as a test structure in CMOS. The slow-wave shield grid was cut at the center points of the slots of the CPW. The structure of the cut shield CPW (CPWCS) and the slow-wave CPW (CPWSW) are shown in figure 3. The idea of this third type of CPW is to decrease the capacitance of the line (thus, increase characteristic impedance) and maintain reasonable substrate shielding. With a narrower center conductor (8 µm width and 11 µm gap) it is possible to increase the line inductance, and, thus, the impedance, even further. Ways to change the line capacitance have also been discussed elsewhere [15]. The substrate shield of the lines is created using the two lowest metal levels [Publication I].

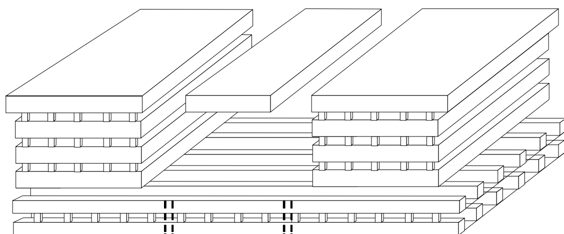


Fig. 3. A simplified CPW structure realized on silicon with a floating shield underneath. The dashed lines show where the cut shield version has been cut. (© 2010 EuMA, with permission from [Publication I]).

To characterize the CPW-lines, the test structures were measured on-wafer and the parasitic shunt capacitances of the pads were subtracted from the line measurement result. Figure 4 shows one of the developed test structures. The characteristic impedance, attenuation and propagation

factors were calculated using equations found in a prior study [16]. The results have been compiled in table 1.

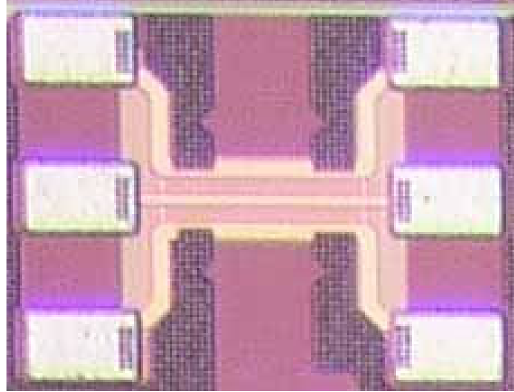


Fig. 4. A micrograph of the cut shield CPW test structure in 65-nm CMOS. The line length, excluding pads and transitions, is 215 μm. (© 2010 EuMA, with permission from [Publication I]).

Table 1. Comparison of the different transmission line realizations in 65-nm CMOS at 60 GHz [Publication I]. The GaAs CPW results have been simulated for purposes of comparison.

| | W [μm] | S [μm] | $Z_0$ [Ohm] | A [dB/mm] | A / λ [dB / λ] |
|---|---|---|---|---|---|
| **CPW** | 12 | 9 | 55 | 3 | 5 |
| **CPWCS** | 8 | 11 | 67 | 2 | 3.3 |
| **CPWSW** | 12 | 9 | 40 | 2 | 2.5 |
| **CPWSW8** | 8 | 11 | 55 | 1.4 | 2.1 |
| | | | | | |
| **GaAs GCPW** | 37 | 6.5 | 31 * | 0.6 * | 1.2 * |
| **GaAs GCPW** | 17 | 16.5 | 52 * | 0.4 * | 0.8 * |
| **GaAs GCPW** | 7 | 21.5 | 69 * | 0.5 * | 1.1 * |

* Simulated using design kit models for comparison purposes.

## 2.2 Capacitors in CMOS

Millimeter-wave integrated circuits typically utilize capacitors for RF short-circuiting and DC-decoupling purposes. The capacitors may also be used as part of a matching circuit. In CMOS technology, the metal-insulator-metal (MIM) capacitor is one of the simplest types of capacitors. It is simple to model and the parasitics are easy to predict as opposed to complex, interleaved finger capacitors that use several metal levels and both sidewall and plate capacitances between the fingers. However, the MIM capacitors

may not be available in a chosen technology and library finger capacitors in a design kit may have large and unpredictable parasitics. To overcome this problem, a custom capacitor, which has wide separate fingers drawn with upper metal levels, was designed in this work. This is done to minimize the ground capacitance from the lower levels to the substrate and decrease the parasitic series resistances and inductances by using wide fingers instead of a large number of narrow fingers [Publication III]. Of course, the drawback in the case of wide fingers is the reduced capacitance per unit area. This may not become a problem if the operating frequency is quite high (100 GHz or higher) and, thus, the required capacitances are small.

# 3. Transistor

A fast transistor is needed, when trying to improve the amplifier performance to the 60-GHz range and even beyond. One convenient way to measure the transistor speed is the maximum frequency of oscillation, since this is also the frequency of unity power gain. The gain of the transistor can be evaluated as a function of frequency by using the maximum stable gain (MSG), when $k < 1$, and the maximum available gain, when $k > 1$. At high enough frequencies, the gain of a transistor is limited by the parasitics and not by its stability. By trying to minimize the gate resistance, it is possible to obtain lower minimum noise figure and high $f_{MAX}$, which results higher available gain. The optimum values for the width of a single finger $W_f$ and drain current density $J_d$ are approximately 1 µm and 0.20 mA/µm, respectively [17][18]. These values give the best $f_{MAX}$ and, thus, the best maximum available gain. For the optimum noise figure a value of 0.15 mA/µm has been proposed [17][18]. The noise performance can be further optimized by selecting the best number of gate fingers $n_f$ for the transistor. The noise figure is minimized by selecting a large $n_f$, because of the reduced total gate resistance. However, the number of gate fingers $n_f$ cannot be increased arbitrarily, because at some point the increased drain current (assuming constant drain current density scaling) will eventually produce more noise and result in a higher noise figure [19][20]. Figure 5 shows the basic principle behind the transistor layout.

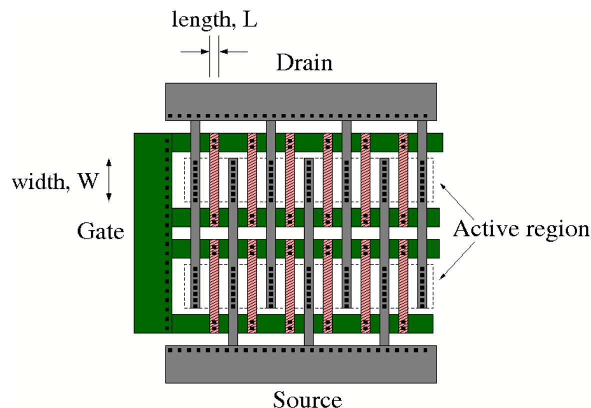
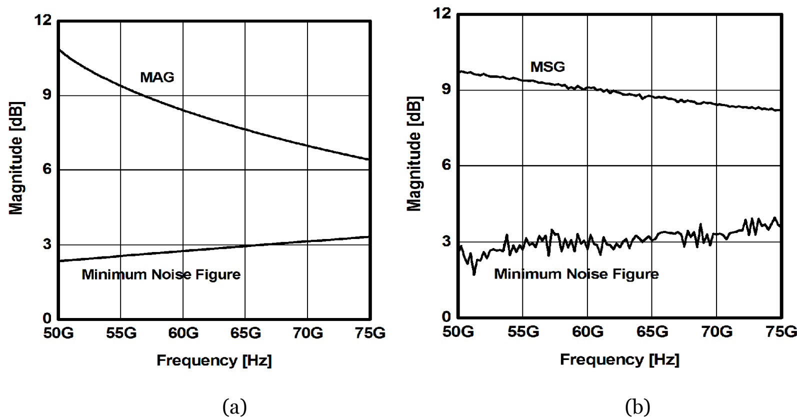



Fig. 5. Transistor layout. (© 2009 IEEE, with permission from [Publication III])

The width of the transistor finger and current density can be selected to maximize the $f_{MAX}$ and, thus, the maximum available gain at high frequencies (k > 1). The number of fingers in each transistor and, eventually, the number of transistors in parallel can be selected by looking at the minimum noise figure, gain, power consumption, and linearity. The impedances required for matching can also be one of the limiting factors. The maximum stable gain and the minimum noise figure are approximately the same for different numbers of transistors and fingers, when considering a constant drain current density [21][22]. The $f_{MAX}$, the related maximum available gain (MAG) at high frequencies (k > 1), dc current consumption, and noise figure will be affected and they are important parameters when considering the low-noise amplifier design.

As an example, figure 6 compares a 2x25 µm GaAs-PHEMT and a 90-µm, 65-nm CMOS transistor in terms of their gain and noise. Their performance is quite similar and shows the potential of CMOS technology for millimeter-wave applications. Both transistors have approximately 7–9 dB of gain and a 3–dB minimum noise figure from 55 to 60 GHz.



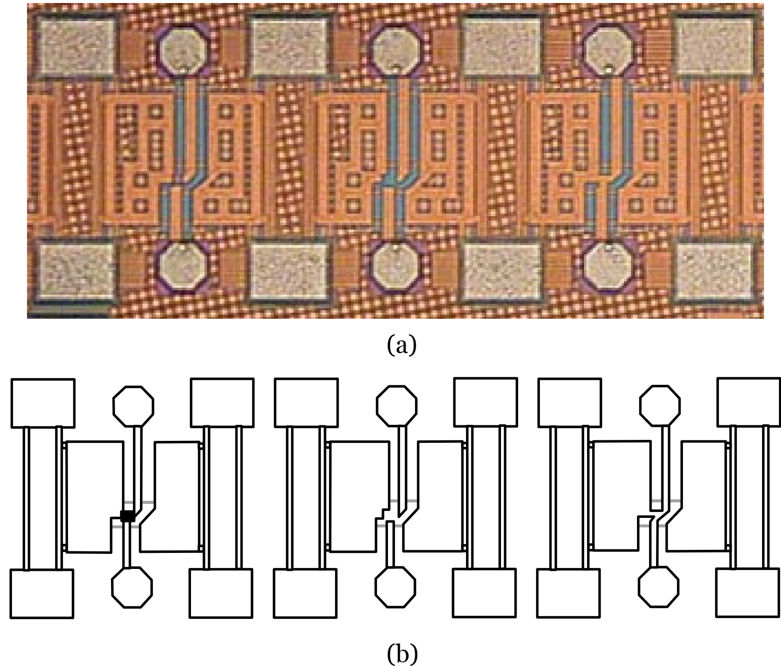

(a) (b)

Fig. 6. The maximum stable and available gain (MSG/MAG) and minimum noise figure ($NF_{min}$) are simulated for a 0.15-µm GaAs pseudomorphic HEMT having a gate width of 2x25 µm (a) and measured for an NMOS having a total width of 90 µm in 65-nm CMOS (b) [Publication IV] [Publication V].

## 3.1 Transistor model

When CMOS design first began, there was no small-signal model or noise model available for the 90/0.07-µm NMOS transistor chosen as a suitable size for the V-band designs. This size was also the smallest of the originally available test set of transistors. In this work the transistor is de-embedded using open-short de-embedding [23] and a test structure is used that has a well-defined impedance and reasonable loss at the millimeter-wave

frequencies. The coplanar waveguide interconnections to the input and output pads were seen as a viable choice for the test structure. Figure 7 shows a micrograph of the realized test structure. The accuracy of the de-embedding is degraded after 80 GHz [Publication V]. Recently, there has been a study indicating that it is possible to simulate transistors with SOI CMOS design kit models and RC-parasitics extraction up to 75 GHz accurately [8].



(a)

(b)

Fig. 7. Coplanar test structures for characterizing the transistor. The chip area is 0.7 x 0.3 $mm^2$. From left to right: transistor, open, and short test structure. Both a micrograph of the test structure (a) and a simplified layout drawing principle (b) are depicted.

In order to remove the effect of the connecting lines from the transistor measurement, the measured data has to be de-embedded first. The de-embedding is performed by using the open-short method [23]. There are issues related to characterizing the transistor at high frequencies when using scattering parameter measurements and test structures. These are the parasitics of the test structure, which have a pronounced effect and, the gain of the transistor, which is low above 110 GHz [24].

There are different ways to create a small-signal model, but some of them require several measurements and optimizations [25][26]. The goal in this work was to obtain an acceptable small-signal model for V-band circuit design in CMOS technology based on a single measured frequency sweep of a saturated transistor and the s-parameters of the corresponding open and short structures. To do this, the extrinsic parasitics are evaluated [25]. The values for $R_g$, $R_d$, $R_s$, and $L_d$ were evaluated by fitting a line to the measured

data as shown in figures 10, 11, 12, and 13, respectively. The gate inductance, $L_g$, calculation requires two linear fitted lines and an additional fitted plane in three-dimensional space as in figures 14, 15, and 16, respectively. The resistances are evaluated using measured data from 34 to 60 GHz, whereas the data range for the inductances is from 70 to 110 GHz. These frequency ranges were selected to obtain a good linear fit and, thus, to reduce the effect of other frequency-dependent terms on the transistor's z-parameters.

The source parasitic inductance was evaluated separately from the short test structure [27] and later adjusted to minimize the frequency dependence of the transconductance in an iterative way since the $L_g$ and $L_d$ depend on the $L_s$. The transconductance can be plotted as a function of frequency for three different source inductance values (fig. 8) for the W/L = 90/0.07-µm NMOS test transistor.

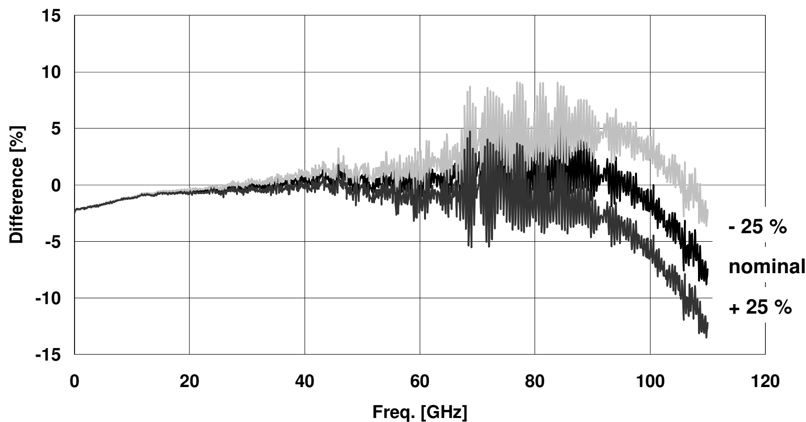



Fig. 8. The frequency dependence of the transconductance. The value for the source inductance is chosen to obtain as flat a transconductance as possible. In this case the nominal source inductance is 1.7 pH.

The series and shunt parasitics can then be subtracted from the de-embedded transistor data [28]. The configuration of the extrinsic parasitics can be varied according to the test structure [29]. However, here it was discovered that the residual shunt capacitances are practically negligible. Finally, the intrinsic transistor component values can be calculated in a straightforward manner if the extrinsic parasitics are subtracted correctly [30]. However, the drain substrate network formed with the source and bulk connections needs special attention, because the conventional small-signal model does not model its frequency dependence correctly [31]. The transistor model is presented in figure 9.

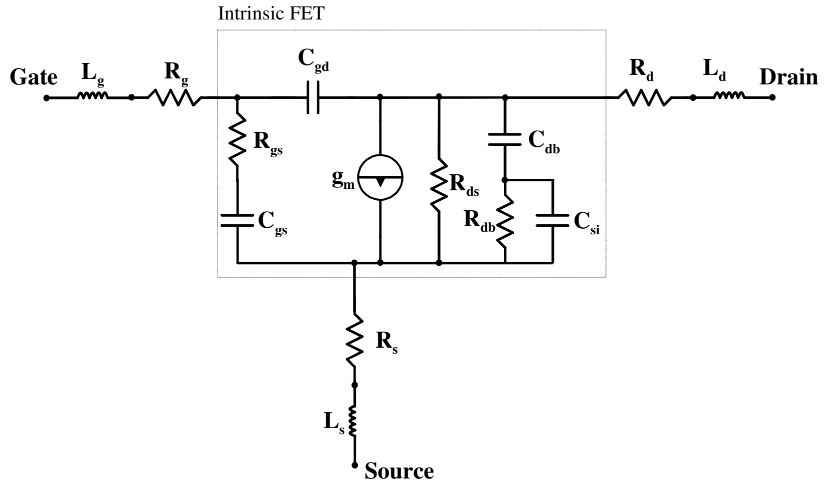



Fig. 9. The transistor model.

The source resistance can be evaluated using a parametric plot using de-embedded transistor's z-parameters as follows

$$[x_1, x_2] = [\mathrm{Re}\{Z_{12}\}, \mathrm{Re}\{Z_{21}\}], \quad (1)$$

which is plotted in figure 10. Then, using a fitted line, the value of the source resistance can be simply calculated as

$$R_s = \frac{ICP}{1 - \frac{dx_2}{dx_1}}, \quad (2)$$

where ICP is the x-axis intercept point and $dx_2/dx_1$ is the slope of the line.

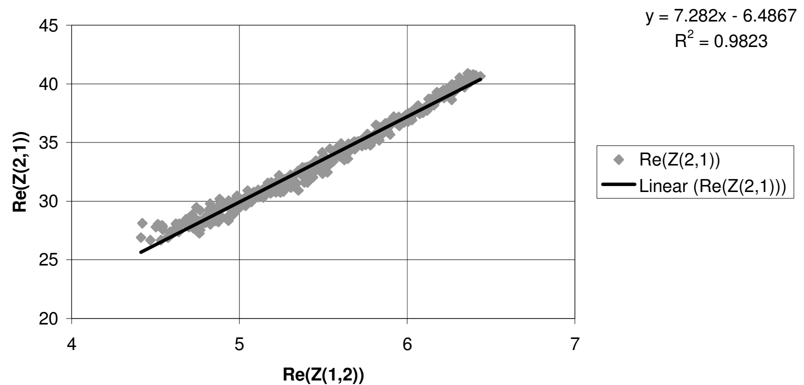



Fig. 10. A parametric plot for calculating the source resistance.

The values of the drain and gate resistances can be found in the same manner by plotting

$$[x_1, x_2] = [\mathrm{Re}\{Z_{22}\}, \mathrm{Re}\{Z_{12}\}], \tag{3}$$

and

$$[x_1, x_2] = [\mathrm{Re}\{Z_{11}\}, \mathrm{Re}\{Z_{21}\}], \tag{4}$$

respectively. These plots are presented in figures 11 and 12. The values are calculated as

$$R_d = \frac{ICP - R_s}{-\frac{dx_2}{dx_1}} - R_s, \tag{5}$$

and

$$R_g = \frac{ICP - R_s}{-\frac{dx_2}{dx_1}} - R_s, \tag{6}$$

where ICP is the x-axis intercept point and $dx_2/dx_1$ is the slope of the corresponding line.

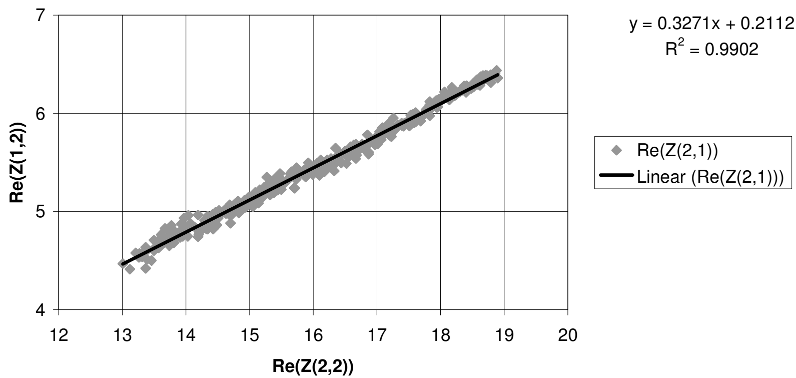



Fig. 11. A parametric plot for calculating the drain resistance.

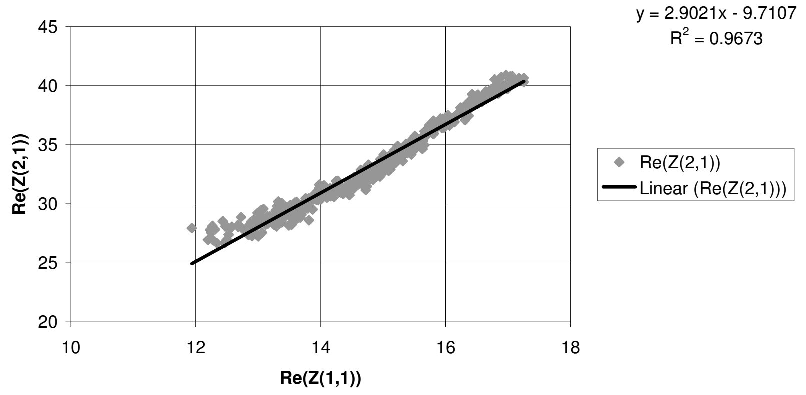



Fig. 12. A parametric plot for calculating the gate resistance.

The drain inductance can be found by plotting

$$[x_1, x_2] = \left[ \frac{\mathrm{Im}\{Z_{22}\}}{\omega}, \frac{\mathrm{Im}\{Z_{12}\}}{\omega} \right] \tag{7}$$

as in figure 13. From the fitted line, the value can then be calculated as follows:

$$L_d = \frac{ICP - L_s}{-\frac{dx_2}{dx_1}} - L_s , \tag{8}$$

where ICP is the intercept point, $dx_2/dx_1$ is the slope of the line, and $L_s$ is the source inductance.

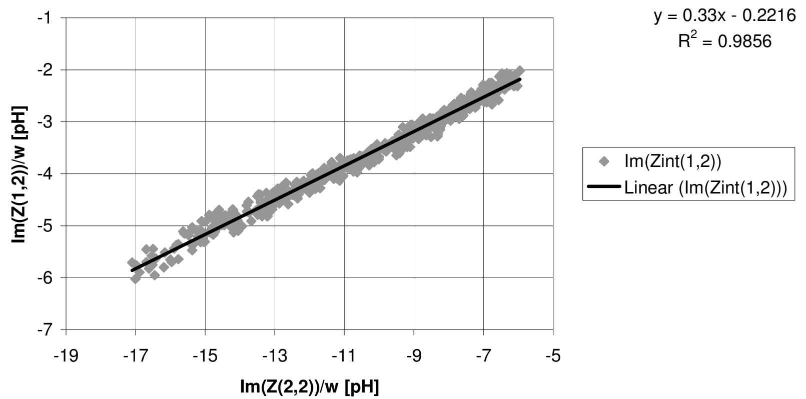



Fig. 13. A parametric plot for calculating the drain inductance.

Calculating the gate inductance requires three plots: Two 2-dimensional plots and an additional three-dimensional plot. A line must be fitted to the first and second plot and then a plane must be fitted to the third plot as in figures 14–16. The three-dimensional parametric plot can be created using the following equation:

$$[x_1, x_2, x_3] = \left[\frac{\operatorname{Im}\{Z_{21}\}}{\omega}, \frac{\operatorname{Im}\{Z_{12}\}}{\omega}, \frac{\operatorname{Im}\{Z_{11}\}}{\omega}\right], \tag{9}$$

which represents a plane of form ax+by+cz+d=0. It crosses the z-axis at point

$$z_{00} = -\frac{d}{c}. \tag{10}$$

The gate inductance value can then be found as follows:

$$L_g = z_{00} - L_s \cdot \left(1 - \frac{dx_3}{dx_1} - \frac{dx_3}{dx_2}\right) \tag{11}$$

where $dx_3/dx_1$ and $dx_3/dx_2$ are slopes of the corresponding two dimensional parametric plots:

$$[x_1, x_2] = \left[\frac{\operatorname{Im}\{Z_{21}\}}{\omega}, \frac{\operatorname{Im}\{Z_{11}\}}{\omega}\right] \tag{12}$$

and

$$[x_1, x_2] = \left[\frac{\operatorname{Im}\{Z_{12}\}}{\omega}, \frac{\operatorname{Im}\{Z_{11}\}}{\omega}\right], \tag{13}$$

respectively.

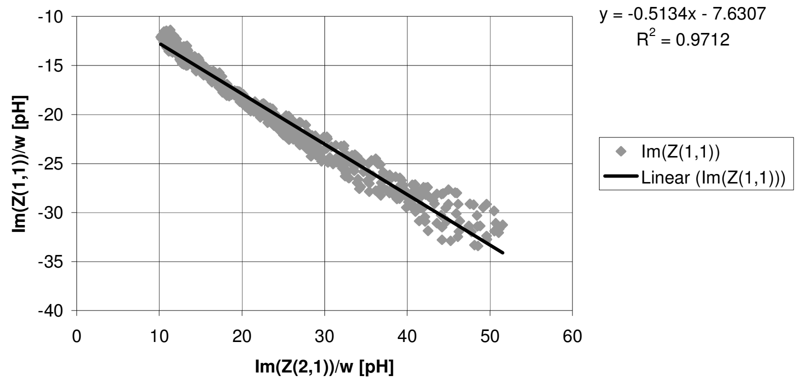



Fig. 14. A parametric plot for calculating the gate inductance.

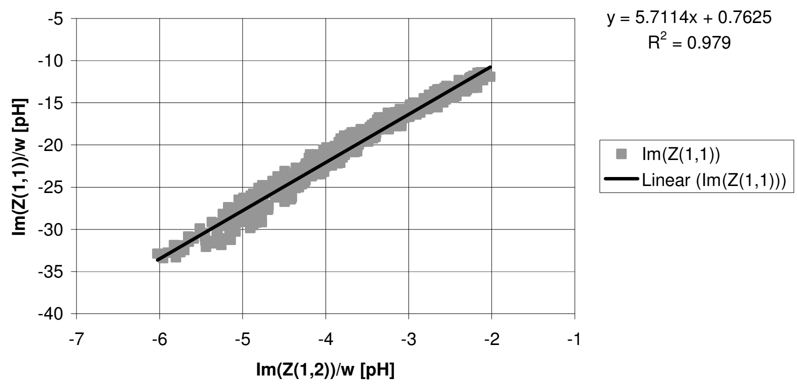



Fig. 15. A parametric plot for calculating the gate inductance.

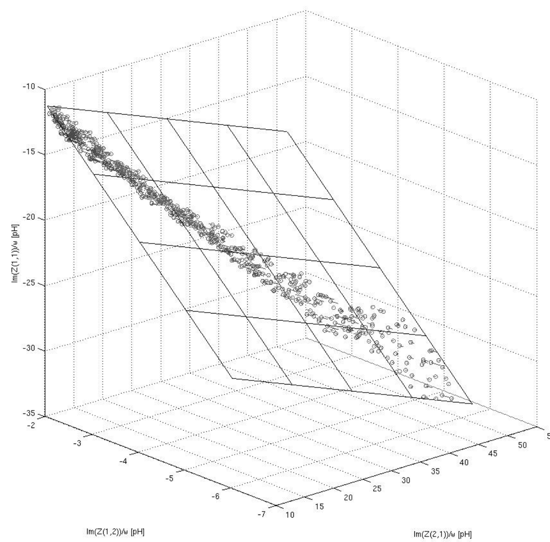



Fig. 16. A 3-dimensional parametric plot for calculating the gate inductance.

Finally, the extrinsic parasitics are shown in table 2. The source inductance is the only iterated value and all of the other values are calculated based on the properties of the parametric plots presented above.

Table 2. The extrinsic parasitics of the measured transistor.

| | | |
|---|---|---|
| Rs | 1.00 | [Ohm] |
| Rd | 1.50 | [Ohm] |
| Rg | 2.67 | [Ohm] |
| Ls | 1.70 | [pH] |
| Ld | 4.10 | [pH] |
| Lg | 5.40 | [pH] |

After removing the effect of the extrinsic parasitics, the intrinsic transistor elements can be calculated. The variation over frequency of the intrinsic elements is presented in figures 17–20.

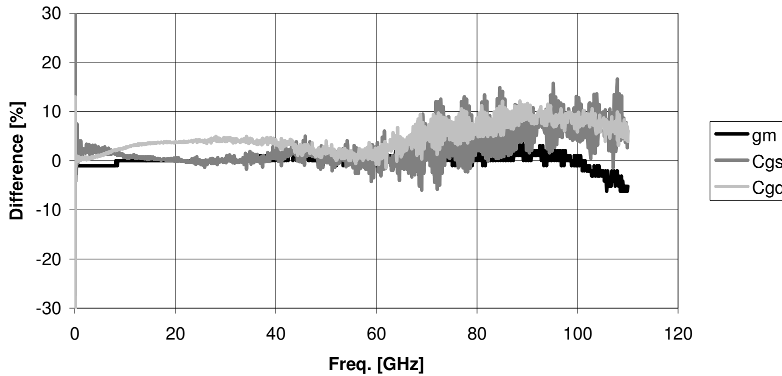



Fig. 17. The variation in transconductance, gate-to-source capacitance, and gate-to-drain capacitance of the measured transistor.

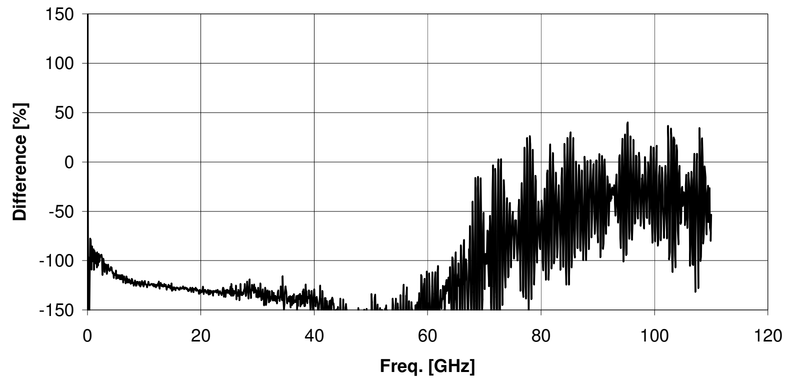



Fig. 18. The variation in gate-to-source resistance of the measured transistor.

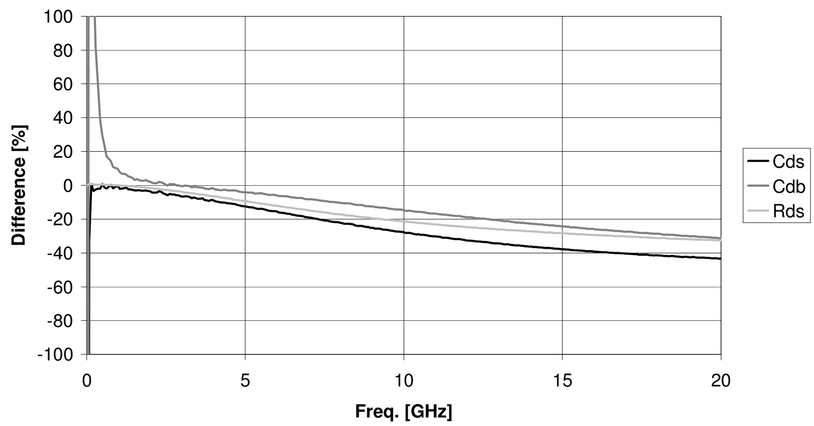



Fig. 19. The variation in drain-to-source capacitance, drain-to-bulk capacitance and drain-to-source resistance of the measured transistor. The values were obtained from low frequencies.

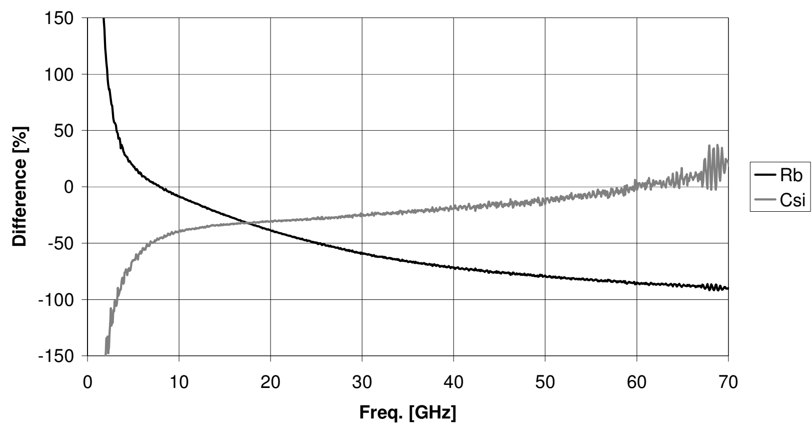



Fig. 20. The variation in bulk resistance and capacitance-to-silicon of the measured transistor. The values were obtained at a frequency of approximately 30 GHz.

### 3.2 Noise characteristics

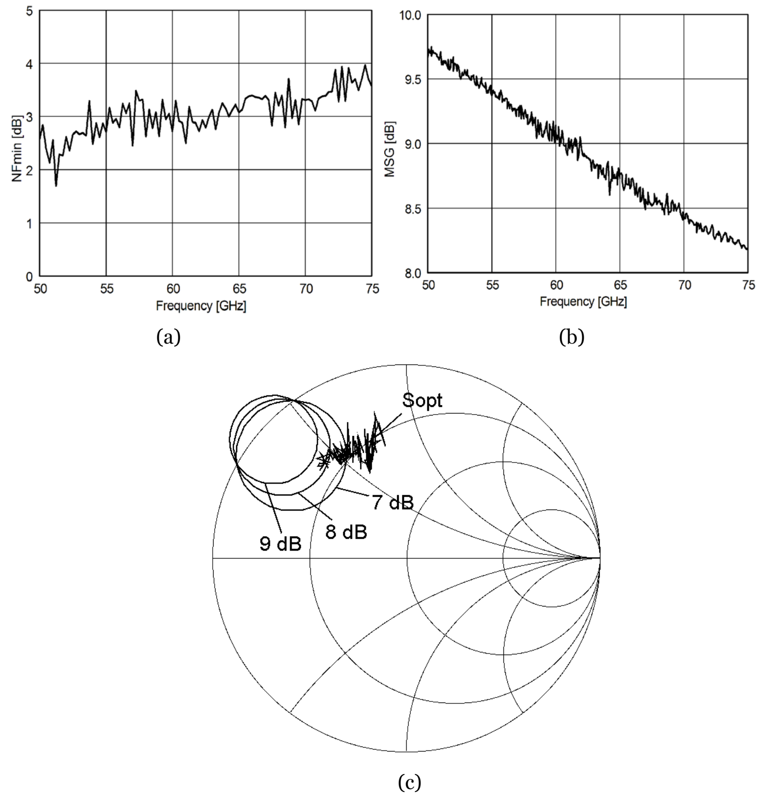
There has been a need to model the transistor noise characteristics, particularly at the V-band, to enable a low-noise amplifier design and accurate noise simulations. The pseudomorphic HEMT 2x25-μm transistor was measured in a test structure configuration and the scattering parameters were de-embedded using negative length transmission lines [32]. The geometry of the transmission line was approximated in ADS simulations using a coplanar waveguide model with average values for the center conductor and ground gaps. In the case of the noise parameters, the coplanar lines were added to the input and output of the small-signal transistor model (provided by the foundry). Then, the temperature of the resistors inside the small-signal model was set to 295 kelvins and the temperature of the drain resistor was adjusted until the simulation results resembled the measured noise parameters. Finally, the connecting lines could be removed and the model could be used for designing low-noise amplifiers [Publication IV]. There was no need for the gate resistor temperature to be higher than the ambient value. This type of a temperature noise model was originally presented in [33]. The effect of correlating noise sources can also be included [34].

Because it was assumed that the losses of the connecting lines would be significantly larger than in the case of the HEMT, a precise noise de-embedding is necessary for the MOSFET. The loss and other characteristics are discussed in detail in chapter 2. By measuring the scattering parameters of the corresponding open and short structures it is possible to calculate the noise correlation matrices for the series and shunt impedances and remove their effect from the noise parameters of the entire transistor test structure [35]. The noise parameters of the transistor's test structure were measured using methods described in [36]. The noise correlation matrices $C_{A,OPEN}$ and $C_{A,SHORT}$ for the open and short test structures can be computed simply based on the measured y-parameters as

$$C_A = 2kT_a \operatorname{Re}(Y), \tag{14}$$

where k is Bolzmann's constant, $T_a$ the ambient temperature and Y is the admittance matrix of the structure. The results are shown in figure 21. The de-embedded result shows a minimum noise figure of 3.0 dB for the W/L = 90/0.07 μm –sized NMOS transistor biased to 200 μA/μm current density at 60 GHz. The small-signal model, including the gate and drain

noise sources, is presented in figure 22. After removing the effect of the test structures and the extrinsic parasitics, the values for the noise sources and their correlation are presented in figures 23 and 24, respectively.




(a) (b)

(c)

Fig. 21. The minimum noise figure (a), maximum stable gain (b) and optimum noise input match with available gain circles (c) are plotted for a 90 µm NMOS transistor in 65-nm CMOS at V-band. The transistor drain current density is 0.2 mA/µm. (© 2008 IEEE, with permission from [Publication V]).

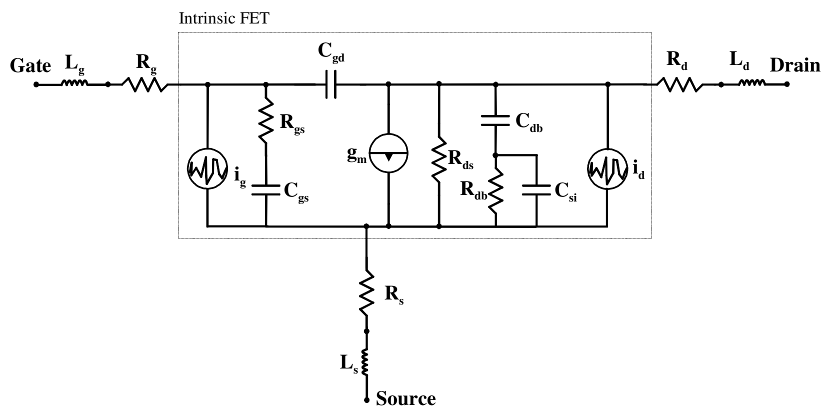



Fig. 22. The transistor model with the noise sources.

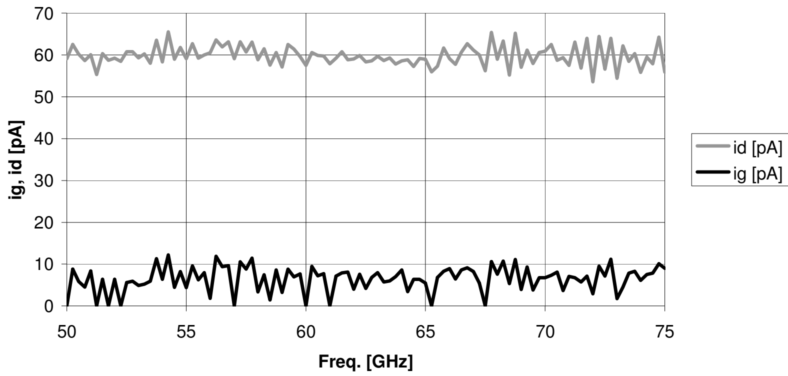



Fig. 23. The calculated gate and drain noise sources.

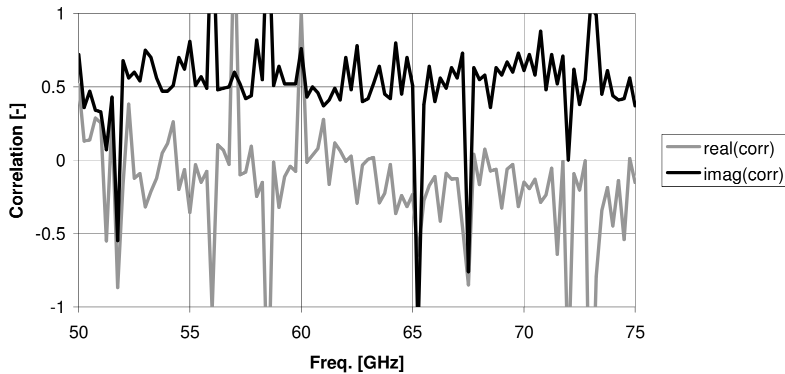



Fig. 24. The calculated correlation between the gate and drain noise sources.

## 3.3 Comparison to experimental amplifier results

As an example, simulations from three different amplifier designs are presented in this section. The results were simulated using the transistor small-signal model that was described in the previous section. The first version of the 60-GHz amplifier was manufactured in the same process run as the transistor test structures that were used for the transistor modeling [Publication V]. The second version of the 60-GHz amplifier and a 100-GHz amplifier were manufactured in a later process run [Publication III][Publication VI]. These circuits were designed by Mikko Varonen and Dan Sandström and the author re-simulated them using the presented transistor model. From figures 25-30 it is possible to see, how the modeled values match quite well with the measured results in the case of versions 1 and 2 of the 60-GHz amplifier as well as that of the 100-GHz amplifier. Version 1 of the 60-GHz amplifier experienced an unexpected gain spike,

which vanishes with a lower transconductance. However, the amplifiers from the later process run (version 2 of the 60-GHz amplifier and the 100-GHz amplifier) can have transistors that have a higher transconductance. This result can be explained with run-to-run variations.

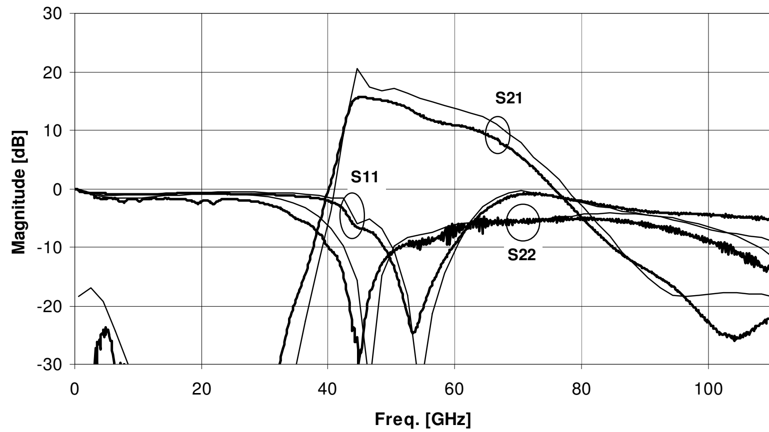



Fig. 25. Simulated (thin) and measured (thick) S11, S22, and S21 are plotted from 10 MHz to 110 GHz for the version 1 of the 60-GHz amplifier.

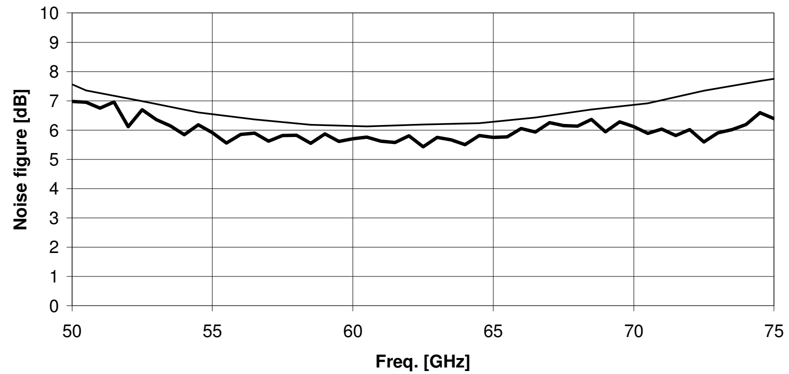



Fig. 26. Simulated (thin) and measured (thick) noise figures are plotted from 50 to 75 GHz for the version 1 of the 60-GHz amplifier.

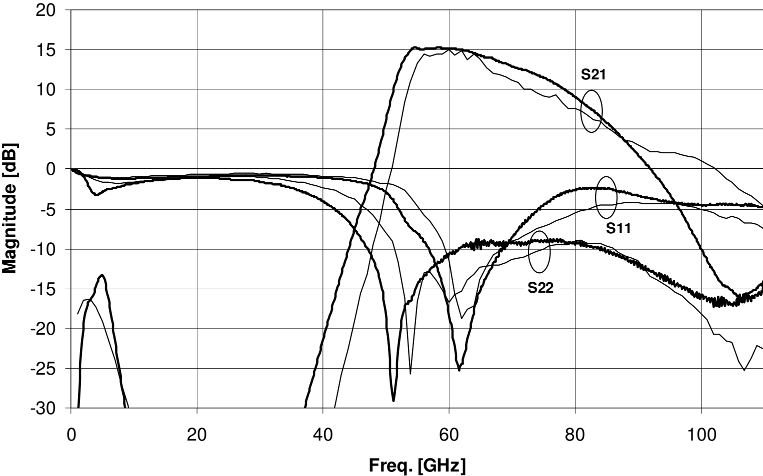



Fig. 27. Simulated (thin) and measured (thick) S11, S22, and S21 are plotted from 10 MHz to 110 GHz for the version 2 of the 60-GHz amplifier.

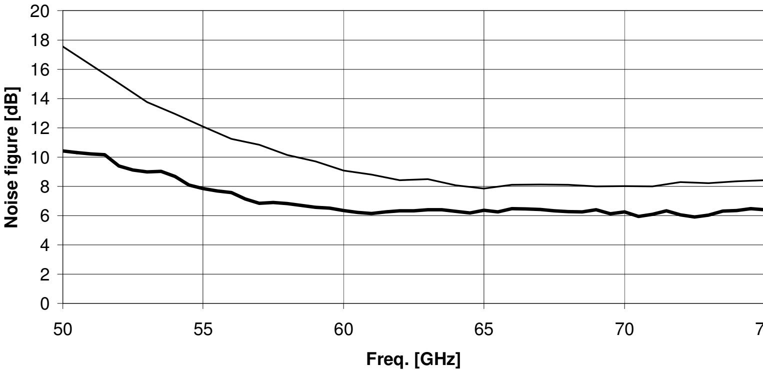



Fig. 28. Simulated (thin) and measured (thick) noise figures are plotted from 50 to 75 GHz for the version 2 of the 60-GHz amplifier.

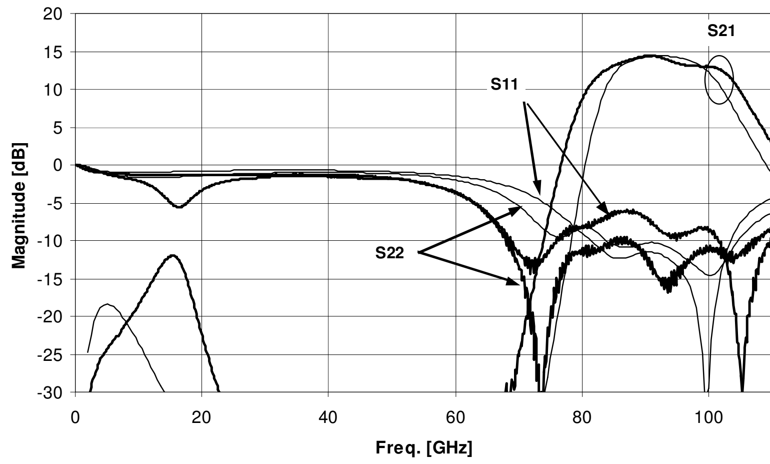



Fig. 29. Simulated (thin) and measured (thick) S11, S22, and S21 are plotted from 10 MHz to 110 GHz for the 100-GHz amplifier.

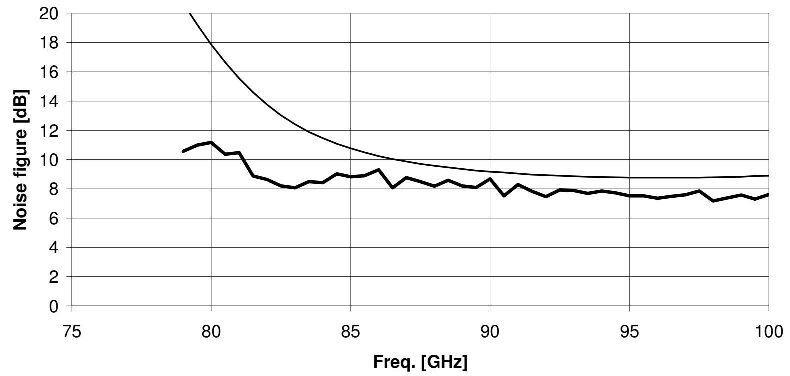



Fig. 30. Simulated (thin) and measured (thick) noise figures are plotted from 75 to 100 GHz for the 100-GHz amplifier.

# 4. Receiver system

Two types of receiver front-ends are presented in figure 31. The superheterodyne and direct conversion techniques were developed approximately 100 years ago [37]-[41]. There are many ways to assess the performance of the receiver front-end, including the sensitivity and dynamic range that the receiver is capable of coping with and the level of interference that the receiver can tolerate. Power consumption can also be a limiting factor, if battery operation is required.

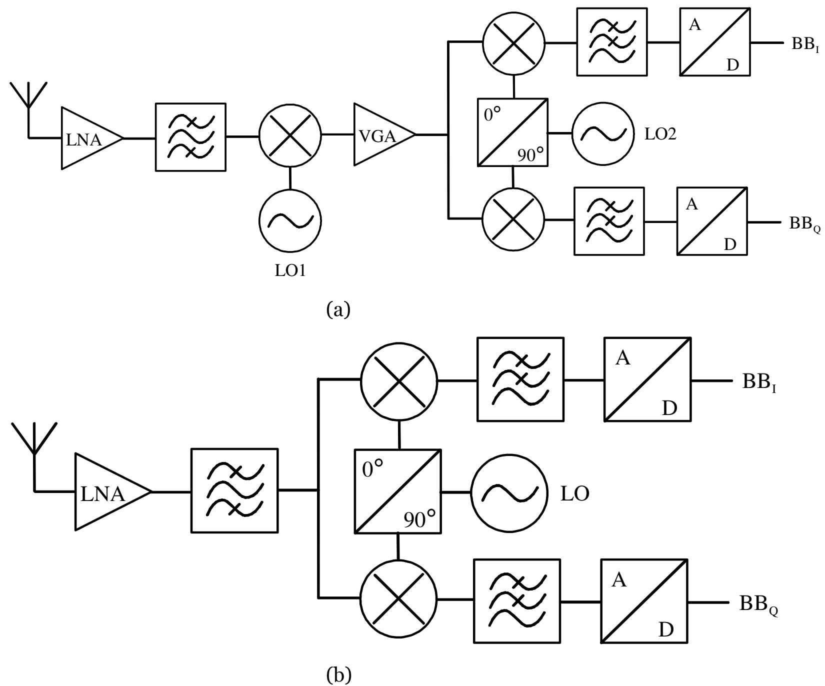



Fig. 31. Block diagrams of a receiver superheterodyne (a) and direct conversion (b) front-ends.

## 4.1 Receiver front-end performance measures

The direct conversion architecture has certain benefits compared to the superheterodyne front-end. These include a single local oscillator, no IF

blocks, and DSB reception when both sidebands are in use. However, typically a direct conversion receiver requires an I/Q division for the local oscillator signal. This is particularly challenging at millimeter-wave frequencies [42]. Thus, it may be more practical to resort to a superheterodyne architecture with one intermediate frequency.

At millimeter-wave frequencies, there are difficulties in obtaining a low noise figure. This is further complicated by a mixer, in which additional noise originates from the image frequency; this can increase the overall noise figure and degrade the sensitivity in the case of the superheterodyne receiver. Even a reasonable level of image rejection can be difficult to achieve with on-chip millimeter-wave filters, since the integrated low quality passive components lead to poor performance. Thus, an image rejecting mixer may provide a solution to the image problem.

The analysis of receiver noise figures is well known [43]. An example of how LNA gain affects the system noise figure is presented in figure 32. The low gain from a single amplifier stage can easily lead to complex optimization problem. Figure 32 shows that a gain of 20 dB or more is required to make the contribution of the following receiver blocks insignificant in practice.

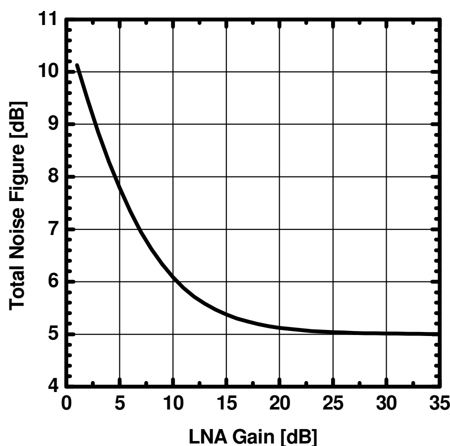



Fig. 32. The total noise figure as a function of the LNA gain. Here, it is assumed that the mixer following the LNA has a 10-dB conversion loss (and a 10-dB noise figure) and that the LNA noise figure is 5 dB.

## 4.2 Low-noise amplifier circuit design

When considering a suitable transistor for LNA design, the unit gate finger size is selected to maximize the gain ($f_{max}$, MSG) and minimize the noise figure [2]. $NF_{min}$ and MSG do not directly depend on the number of

transistor fingers and the number of transistors [44][45]. The drain current density for obtaining the optimum $NF_{min}$ or $f_{max}$ [46] and related MAG [2] is the same irrespective of the technology node if constant field scaling is assumed. The total number of gate fingers and transistors in parallel are chosen so that the linearity requirements are fulfilled; additionally, they can be chosen if low $R_n$ is required for insensitivity to source impedances and wideband noise matching are of importance. $R_n$ and the $|\Gamma|_{opt}$ are inversely proportional to the total gate width [44], which means that there will be a trade-off between noise insensitivity to source impedances (low $R_n$), wideband noise matching (low $|\Gamma|_{opt}$) and dc power consumption, while assuming a fixed unit finger width and a constant current density [47].

Because the lossless feedback network does not affect the minimum noise measure, power match and stability can typically be achieved by using inductive series feedback [48][49][50]. Of course, there should not be too much feedback, such that the system noise figure and the sensitivity would be affected or the number of stages required would be unpractical in terms of the circuit area and dc power consumption. Finally, the transistor is matched to the optimum noise measure $M_{opt}$ and the output is matched to the corresponding conjugate impedance [51][52]. A suitable number of stages can then be cascaded to obtain the specified total required LNA gain.

The feedback amplifiers and the inductive series feedback realized with a transmission line have been presented elsewhere ([53] and [54], respectively). Stability considerations are important when choosing the amount of feedback needed and the stability can be analyzed by using the stability factor and s-probe methods [55][56].

By using the methods described above, the transistor performance as a function of feedback is plotted in this work. The effect of the feedback line length is simulated from a structure that is presented in figure 33.

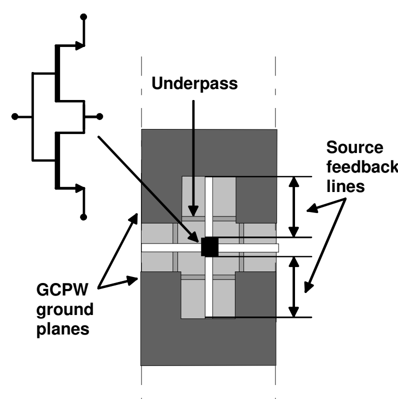



Fig. 33. The simulated transistor structure with transmission line feedback. Both lines have the same length. (© 2014 IEEE, with permission from [Publication XI]).

The results from simulations are shown in figures 34 and 35. The noise and gain performance of the transistor are in best balance for the 10 µm unit finger width MHEMT and source feedback line lengths varying from 7 to 27 µm at 183 GHz [Publication XI].

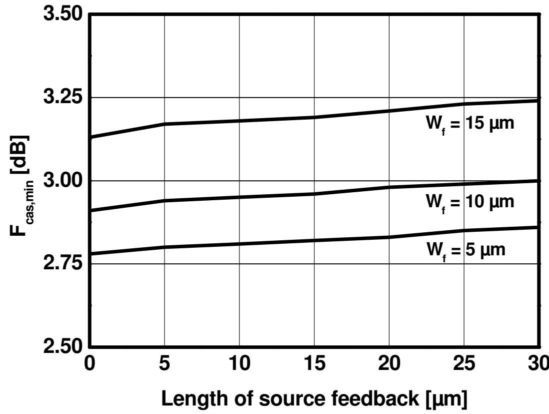



Fig. 34. The simulated $F_{cas,min}$ of three different size two finger MHEMTs at 183 GHz and a drain current density of 400 mA/mm. (© 2014 IEEE, with permission from [Publication XI]).

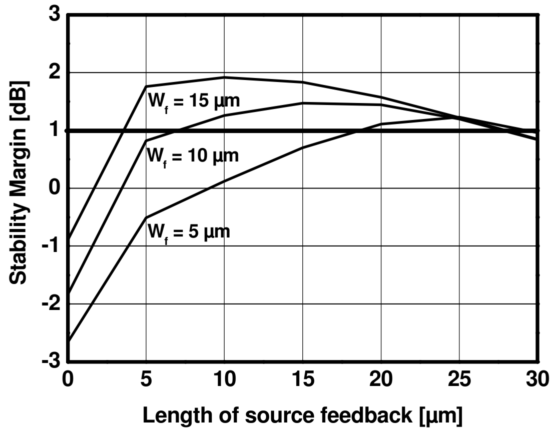



Fig. 35. The simulated stability margin of three different size two finger MHEMTs at 183 GHz and a drain current density of 400 mA/mm. The margin is calculated as a difference between the gain of a transistor matched to the optimum noise measure and maximum stable gain (MSG). (© 2014 IEEE, with permission from [Publication XI]).

The input matching consists of several parts as shown in figure 36 and the corresponding reflection coefficients are shown in figure 37. A wide center conductor GCPW with a characteristic impedance of 30 ohms helps to bring the impedance closer to the optimum and it has lower loss compared to the other 50- and 70-ohm lines available in the design kit. The capacitors C1 and C2 have a small capacitance in order to provide a good short at the

center frequency, while the C3 capacitor is used for stabilizing the amplifier and decoupling the DC bias network from the rest of the amplifier [Publication XI].

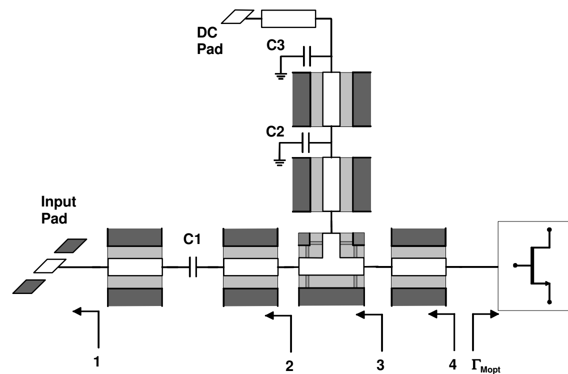



Fig. 36. Low-noise amplifier input matching. (© 2014 IEEE, with permission from [Publication XI]).

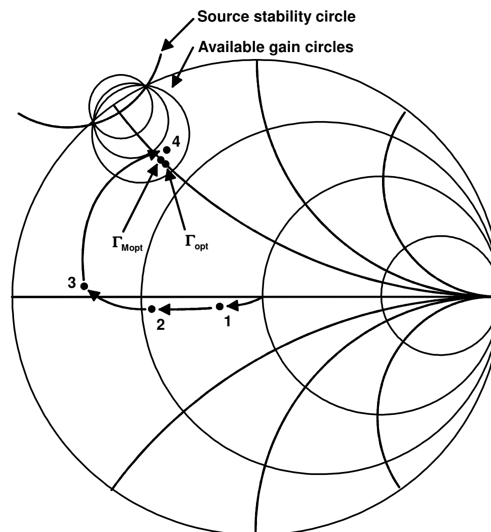



Fig. 37. Low-noise amplifier input matching showing the impedances at different points of the network. $\Gamma_{opt}$ shows the reflection coefficient for the minimum noise figure, while $\Gamma_{Mopt}$ shows the corresponding reflection coefficient for the minimum noise measure. (© 2014 IEEE, with permission from [Publication XI]).

## 4.3 Mixer circuit design

A mixer circuit is needed to convert information from one frequency to another. An active mixer may provide gain while a passive mixer has loss, which must to be compensated for with amplifiers to achieve the required gain. The basic mixing principle is presented in figure 38.

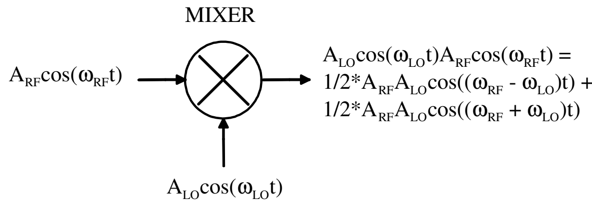



Fig. 38. The mixing principle.

An image rejecting mixer can be used for image suppression [57]. A basic image rejection mixer is shown in figure 39.

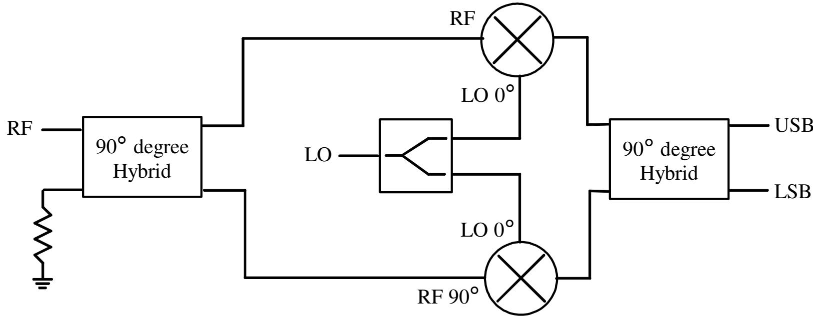



Fig. 39. An image rejecting mixer.

The image rejection can then be calculated as follows:

$$IRR = \frac{1 + \Delta A^2 - 2\Delta A\cos(\theta)}{1 + \Delta A^2 + 2\Delta A\cos(\theta)}, \qquad (15)$$

where $\Delta A$ is the amplitude difference and $\theta$ is the phase difference of the signals [58]. The LO-to-RF leakage can be reduced by using a balanced topology. If both the balanced LO input and image rejection are needed, then another mixer topology (fig. 40.) can be used. A similar configuration has been presented in a previous study [59] except that the LO balancing is different. Four unit mixers are needed: One pair of unit mixer provides the balancing and the other pair produces the image rejection. The IF output has four branches and the signal has four different phases. The 5.3-GHz IF signal combination can be performed with an external circuitry consisting of 180- and 90-degree hybrids. The image rejection depends mostly on the external connections and hybrids having narrow operating bandwidth because of the fact that the errors caused by the on-chip components to should be small and the relative bandwidth of the wanted signal is narrow. The effect of the hybrid network is presented in detail in chapter 5.

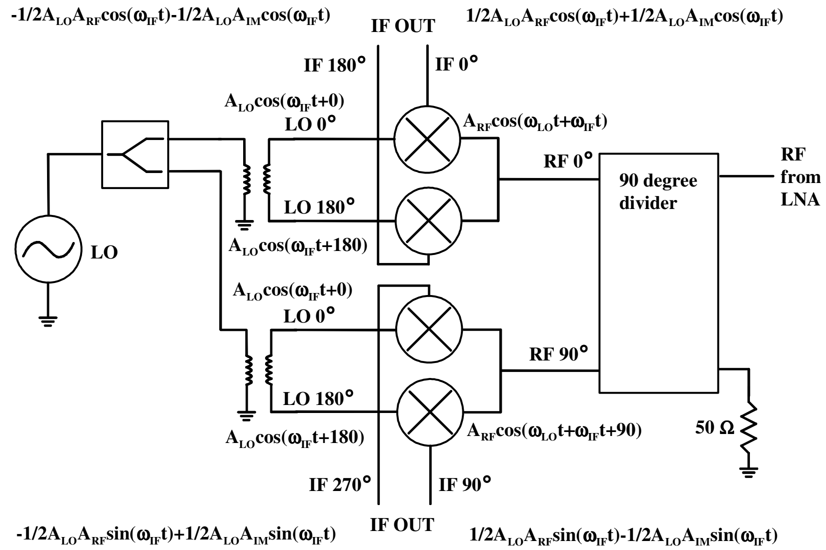



Fig. 40. Balanced image rejection mixer and signals in different branches.

### 4.3.1 Active and passive mixers

One commonly used type of an active mixer is the Gilbert cell mixer and its variants [60][61]. The performance of the Gilbert mixer can be improved by providing a boost current to the transconductance stage. The current is fed through a short-circuited stub, which can be used to tune out the parasitic capacitance of the transistors [62]. The Gilbert cell mixer has drawbacks though, such as the non-grounded transistor bulk connection and voltage headroom. These issues can lead to increased threshold voltage and linearity problems. Typically the dynamic range of an active mixer is smaller than that of a passive mixer. As an example, there were two early attempts to realize active Gilbert type mixers operating at approximately 50–60 GHz both in GaAs PHEMT and CMOS technology [63][64].

Passive mixers can be created with diodes or resistive FETs as mixing components. A resistive FET mixer uses the characteristics related to the resistive channel of a transistor for frequency conversion. A resistive FET mixer can be realized by applying the LO to the gate, the RF to the drain and filtering the IF from the drain. Because there is no dc voltage at the drain, this type of a mixer is called a resistive mixer. The transistor gate is biased with a proper dc voltage. Usually a voltage near the threshold of the transistor is suitable for the gate bias. This type of a mixer has various advantages: Distortion is quite low due to the linear channel of the resistive FET, there is no shot noise and the 1/f-noise level is low [65][66].

In this study, a passive FET mixer is used in the case of the 0.15-μm GaAs PHEMT receiver front-end, while the 65-nm CMOS receiver front-end has an active mixer [Publication VII][Publication XII][Publication XIII].

# 5. Measurement techniques

Most of the scattering parameter measurements were carried out using a HP8510C vector network analyzer with extension modules for the W-band. The measurements in the range of 140-200 GHz were measured using a HP8510B network analyzer with extension modules for the G-band (140-220 GHz). Picoprobe model 220 probes in a GSG configuration with a pitch of 75-µm were used for the RF input and output pads. These measurements were carried out at the MilliLab using a Cascade model 42 probe station. Sometimes, an external attenuator was needed to reduce the input power of the analyzer and to ensure the linear operation of the amplifiers. Unfortunately, this leads to a higher measurement uncertainty for the input port return loss.

The noise figure and insertion gain in the range of 141-212 GHz were measured using a noise figure analyzer and a noise diode. The V-band and W-band noise parameter measurement systems have been described elsewhere ([36] and [67], respectively). An analysis of the uncertainty of the noise measurement system shows a 0.37-dB variation for the minimum noise figure of a test transistor at the V-band, when using a 95 % confidence level [68].

In this work the noise figure of the CMOS radio front-end was measured in two separate ways. The first measurement was done at MilliLab using a noise figure analyzer and it produced the values for the double sideband noise figure. The second measurement was done by the author using a spectrum analyzer and by integrating the noise power level over the IF bandwidth. This requires information on the gain of the front-end. By using the gain values for the selected sideband, the corresponding single sideband noise figure can be calculated as follows:

$$F = \frac{S_{IN}/N_{IN}}{S_{OUT}/N_{OUT}} = \frac{N_{OUT}}{GkTB}, \tag{16}$$

where $S_{IN}$ and $S_{OUT}$ are the input and output signals, $N_{IN}$ and $N_{OUT}$ are the corresponding noise powers, G is power gain, T is the temperature of the input termination and B is bandwidth. The noise measurement setup is presented in figure 41. The obtained noise figure is the total value while the effect of the IF hybrid has to be subtracted to calculate the noise figure of the front-end, as in equation 17.

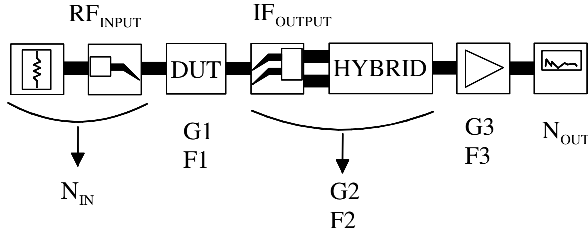



Fig. 41. The receiver front-end measurement setup.

$$F_1 = \frac{N_{OUT}}{G_1 G_2 G_3 kTB} - \frac{F_2 - 1}{G_1} - \frac{F_3 - 1}{G_1 G_2}, \quad (17)$$

where $G_X$, $F_X$, $N_{OUT}$ and $N_{IN}$ = kTB refer to the measurement setup in figure 41.

In the case of the passive mixer and GaAs front-end, the designed IF hybrids significantly affect the image rejection ratio [Publication VII][Publication XII]. The IF hybrids have been designed for a frequency of 5.3 GHz and they only have a narrow bandwidth where they operate accurately. The configuration of the hybrids in presented in figure 42.

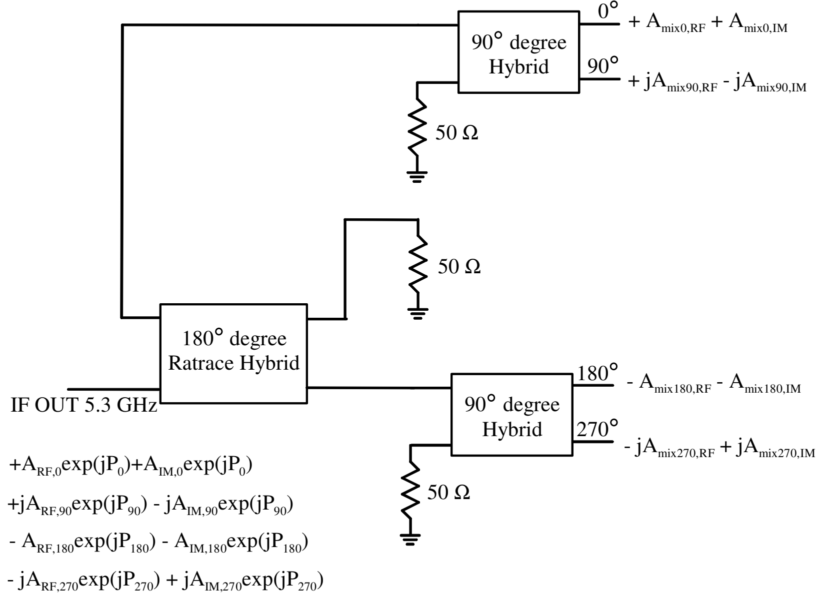



Fig. 42. The hybrid configuration for combining the four phase IF signal.

The effect of the hybrid network on image rejection can be calculated as follows:

$$IRR = \frac{P_{IM}}{P_{RF}} = \frac{\left(\left|IF_{OUT,IM,TOTAL}\right|/\sqrt{2}\right)^2/Z_0}{\left(\left|IF_{OUT,RF,TOTAL}\right|/\sqrt{2}\right)^2/Z_0} = \frac{\left|IF_{OUT,IM,TOTAL}\right|^2}{\left|IF_{OUT,RF,TOTAL}\right|^2}; \tag{18}$$

then, the image and RF signals can be calculated as

$|IF_{OUT,IM,TOTAL}|^2 =$

$$(A_0\cos(P_0) + A_{90}\sin(P_{90}) - A_{180}\cos(P_{180}) - A_{270}\sin(P_{270}))^2 +$$
$$(A_0\sin(P_0) - A_{90}\cos(P_{90}) - A_{180}\sin(P_{180}) + A_{270}\cos(P_{270}))^2, \tag{19}$$

and

$|IF_{OUT,RF,TOTAL}|^2 =$

$$(A_0\cos(P_0) - A_{90}\sin(P_{90}) - A_{180}\cos(P_{180}) + A_{270}\sin(P_{270}))^2 +$$
$$(A_0\sin(P_0) + A_{90}\cos(P_{90}) - A_{180}\sin(P_{180}) - A_{270}\cos(P_{270}))^2, \tag{20}$$

where $A_x$ is the amplitude and $P_x$ is the phase of the corresponding branch of the hybrid network. The final IRR is then

$$IRR_{dB} = 10 \cdot \log_{10}\left(\frac{\left|IF_{OUT,IM,TOTAL}\right|^2}{\left|IF_{OUT,RF,TOTAL}\right|^2}\right). \quad (21)$$

Finally, the calculated image rejection ratio can be plotted as in figure 43.

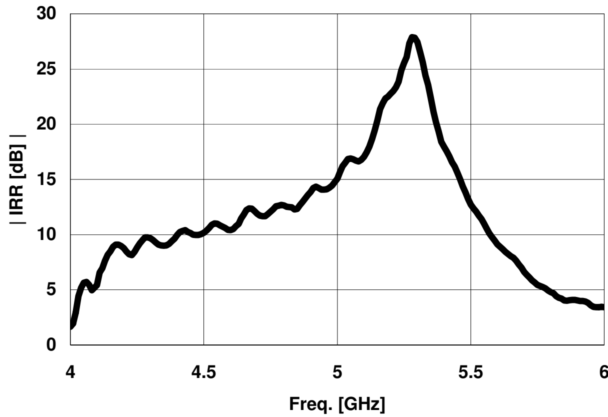



Fig. 43. The calculated image rejection ratio.

A suitable signal source was needed for the downconversion measurements. Typically, a frequency multiplier is used and the power level can be adjusted with an attenuator. However, the multiplier and attenuator system has a significant frequency response that needs to be characterized accurately. The measured input power is shown in figure 44.

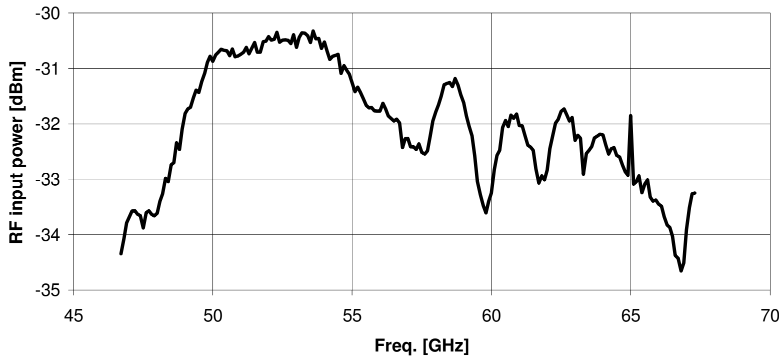



Fig. 44. The measured input power from a frequency quadrubler and an attenuator connected together. The range of the measurement is from 46.7 to 67.3 GHz.

The spectrum measurements at around the V-band require a harmonic mixer to convert the signal into a suitable IF frequency for the analyzer. The harmonic mixer has a significant loss that needs to be characterized over the desired frequency range. The measured result from the harmonic mixer measurement is presented in figure 45.

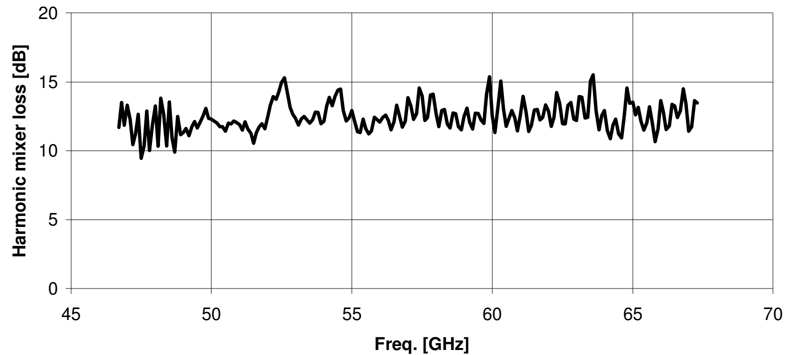



Fig. 45. The measured loss of the harmonic mixer from 46.7 to 67.3 GHz.

The probes have to be characterized as well at the selected frequency range. The results from two back-to-back probe measurements are presented in figure 46.

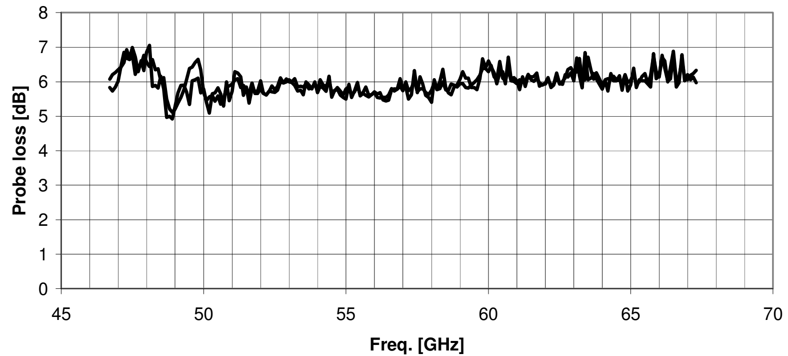



Fig. 46. Two separate back-to-back probe loss measurements. The two measurements were performed to check the consistency of the probe contact.

# 6. Integrated millimeter-wave amplifiers

This chapter describes experimental results from several integrated millimeter-wave amplifiers designed in this work. The operating frequencies vary from 94 to 183 GHz and the circuits have been realized both in 100-nm and 50-nm technologies. The circuits are aimed at a cloud profiling radar application, in which sensitivity is a major performance limiting factor. All circuit models for the active and passive components were provided by the Fraunhofer IAF. The circuit topology is based on grounded coplanar waveguides.

## 6.1 94-GHz amplifier

A 94 GHz amplifier was designed in 100-nm GaAs metamorphic HEMT technology from Fraunhofer IAF [Publication VIII][Publication IX]. A simplified schematic of the amplifier is presented in figure 47. The design is based on grounded coplanar transmission lines. The source feedback was primarily used for transistor stabilization. This four-stage design achieved an 18-dB gain and a 3.1-dB noise figure at 94 GHz. The micrograph and measured results are presented in figures 48, 49, and 50. The measured values were in good agreement with the simulated s-parameters. The $S_{22}$ experienced the largest difference and the gain shifted slightly downward in frequency. The simulated noise figure was quite close to the measured value up to 100 GHz.

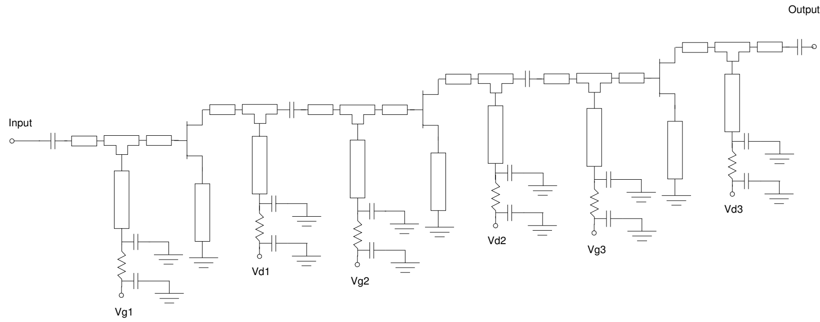



Fig. 47. A simplified schematic of the low-noise amplifier. (© 2007 EuMA, with permission from [Publication IX]).

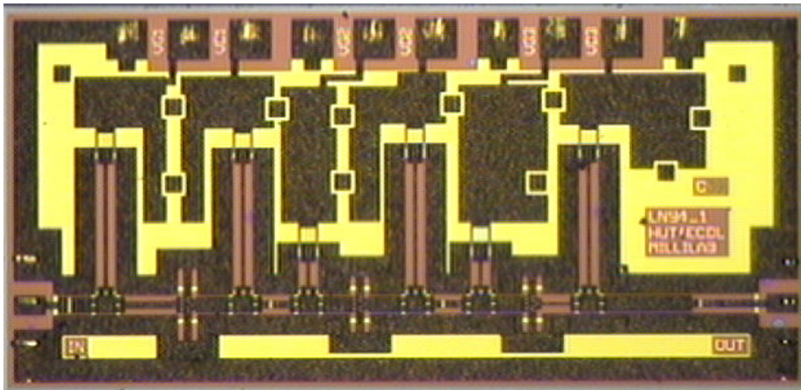



Fig. 48. A micrograph of the 94-GHz amplifier. The chip size is 2.0 x 1.5 mm². (© 2006 EuMA, with permission from [Publication VIII]).

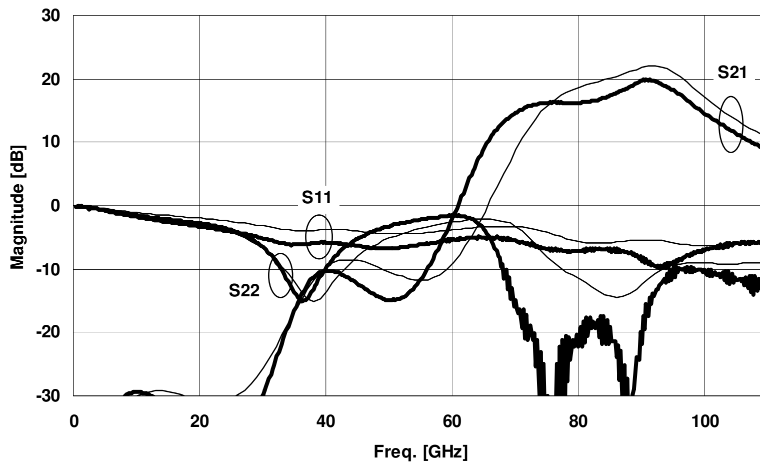



Fig. 49. The measured and simulated s-parameters of the 94-GHz amplifier.

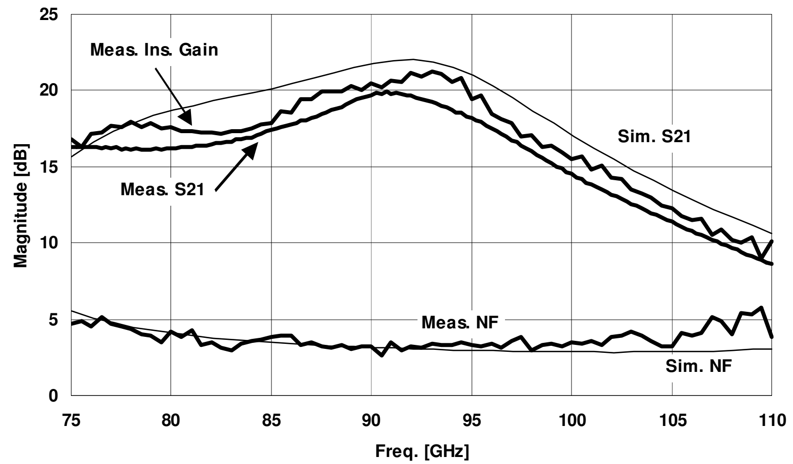



Fig. 50. The measured and simulated noise figure of the 94-GHz amplifier. The measured insertion gain is also plotted.

The 94-GHz amplifier was assembled in a split block package and the measured results are presented in figures 51 and 52. The packaged chip has almost the same $S_{21}$ results as it had on-wafer, but the $S_{11}$ and $S_{22}$ showed more variations. The insertion gain showed more differences, as was to be expected. This was caused by the relatively poor input matching and the source impedance of the noise source. The on-wafer result is compared to other published results in table 3.

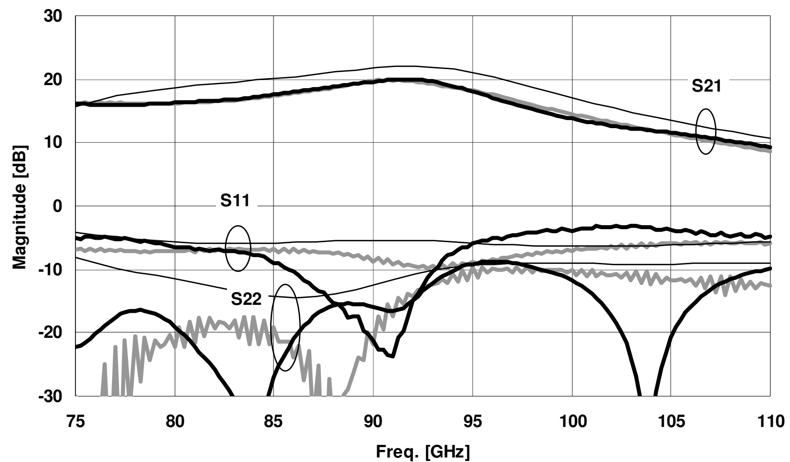



Fig. 51. Measured s-parameters of the packaged 94-GHz amplifier. The on-wafer results are drawn with thick gray lines and while the simulated values are drawn with thin lines.

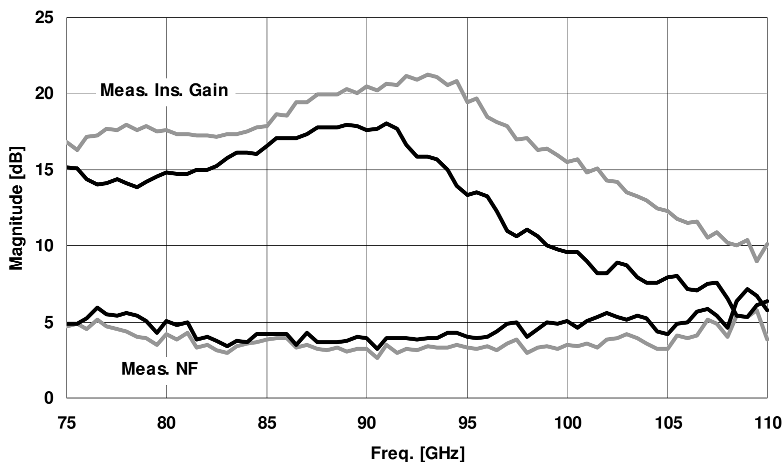



Fig. 52. Measured noise figure of the packaged 94-GHz amplifier. The on-wafer results are drawn with thick gray lines.

Table 3. A comparison of some published amplifiers at 94 GHz.

| Freq. [GHz] | Stages | Gain [dB] | NF [dB] | Topology | Technology | Chip size [mm²] | Ref. |
|---|---|---|---|---|---|---|---|
| 94 | 2 | 16.2 | 10.6 | Cascode | 0.25 µm SiGe | 0.28 | [69] |
| 85-99 | 3 | 33 | 3.2-3.5 | Cascode | 0.13 µm InP HEMT | 2.75 | [70] |
| 94 | 1 | 12 | 2.3 | Cascode | 0.07 µm GaAs MHEMT | 1.00 | [71] |
| 94 | 5 | 6.4 | - | Distributed | 0.1 µm InP HEMT | 0.34 | [72] |
| 94 | 2 | 11 | 4.7 | - | 0.1 µm GaAs PHEMT | 2.64 | [73] |
| 80-100 | 4 | 27 | 5 | CS | 0.1 µm InP HEMT | 4.20 | [74] |
| 77-101 | 4 | 45 | 6-8.3 | Cascode | 0.13 µm SiGe | 0.77 | [75] |
| 82-101 | 2 | 10.8 | - | CS | 0.1 µm GaAs MHEMT | 4.08 | [76] |
| 94.7 | 1 | 9 | 8.6 | Cascode | 0.13 µm SiGe:C | 0.28 | [77] |
| 78-102 | 3 | 13 (s) | < 4.5 (s) | Distributed | 0.1 µm GaAs MHEMT | 3.64 | [78] |
| 90 | 5 | 17 | 9 | CE | 0.18 µm SiGe | - | [79] |
| 94 | 2 | 10.5 | 7.7 | CE | 0.13 µm SiGe:C | - | [80] |
| 70-86 | 3 | 26-30 | < 3.1 | CS, WR-12 | 35 nm InP HEMT | 1.68 | [81] |
| 75-110 | - | 20 | 3.2 | WR-10 | 0.1 µm GaAs MHEMT | - | [82] |
| 94 | 2 | 16.2 | 10.6 | Cascode | 0.25 µm SiGe | 0.28 | [83] |

| 90 | 2 | 22 | 7 | Dif. Cascode | 0.13 µm SiGe | - | [84] |
|---|---|---|---|---|---|---|---|
| 86-96 | 3 | 17.5-19.8 | 1.9-2.7 | CS | 0.1 µm InP HEMT | - | [85] |
| 90-110 | 7 | 35 | 4-4.5 | CS | 0.13 µm InP HEMT | 3.00 | [86] |
| 94 | 5 | 20.5 | 3.9 | - | 0.2 µm ABCS HEMT | 1.20 | [87] |
| 94 | 3 | 11.1 | 5.4 | - | 0.1 µm ABCS HEMT | 1.36 | [88] |
| 70-105 | 2 | 20 | 2.5 | Cascode | 70 nm GaAs MHEMT | 1.13 | [89] |
| 94 | 4 | 16.3 | 5.7 | CS | 0.15 µm GaAs MHEMT | 2.31 | [90] |
| 70-105 | 2 | > 20 | 2.5 | Cascode | 70 nm GaAs MHEMT | - | [91] |
| 80-95 | 1 | 12 | 2.2 | Cascode | 70 nm GaAs MHEMT | 1.00 | [92] |
| 80-100 | 1 | > 12 | 2.3 | Cascode | 70 nm GaAs MHEMT | 1.00 | [93] |
| 80-95 | 1 | > 12 | 2.8 | Cascode | 70 nm GaAs MHEMT | 1.00 | [94] |
| 85-105 | 3 | 18 | 10 | Cascode | 0.15 µm GaAs PHEMT | 3.00 | [95] |
| 94 | 2 | 12.2 | 3.3 | - | 0.1 µm InP HEMT | - | [96] |
| 94 | 3 | 22 | - | - | 0.12 µm InP HEMT | 3.15 | [97] |
| 94 | 2 | 18-20 | 6-7 | Dual gate | 0.15 µm GaAs PHEMT | - | [98] |
| 94 | 3 | 14.7 | 5.5 | CS | 0.12 µm GaAs PHEMT | 2.00 | [99] |
| 94 | 4 | 37 | 6.6 | Dual gate | 0.15 µm GaAs PHEMT | 3.00 | [100] |
| 94 | 4 | > 15 | 6.5 (s) | CS | 0.25 µm InP HEMT | 4.42 | [101] |
| 85-115 | 4 | 20 | 2.7-4.2 | CS | 0.1 µm InP HEMT | 1.46 | [102] |
| 95 | 4 | 20 | 2.5 | - | - | - | [103] |
| 94 | 3 | 18 | 2.9 | - | InP HEMT | - | [104] |
| 94 | 4 | 16 | 3.2 | CS | 0.1 µm InP HEMT | 3.00 | [105] |
| 94 | 2 | 12.2 | 3.3 | - | 0.1 µm InP HEMT | 2.55 | [106] |
| 85 | 3 | 13 | 5.7 | CS | 45 nm CMOS SOI | - | [8] |
| 95 | - | 15 | 2.3 | - | 35 nm InP HEMT | WG housing | [9] |
| 94 | 4 | 18 | 3.1 | CS | 100 nm GaAs MHEMT | 3.00 | [P. VIII] [P. IX] |

## 6.2 155-GHz amplifier

A 155-GHz amplifier was designed in 100-nm GaAs metamorphic HEMT technology from Fraunhofer IAF [111][Publication X]. A simplified schematic of the amplifier is presented in figure 53 and the design method is mostly the same. This four-stage design achieved a 15.6-dB gain and a 7.2-dB noise figure at 155 GHz. The micrograph and measured results are presented in figures 54, 55, and 56. The simulated $S_{11}$ and $S_{21}$ compared

relatively well with the measured values, but the S22 had more discrepancies and it shifted downwards in frequency.

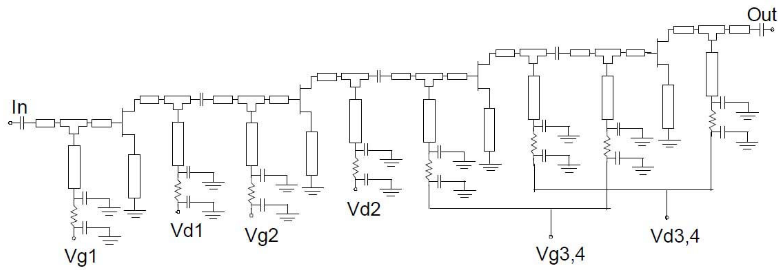



Fig. 53. A simplified schematic of the 155-GHz low-noise amplifier.

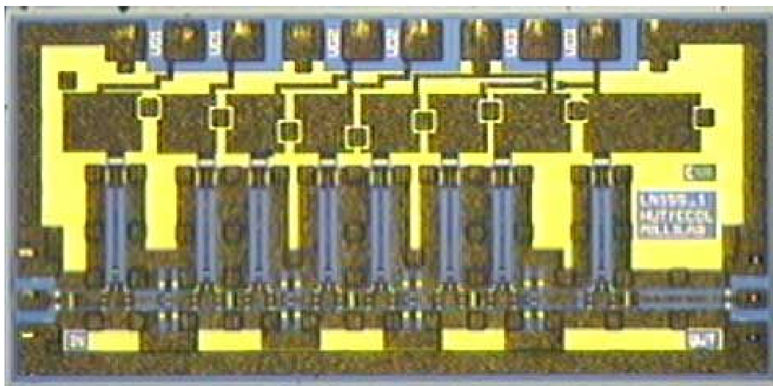


Fig. 54. Micrograph of the 155-GHz amplifier. The chip size is 2.0 x 1.0 mm² [111] [Publication X].

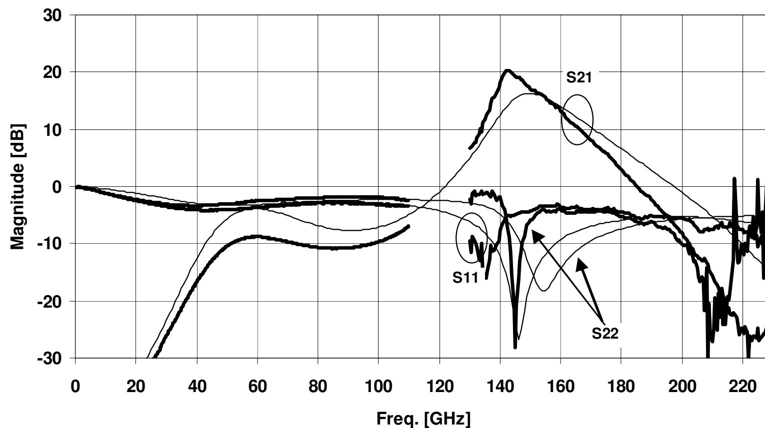



Fig. 55. Measured and simulated s-parameters of the 155-GHz amplifier [111][Publication X]. The thin lines represent simulated values.

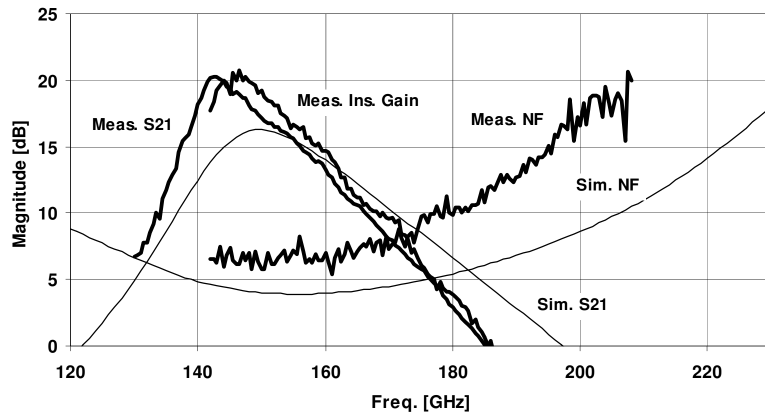



Fig. 56. Measured noise figure of the 155-GHz amplifier [111][Publication X]. The measured insertion gain is also shown.

The 155-GHz amplifier was assembled in a split block package with waveguide interfaces at the input and output. A photograph of the packaged chip is provided in figure 57. The measured s-parameters are compared to the on-wafer results and simulated values in figure 58 and the noise figure is presented in figure 59. The packaged chip had a similar $S_{21}$, but the $S_{11}$ and $S_{22}$ had more variations. Figure 59 shows that the effect of the package on the noise figure was small. The on-wafer result is compared to other published results in table 4.

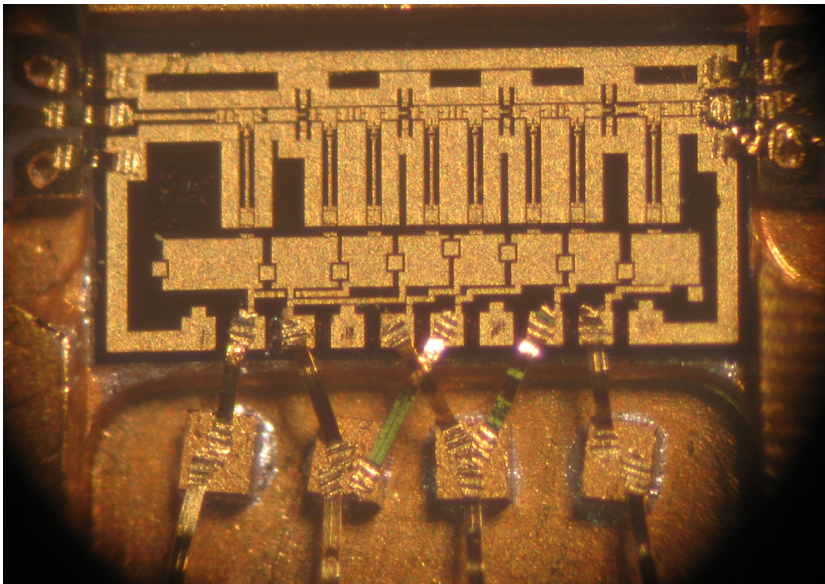


Fig. 57. A photograph of the 155-GHz amplifier assembled in a split block package.

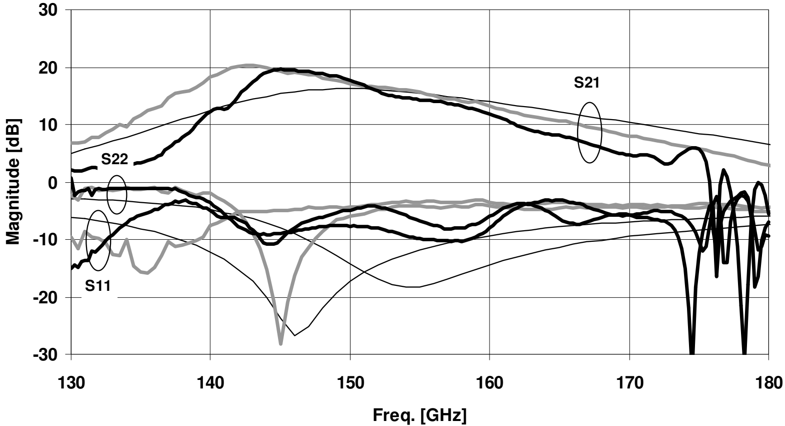



Fig. 58. Measured s-parameters of the packaged 155-GHz amplifier. The on-wafer results are drawn with thick gray lines and the simulated values with thin lines.

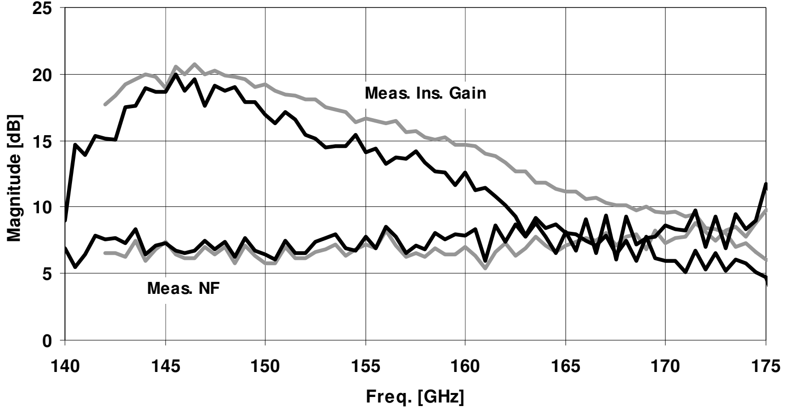



Fig. 59. Measured noise figure of the packaged 155-GHz amplifier. The on-wafer results are drawn with thick gray lines.

Table 4. A comparison of some published amplifiers at approximately 155 GHz.

| Freq. [GHz] | Stages | Gain [dB] | NF [dB] | Topology | Technology | Chip size [mm²] | Ref. |
|---|---|---|---|---|---|---|---|
| 160-220 | 3 | 15-25 | 4.9-5.6 | Cascode, CS,WR5 | 35 nm InP HEMT | - | [107] |
| 160 | 3 | 15 | - | CG | 75 nm InP HEMT | 0.37 | [108] |
| 145 | 3 | 21 | 8.5 | Cascode | 0.13 µm SiGe | 0.36 | [109] |
| 140 | 2 | > 17 | < 9 | Dif. Cascode | 0.13 µm SiGe | 0.33 | [110] |
| 155 | 4 | 21.7-15.9 | 6.7-7.2 | CS | 100 nm GaAs MHEMT | 2.00-2.25 | [111] |
| 155 | 2 | 15 | 4 | Cascode | 100 nm GaAs MHEMT | 2.00 | [112] |
| 155 | 3 | 12.5 | - | - | 100 nm InP HEMT | 4.00 | [113] |
| 155 | 3 | 10.1 | 5.1 | CS | 0.1 µm InP HEMT | 4.00 | [114] |
| 160 | 3 | 27 (s) | 7.4-7.8 (s) | Dif. Cascode | 0.13 µm SiGe | - | [115] |
| 150-160 | - | 16 | 3.1 | - | 35 nm InP HEMT | WG housing | [9] |
| 155 | 4 | 15.6 | 7.2 | CS | 100 nm GaAs MHEMT | 2.00 | [111] [P. X] |

### 6.3 183-GHz amplifiers

A 183-GHz amplifier was designed in 100-nm GaAs metamorphic HEMT technology from Fraunhofer IAF [117]. The simplified schematic is similar to the one in figure 53. This four-stage design achieved a 14.9-dB gain and a 7.5-dB noise figure at 183 GHz. The measured results and a micrograph of the chip are presented in figures 60–62. The gain has shifted downwards in frequency and the noise figure was significantly higher than in the simulations. A second version was designed in 50-nm GaAs metamorphic HEMT technology and it achieved a 16-dB gain and a 7.4-dB noise figure at 183 GHz [Publication XI]. The results and a micrograph of the second version are shown in figures 63–65. The gain response did not shift downwards as much and there were variations in both the $S_{11}$ and $S_{22}$. The noise figure was simulated accurately up to 170 GHz; beyond that frequency, the measured noise figure was higher. The insertion gain was different from the $S_{21}$ at a frequency range of 162 to 175 GHz. The on-wafer results of both amplifiers are compared to other published results in table 5.

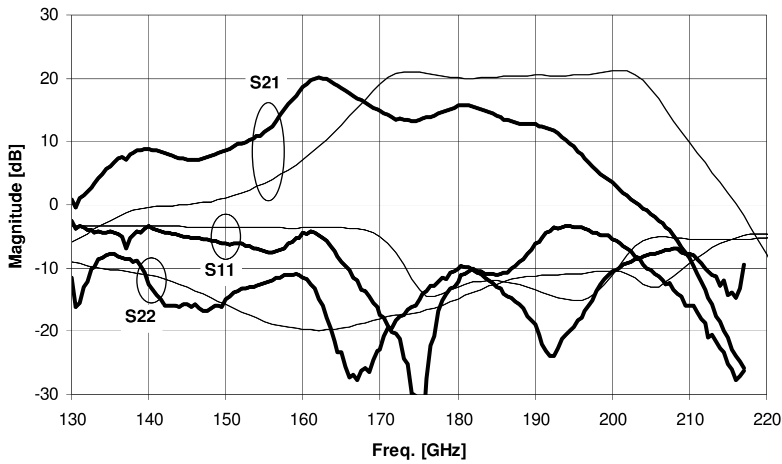



Fig. 60. Measured and simulated gain, input and output return loss and noise figure for the 100-nm GaAs MHEMT 183-GHz amplifier.

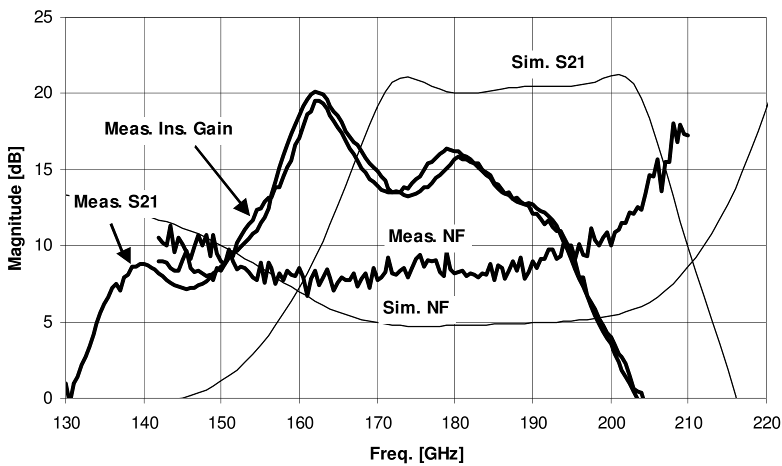



Fig. 61. Measured noise figure and insertion gain of the 100-nm GaAs MHEMT 183-GHz amplifier.

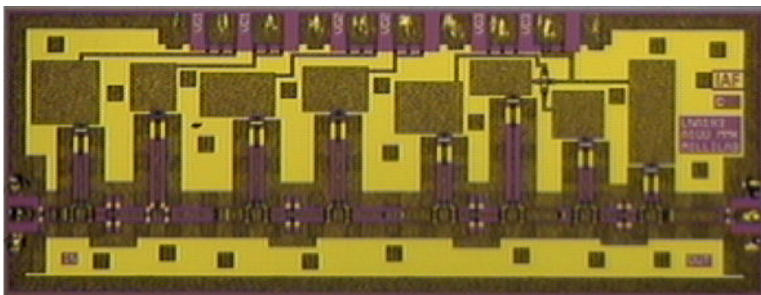


Fig. 62. A micrograph of the 100-nm GaAs MHEMT 183-GHz amplifier. The chip size is 2.5 x 1.0 mm$^2$ [117].

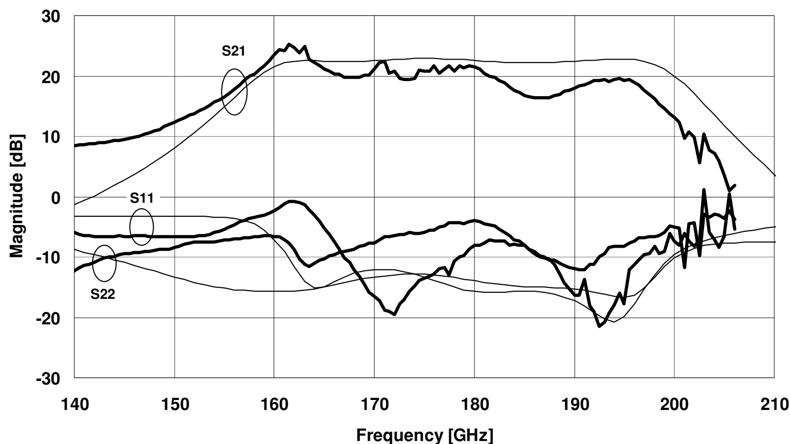



Fig. 63. Measured and simulated gain, input and output return loss and noise figure of the 50-nm GaAs MHEMT 183-GHz amplifier.

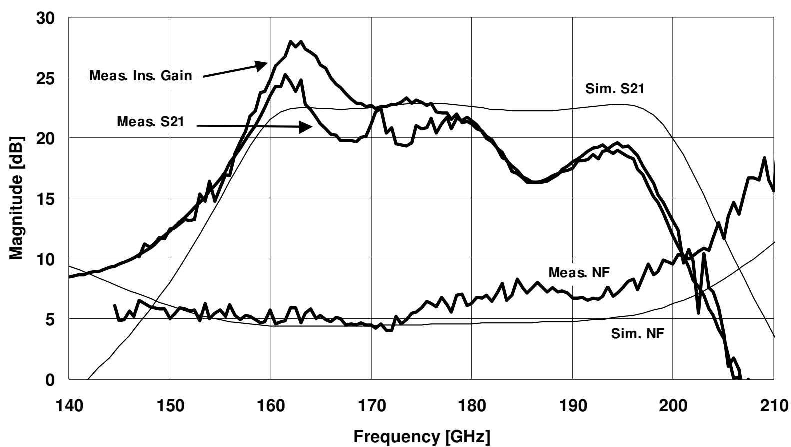



Fig. 64. Measured noise figure and insertion gain of the 50-nm GaAs MHEMT 183-GHz amplifier.

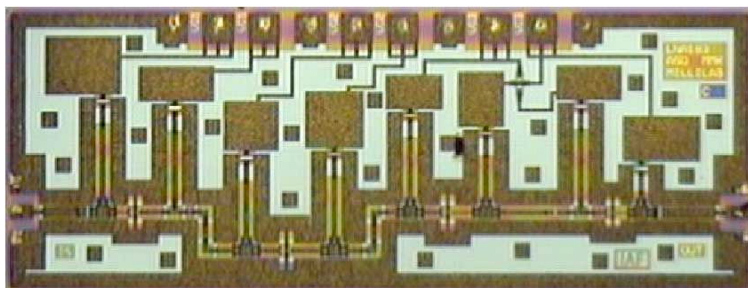



Fig. 65. A micrograph of the 50-nm GaAs MHEMT 183-GHz amplifier. The chip size is 2.5 x 1.0 mm².

Table 5. Some published amplifiers at approximately 180 GHz.

| Freq. [GHz] | Stages | Gain [dB] | NF [dB] | Topology | Technology | Chip size [mm²] | Ref. |
|---|---|---|---|---|---|---|---|
| 194 | 3 | 12 | - | CG | 75 nm InP HEMT | 0.37 | [108] |
| 160-195 | 2 x 4 | 25-40 | - | 2x4-stage bal. | 70 nm InP HEMT | Test fixture | [116] |
| 160-220 | 3 | 15-25 | 4.9-5.6 | Cascode,CS,WR5 | 35 nm InP HEMT | - | [107] |
| 183 | - | 17 | 3.4 | - | 35 nm InP HEMT | WG housing | [9] |
| 183 | 4 | 14.9 | 7.5 | CS | 100 nm GaAs MHEMT | 2.5 | [117] |
| 183 | 4 | 16 | 7.4 | CS | 50 nm GaAs MHEMT | 2.5 | [P. XI] |

# 7. Receiver front-ends for 60-GHz applications

Highly integrated microchips are especially preferred in various consumer applications, because they are suitable for mass production and they are small in size. Even an antenna can be integrated on a chip [118]. The integration of millimeter-wave front-ends will lead to new applications that have not been feasible before, because of the cost and size of the previously available systems. SiGe HBT -based transceiver front-ends have already been developed at an operating frequency of 320 GHz [119]-[121]. Several transmitters and receivers operating above 125 GHz have also been developed in 65-nm CMOS technology [122][123]. Likewise, researchers have studied a number of high-performance 60-GHz CMOS transceivers [124]-[139], as well as packaged transceiver systems [125][126]. A 60-GHz, highly integrated, phased-array system has also been integrated in SiGe technology [127].

## 7.1 Realized receiver front-ends

In this work two different 60-GHz receiver front-ends are presented [Publication XII][Publication XIII]. The author's work is related to the amplifier in case of the GaAs front-end and to the active mixer in the case of the CMOS front-end. The GaAs front-end has a quadrature, balanced IF output and it also allows an IF of 0 Hz, so it is suitable for direct conversion reception with IQ-phase information. The CMOS front-end has a balanced IF output, so it could operate at as low as 0 Hz, but without IQ-separation. Table 6 compares the on-wafer results of these front-ends with some published 60-GHz receiver front-ends. The noise figure of the GaAs front-end compares well with the published results and the CMOS front-end has a relatively small circuit area.

Table 6. A comparison of some recently published 60-GHz receiver front-ends.

| Freq. [GHz] | Gain [dB] | NF [dB] | Blocks | $P_{DC}$ [mW] | Technology | Chip size [mm²] | Ref. |
|---|---|---|---|---|---|---|---|
| 52-66 | 25-28 | 7.1-8.2 | LNA, mixer | 20 | 90 nm CMOS | 0.80 | [128] |
| 57.5-60.8 | 15 * | 9 | LNA, mixer, PLL | 96 | 90 nm CMOS | 0.45 | [129] |
| 58.2-67.8 | 19 | 8.7 | LNA, mixers, buffers | 32.6 | 0.18 µm SiGe | - | [130] |
| 56 | 18.7 | 9 | LNA, mixer, BB amp | 50.2 | 0.13 µm CMOS | 1.20 | [131] |
| 60 | 4 | 15 | LNA, mixer, buffers | 6 | 65 nm CMOS | - | [132] |
| 60 | 30 | 10 | LNA, mixers, BB amp | 44 | 0.13 µm CMOS | 1.32 | [133] |
| 60 | 66 | 4.2 | LNA, mixer, filter, PGA | 75 | 65 nm CMOS | 0.26 | [134] |
| 55-65 | 14.7 | 5.6 | LNA, mixer | 134 | 65 nm CMOS | 0.90 | [135] |
| 49-52 | 24.6-30 | 7.1-9.8 | LNA, mixer, QVCO, LO-buffer | 65 | 90 nm CMOS | 1.40 | [136] |
| 60 | 8-22 | < 6.9 | LNA, PS, Gm | 66 | 120 nm SiGe | 4.62 ** | [137] |
| 60 | 7 | 8.7 | LNA, PS, Combiner | 13 | 90 nm CMOS | 1.60 | [138] |
| 61 | > 10 | < 7.2 | LNA, PS | 78 | 65 nm CMOS | 1.60 | [139] |
| 55-63 | 7.1 | 10.5 | LNA, mixer, IF-hybrid, 8 x multiplier | 990 | 150 nm PHEMT | 28.5 | [140] |
| 60 | 3 | 6.3 | LNA, PS | 18 | 90 nm CMOS | 0.89 | [141] |
| 57-62 | 12-5.5 | 3.7-4.0 ***) | LNA, mixer | 255 | 150 nm PHEMT | 4.50 | [P. XII] |
| 51.5 | 14.5 | 9.2 (DSB) 12.0 (SSB) | LNA, mixer | 174 | 65 nm CMOS | 0.90 | [P. XIII] |

*) voltage gain

**) several receive channels

***) calculated from measured results obtained from individual test blocks

## 7.2 Receiver front-end in 150-nm PHEMT GaAs technology

The designed GaAs front-end consists of a three-stage low-noise amplifier and a resistive FET mixer integrated on a single chip [Publication IV][Publication VII][Publication XII]. A simplified schematic is shown in figure 66 while a micrograph of the front-end is shown in figure 67. The radio front-end exhibited a gain ranging from 5.5 to 12 dB and an image rejection ratio ranging from 10.6 to 18.7 dB for an RF frequency ranging from 57 to 62 GHz. The measured 1-dB input compression point was -21 dBm when using a 61-GHz RF signal. The noise figure was calculated to be approximately 3.7-4.0 dB at 60 GHz according to the measured results

obtained separately from the LNA and mixer blocks [Publication IV][Publication VII].

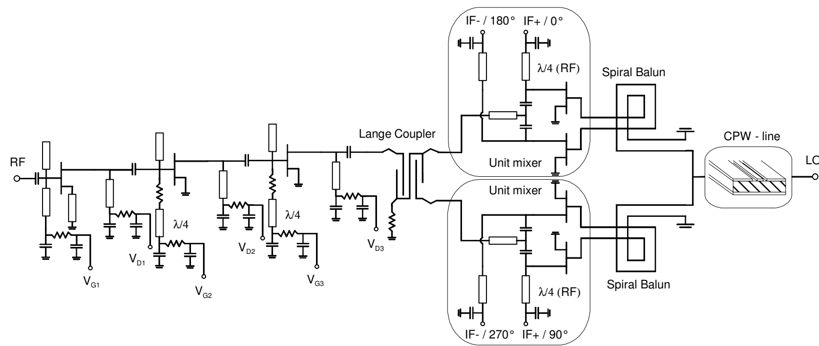



Fig. 66. A simplified schematic of the 60-GHz receiver front-end in 0.15-µm GaAs PHEMT technology. (© 2006 IEEE, with permission from [Publication XII]).

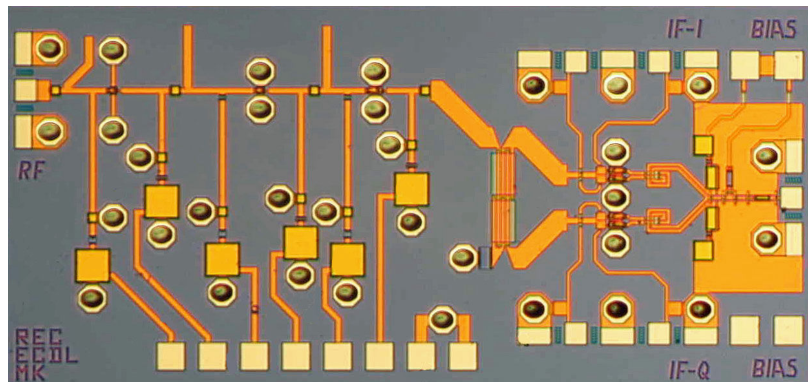



Fig. 67. A micrograph of the 60-GHz receiver front-end chip. This chip was developed in 0.15-µm GaAs PHEMT technology and it consists of a balanced IQ-resistive-FET mixer and a 3-stage low-noise amplifier. The chip size is 3.0 x 1.5 mm². (© 2006 IEEE, with permission from [Publication XII]).

### 7.3 Receiver front-end in 65-nm CMOS technology

The designed CMOS receiver front-end consists of a 5-stage low-noise amplifier and an active mixer that includes buffers at the balanced IF output. A simplified schematic is shown in figure 68 while a micrograph of the front-end is shown in figure 69. For the active mixer, a 4x25 µm transistor was chosen for the transconductance stage since it was characterized earlier. The mixing transistors were 2x25 µm in size and they were biased near the threshold voltage for minimum conversion loss. The measured results show that the receiver obtains a 14.5-dB gain and a 9.2-dB double sideband noise figure with a 53-GHz local oscillator and 1.5-GHz intermediate frequencies. The 1-dB input compression point was at a level of -24.4 dBm.

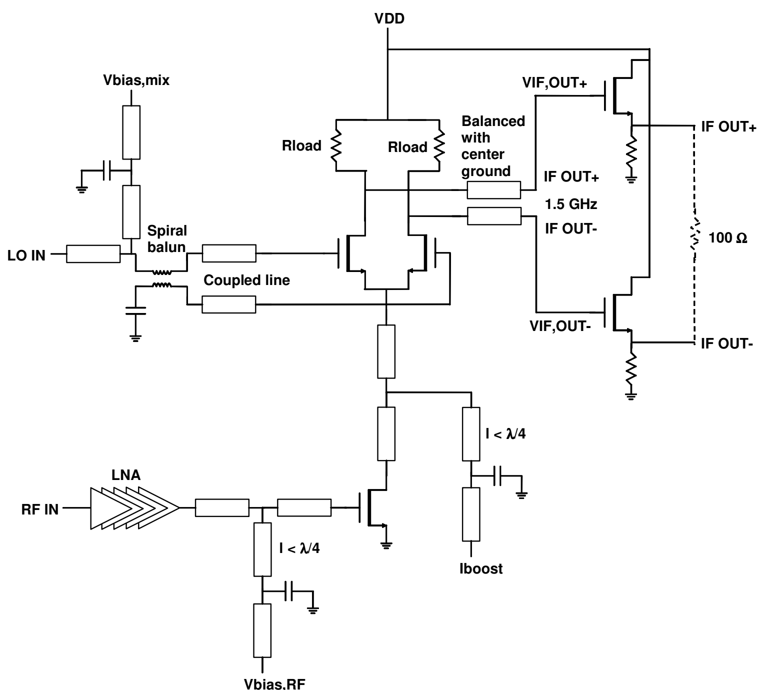



Fig. 68. A simplified schematic of the 60-GHz receiver front-end in 65-nm CMOS.

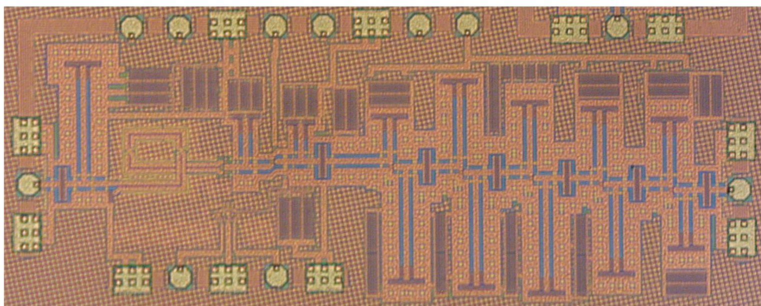


Fig. 69. A micrograph of the 60-GHz receiver front-end chip. The chip was developed in 65-nm CMOS technology and it consists of a balanced active mixer and a 5-stage amplifier. The chip size is 0.90 $mm^2$ including pads. (© 2009 IEEE, with permission from [Publication XIII]).

# 8. Conclusions

Several design issues and techniques for millimeter-wave integrated circuit design were presented in this work. The modeling of transmission lines and transistors was presented in more detail and the usability of such components in millimeter-wave circuit design was evaluated using circuit examples, which consisted of two 60-GHz amplifiers and one 100-GHz CMOS amplifier. The re-simulations using the presented transistor model were the work of the author. The chapter on measurement techniques considered some of the issues that were encountered during the circuit characterization phase.

Circuit realizations are shown for gallium arsenide as well as CMOS technologies. GaAs technologies include both pseudo- and metamorphic HEMTs. The developed CMOS circuit is designed using the 65-nm node. The performance of these circuits and, especially, the GaAs MHEMT amplifiers compares well with the results published by others. In fact, the results show that the metamorphic HEMTs reached performance levels that had previously been almost exclusively achievable by only InP HEMTs. The millimeter-wave amplifiers can help in efforts to improve the performance of millimeter-wave radiometric instruments. Furthermore, experimental results were presented for 60-GHz receiver front-ends developed in both 0.15-µm GaAs PHEMT and 65-nm CMOS technologies.

The 94- and 155-GHz amplifiers were designed in 100-nm GaAs MHEMT technology. The 94-GHz amplifier achieved an 18-dB gain and a 3.1-dB noise figure. The 155-GHz amplifier achieved a 15.6-dB gain and a 7.2-dB noise figure. In addition, the 155-GHz version of the amplifier was assembled in a split block package. Two 183-GHz amplifiers were designed in 100-nm and 50-nm GaAs metamorphic HEMT technology. The 100-nm version achieved a 14.9-dB gain and a 7.5-dB noise figure, while the 50-nm version achieved a 16-dB gain and a 7.4-dB noise figure. The chip sizes of the GaAs amplifiers varied from 2.0 to 3.0 $mm^2$. Furthermore, two 60 GHz receiver radio front-ends were presented. One front-end was developed in 150-nm GaAs PHEMT and the other was developed in 65-nm CMOS technology. The GaAs front-end exhibited a gain ranging from 5.5 to 12 dB

and an image rejection ratio ranging from 10.6 to 18.7 dB for an RF frequency range of 57 to 62 GHz. The measured 1-dB input compression point was -21 dBm when using a 61-GHz RF signal. The noise figure was calculated to be approximately 3.7–4.0 dB at 60 GHz. The measured results for the CMOS front-end show a 14.5-dB gain and a 9.2-dB double sideband noise figure. The 1-dB input compression point was -24.4 dBm. The chip sizes were 4.5 mm$^2$ for the GaAs front-end and 0.90 mm$^2$ for the CMOS version of the front-end.

Future work should focus on reliability issues and evaluate the suitability of CMOS technology for millimeter-wave space applications, by achieving higher frequencies and adapting new technology nodes to millimeter-wave or even submillimeter-wave circuits. The compound technologies are already reaching terahertz frequencies [142] and may continue to become even faster and better in terms of noise characteristics in the near future. However, one should bear in mind that the issue of technology scaling will be facing challenges related to quantum mechanics and the cost and performance of it may not be heading in the same directions in the future as it did in the past [143].

# Bibliography

[1] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," *IEEE Communications Magazine*, vol. 40, no. 1, pp. 140-147, Jan. 2002.

[2] A. M. Niknejad, H. Hashemi, *Mm-Wave Silicon Technology: 60GHz and Beyond*, Springer Science+Business Media Inc. 2008, p. 297.

[3] R. S. Pengelly, J. A. Turner, "Monolithic broadband GaAs f.e.t. amplifiers," *Electronics Letters* , vol. 12, no. 10, pp. 251-252, May 1976.

[4] A. Cathelin, B. Martineau, N. Seller,S. Douyere, J. Gorisse, D. Pruvost, C. Raynaud, F. Gianesello,S. Montusclat, S. P. Voinigescu, A. M. Niknejad, D. Belot,J.-P. Schoellkopf, "Design for millimeter-wave applications in silicon technologies," in *33rd European Solid State Circuits Conference Proceedings*, Munich, Germany, Sept. 2007, pp. 464-471.

[5] M. Tiebout, H.-D. Wohlmuth, W. Simburger, "A 1V 51GHz fully-integrated VCO in 0.12/spl mu/m CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2002, pp. 238-239.

[6] C. H. Doan, S. Emami, A. M. Niknejad, R. W. Brodersen, "Design of CMOS for 60GHz applications," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2004, pp. 440-441.

[7] B. Heydari, M. Bohsali, E. Adabi, A. M. Niknejad, "Low-Power mm-Wave Components up to 104GHz in 90nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2007, pp. 200-201.

[8] O. Inac, M. Uzunkol, G. M. Rebeiz, "45-nm CMOS SOI Technology Characterization for Millimeter-Wave Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1301-1311, Jun. 2014.

[9] P. Kangaslahti, L. Boon, T. Gaier, A. Tanner, M. Varonen, L. Samoska, S. Brown, B. Lambrigtsen, S. Reising, J. Tanabe, O. Montes, D. Dawson, C. Parashare, "Low noise amplifier receivers for millimeter wave atmospheric remote sensing," in *IEEE MTT-S International Microwave Symposium Digest*, Montreal, Canada, Jun. 2012, pp. 1-3.

[10] M. A. Janssen, *Atmospheric remote sensing by microwave radiometry*, John Wiley & Sons, New York, 1993, p. 572.

[11] C. H. Doan, S. Emami, A. M. Niknejad, R. W. Brodersen, "Millimeter-wave CMOS device modeling and simulation," in *Proceedings of the International Symposium on Circuits and Systems*, Vancouver, Canada, May 2004, pp. 524-527.

[12] S. Seki, H. Hasegawa, "Cross-tie slow-wave coplanar waveguide on semi-insulating GaAs substrates," *Electronics Letters* , vol. 17, no. 25, pp. 940-941, Dec. 1981.

[13] T. S. D. Cheung, J. Long, "Shielded passive devices for silicon based monolithic microwave and millimeter-wave integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, May 2006.

[14] A. Sayag, D. Ritter, D. Goren, "Compact Modeling and Comparative Analysis of Silicon-Chip Slow-Wave Transmission Lines With Slotted Bottom Metal Ground Planes," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 4, pp. 840-847, Apr. 2009.

[15] R. R. Lahiji, L. P. B. Katehi, S. Mohammadi, “A distributed analogue CMOS phase shifter with shielded transmission line“, in *Proc. of 38th European Microwave Conference*, Amsterdam, the Netherlands, Oct. 2008, pp. 817–820.

[16] W. R. Eisenstadt, Y. Eo, “S-parameter-based IC interconnect transmission line characterization”, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15 , no. 4, pp. 483–490, Aug. 1992.

[17] K. H. K. Yau, K. K. W. Tang, P. Schvan, P. Chevalier, B. Sautreuil, S. P. Voinigescu, "The Invariance of the Noise Impedance in n-MOSFETs across Technology Nodes and its Application to the Algorithmic Design of Tuned Low Noise Amplifiers," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems Technical Digest*, Long Beach, CA, Jan. 2007, pp. 245-248.

[18] Y. Terry, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, Y. Ming-Ta, P. Schvan, S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1044-1057, May 2007.

[19] H. Hashemi, A. Hajimiri, "Concurrent dual-band CMOS low noise amplifiers and receiver architectures," in *Symposium on VLSI Circuits Digest of Technical Papers*, Kyoto, Japan, Jun. 2001, pp. 247-250.

[20] H. Hashemi, A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 288-301, Jan 2002.

[21] Y. H. Wu, A. Chin, C. S. Liang, C. C. Wu, "The performance limiting factors as RF MOSFETs scale down," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Boston, MA, Jun. 2000, pp. 151-155.

[22] G. Jung-Suk, A. Hee-Tae, D. J. Ladwig, Y. Zhiping, T. H. Lee, R. W. Dutton, "A noise optimization technique for integrated low-noise amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 994-1002, Aug 2002.

[23] M. C. A. M. Koolen, J. A. M. Geelen, M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. of the Bipolar Circuits and Technology Meeting*, Minneapolis, MN, Sept. 1991, pp. 188-191.

[24] N. Waldhoff, C. Andrei, D. Gloria, S. Lepilliet, F. Danneville, G. Dambrine, "Improved Characterization Methology for MOSFETs up to 220 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1237-1243, May 2009.

[25] J.-P. Raskin, G. Dambrine, R. Gillon, "Direct extraction of the series equivalent circuit parameters for the small-signal model of SOI MOSFETs," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 12, pp. 408-410, Dec. 1997.

[26] L. Seonghearn, Y. Hyun Kyu, C.-S. Kim, J.-G. Koo, K.-S. Nam, "A novel approach to extracting small-signal model parameters of silicon MOSFET's," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 3, pp.75-77, Mar. 1997.

[27] A. Issaoun, X. Yong Zhong, S. Jinglin, J. Brinkhoff, F. Lin, "On the Deembedding Issue of CMOS Multigigahertz Measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 9, pp. 1813-1823, Sept. 2007.

[28] G. Dambrine, A. Cappy, F. Heliodore, E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151-1159, Jul 1988.

[29] P. C. Walters, R. D. Pollard, J. R. Richardson, G. Gatti, "Millimetre-wave device modelling differences in microstrip and coplanar waveguide," in *IEEE MTT-S International Microwave Symposium Digest*, Atlanta, GA, Jun. 1993, pp. 1173-1176.

[30] M. Berroth, R. Bosch, "High-frequency equivalent circuit of GaAs FETs for large-signal applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 2, pp. 224-229, Feb 1991.

[31] L. Seonghearn C.-S. Kim, Y. Hyun Kyu, "A small-signal RF model and its parameter extraction for substrate effects in RF MOSFETs," *IEEE Transactions on Electron Devices*, vol. 48, no. 7, pp. 1374-1379, Jul 2001.

[32] J. C. Rautio, V. I. Okhmatovski, "Unification of double-delay and SOC electromagnetic deembedding," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2892-2898, Sept. 2005.

[33] M. W. Pospieszalski, "Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1340-1350, Sept. 1989.

[34] J. Stenarson, M. Garcia, I. Angelov, H. Zirath, "A general parameter-extraction method for transistor noise models," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2358-2363, Dec 1999.

[35] H. Hillbrand, P. Russer, "An efficient method for computer aided noise analysis of linear amplifier networks," *IEEE Transactions on Circuits and Systems*, vol. 23, no. 4, pp. 235-238, Apr 1976.

[36] M. Kantanen, M. Lahdes, T. Vähä-Heikkilä, and J. Tuovinen, “A wideband on-wafer noise parameter measurement system at 50–75 GHz,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 5, pp. 1489–1495, May 2003.

[37] E. H. Armstrong, "The Super-Heterodyne-Its Origin, Development, and Some Recent Improvements," *Proceedings of the Institute of Radio Engineers*, vol. 12, no. 5, pp. 539-552, Oct. 1924.

[38] W. Schottky, "On the Origin of the Super-Heterodyne Method," *Proceedings of the Institute of Radio Engineers*, vol. 14, no. 5, pp. 695-698, Oct. 1926.

[39] F. M. Colebrook, “Homodyne,” *Wireless World and Radio Review*, vol. 13, pp. 645-648, 1924.

[40] D. G. Tucker, "The Synchrodyne," *Electronic Eng.*, 19, pp. 75-76, Mar. 1947.

[41] D. G. Tucker, "The History of the Homodyne and the Synchrodyne," *Journal of the British Institution of Radio Engineers 14*, pp. 143–154, Apr. 1954.

[42] B. Razavi, "Design of Millimeter-Wave CMOS Radios: A Tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 1, pp. 4-16, Jan. 2009.

[43] H. T. Friis, "Noise Figures of Radio Receivers," *Proceedings of the IRE*, vol. 32, no. 7, pp. 419-422, Jul. 1944.

[44] J.-S. Goo, H.-T. Ahn, D. J. Ladwig, Z. Yu, T. H. Lee, R. W. Dutton, "A noise optimization technique for integrated low-noise amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 994-1002, Aug 2002.

[45] Y. H. Wu, A. Chin, C. S. Liang, C. C. Wu, "The performance limiting factors as RF MOSFETs scale down," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Boston, MA, Jun. 2000, pp. 151-155.

[46] K. H. K. Yau, T. Chalvatzis, A. M. Mangan, E. Laskin, R. Beerkens, P. Westergaard, M. Tazlauanu, M.-T. Yang, S. P. Voinigescu, “The invariance of characteristic current densities in nanoscale MOSFETs and its impact on algorithmic design methodologies and design porting of Si(Ge) (Bi)CMOS high-speed building blocks,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1830–1845, Aug. 2006.

[47] B. Hughes, "Designing FET's for broad noise circles," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 2, pp.190-198, Feb. 1993.

[48] H. A. Haus and R. B. Adler, “Optimum noise performance of linear amplifiers,” *Proceeding of the IRE*, vol. 46, no. 8, pp. 1517–1533, Aug. 1958.

[49] J. Engberg, “Simultaneous input power match and noise optimization using feedback,” in *Proc. of the 4th European Microwave Conference*, Montreux, Switzerland, Sept. 1974, pp. 385-389.

[50] S. Weinreb, J. C. Bardin, H. Mani, "Design of Cryogenic SiGe Low Noise Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 11, pp. 2306-2312, Nov. 2007.

[51] H. Fukui, “Available power gain, noise figure and noise measure of two ports and their graphical representation,” *IEEE Transactions on Circuit Theory*, vol. CT-13, pp. 137–142, Jun. 1966.

[52] C. R. Poole, D. K. Paul, "Optimum Noise Measure Terminations for Microwave Transistor Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 11, pp. 1254-1257, Nov 1985.

[53] H. S. Black, "Stabilized feed-back amplifiers", *Electrical Engineering*, vol. 53, pp. 114-120, Jan. 1934.

[54] R. E. Lehmann, D. D. Heston, "X-band monolithic series feedback LNA," *IEEE Transactions on Electron Devices*, vol. 32, no. 12, pp. 2729-2735, Dec. 1985.

[55] J. M. Rollett, "Stability and Power-Gain Invariants of Linear Twoports," *IRE Transactions on Circuit Theory*, vol. 9, no. 1, pp. 29-32, Mar. 1962.

[56] K. Wang, M. Jones, S. Nelson, "The S-probe-a new, cost-effective, 4-gamma method for evaluating multi-stage amplifier stability," in *IEEE MTT-S International Microwave Symposium Digest*, Albuquerque, NM, Jun. 1992, pp. 829-832.

[57] R. Hartley, “Modulation System”, U. S. Patent 1,666,206, Apr. 1928.

[58] D. E. Norgaard, “The Phase-Shift Method of Single-Sideband Signal Reception”, *Proceedings of the I.R.E.*, vol. 44, pp. 1735-1743, Dec. 1956.

[59] K. Kawakami, M. Shimozawa, H. Ikematsu, K. Itoh, Y. Isota, O. Ishida, ”A Millimeter-Wave Broadband Monolithic Even Harmonic Image Rejection Mixer”, in *IEEE MTT-S International Microwave Symposium Digest*, Maryland, MD, Jun. 1998, pp. 1443-1446.

[60] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 4, pp. 365-373, Dec. 1968.

[61] B. Gilbert, "The MICROMIXER: a highly linear variant of the Gilbert mixer using a bisymmetric Class-AB input stage," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 9, pp. 1412-1423, Sept. 1997.

[62] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 17-22, Jan. 2006.

[63] A. W. Dearn, L. M. Devlin, "A MM-wave monolithic Gilbert-cell mixer," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Boston, MA, Jun. 2000, pp. 267-270.

[64] C.-S. Lin, P.-S. Wu, H.-Y. Chang, H. Wang, “A 9-50 GHz Gilbert-Cell Down-Conversion Mixer in 0.13-μm CMOS Technology,” *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 5, pp. 293-295, May 2006.

[65] S. A. Maas, *Microwave Mixers*, Second Edition, Artech House, Norwood, MA, p. 375, 1993.

[66] S. A. Maas, *Nonlinear Microwave and RF Circuits*, Second Edition, Artech House, Norwood, MA, p. 587, 2003.

[67] T. Vaha-Heikkila, M. Lahdes, M. Kantanen, J. Tuovinen, "On-wafer noise-parameter measurements at W-band," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 6, pp. 1621-1628, Jun. 2003.

[68] M. Lahdes, "Uncertainty Analysis of V-Band on-Wafer Noise Parameter Measurement System," in *Proc. of the 28th European Microwave Conference*, Amsterdam, the Netherlands, Oct. 1998, pp. 445-450.

[69] W. Winkler, J. Borngraber, F. Korndorfer, C. Scheytt, "94 GHz Amplifier in SiGe Technology," in *Proc. of the 38th European Microwave Conference*, Amsterdam, the Netherlands, Oct. 2008, pp. 167-170.

[70] M. Sato, T. Hirose, T. Ohki, H. Sato, K. Sawaya, K. Mizuno, "94-GHz Band High-Gain and Low-Noise Amplifier Using InP-HEMTs for Passive Millimeter Wave Imager," in *IEEE MTT-S International Microwave Symposium Digest*, Honolulu, HI, Jun. 2007, pp. 1775-1778.

[71] A. Tessmann, A. Leuther, C. Schwoerer, H. Massler, S. Kudszus, W. Reinert, M. Schlechtweg, "A coplanar 94 GHz low-noise amplifier MMIC using 0.07 μm metamorphic cascode HEMTs," in *IEEE MTT-S International Microwave Symposium Digest*, Philadelphia, PA, Jun. 2003, pp. 1581-1584.

[72] R. Majidi-Ahy, M. Riaziat, C. Nishimoto, M. Glenn, S. Silverman, S. Weng, Y. C. Pao, G. Zdasiuk, S. Bandy, Z. Tan, "94 GHz InP MMIC five-section distributed amplifier," *Electronics Letters*, vol. 26, no. 2, pp. 91-92, Jan. 1990.

[73] H. Wang, K. Tan, G. S. Dow, J. Berenz, D. Garske, P. Rodgers, G. Hayashibara, "State-of-the-art low noise performance of 94 GHz monolithic amplifiers using 0.1 μm InGaAs/GaAs pseudomorphic HEMT technology," in *International Electron Devices Meeting Technical Digest*, Washington, DC, Dec. 1991, pp. 939-942.

[74] H. Wang, T.-N. Ton, R. Lai, D. C.-W. Lo, S. Chen, D. Streit, G. S. Dow, K. L. Tan, J. Berenz, "Low noise and high gain 94 GHz monolithic InP-based HEMT amplifiers," in *International Electron Devices Meeting Technical Digest*, Washington, DC, Dec. 1993, pp. 239-242.

[75] X. Bi, Y. Guo, Y. Z. Xiong, M. A. Arasu, M. Je, "A 19.2 mW, Gain and High-Selectivity 94 GHz LNA in 0.13 μm SiGe BiCMOS," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 5, pp. 261-263, May 2013.

[76] S.-W. Moon; Y.-H. Baek, J.-H. Oh, M. Han, J.-K. Rhee; S. D. Kim, "New small-signal modelling method for W-band MHEMT-based amplifier design," in *Proc. of the European Microwave Conference*, Paris, France, Sept. 2010, pp. 1146-1149.

[77] R. R. Severino, T. Taris, Y. Deval, D. Belot, J.-B. Begueret, "A SiGe:C BiCMOS LNA for 94GHz band applications," in *Proc. of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Austin, TX, Oct. 2010, pp. 188-191.

[78] T. T. L. Nguyen, S.-W. Moon, S.-H. Jung; M. Han, J.-K. Rhee, S. D. Kim, "A W-band cascaded double-stage distributed low-noise amplifier using feedback transmission line," in *Proc. of the Asia-Pacific Microwave Conference*, Yokohama, Japan, Dec. 2010, pp. 382-385.

[79] L. Gilreath, V. Jain, H.-C. Yao; L. Zheng; P. Heydari, "A 94-GHz passive imaging receiver using a balanced LNA with embedded Dicke switch," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Anaheim, CA, May 2010, pp. 79-82.

[80] R. Pilard, D. Gloria, F. Gianesello, F. Le Pennec, C. Person, "94 GHz silicon co-integrated LNA and Antenna in a mm-wave dedicated BiCMOS technology," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Anaheim, CA, May 2010, pp. 83-86.

[81] E. W. Bryerton, X. Mei, Y.-M. Kim, W. Deal, W. Yoshida, M. Lange, J. Uyeda, M. Morgan, R. Lai, "A W-band low-noise amplifier with 22K noise temperature," in *IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, Jun. 2009, pp. 681-684.

[82] H. Essen, M. Brautigam, R. Sommer, A. Wahlen, W. Johannes, J. Wilcke, M. Schlechtweg, A. Tessmann, "SUMATRA, a W-band SAR for UAV application," in *Proc. of the International Radar Conference*, Bordeaux, France, Oct. 2009, pp. 1-4.

[83] W. Winkler, J. Borngraber, F. Korndorfer, C. Scheytt, "94 GHz Amplifier in SiGe Technology," in *Proc. of the 38th European Microwave Conference*, Amsterdam, the Netherlands, Oct. 2008, pp. 167-170.

[84] J. Powell, H. Kim, C. G. Sodini, "SiGe Receiver Front Ends for Millimeter-Wave Passive Imaging," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 11, pp. 2416-2425, Nov. 2008.

[85] X. B. Mei, C. H. Lin, L. J. Lee, Y.-M. Kim, P.-H. Liu, M. Lange, A. Cavus, R. To, M. Nishimoto, R. Lai, "A W-band InGaAs/InAlAs/InP HEMT Low-Noise Amplifier MMIC with 2.5dB noise figure and 19.4 dB gain at 94GHz," in *Proc. of the 20th International Conference on Indium Phosphide and Related Materials*, Versailles, France, May 2008, pp. 1-3.

[86] M. Sato, T. Hirose, T. Ohki, T. Takahashi, K. Makiyama, N. Hara, H. Sato, K. Sawaya, K. Mizuno, "InP-HEMT MMICs for passive millimeter-wave imaging sensors," in *Proc. of the 20th International Conference on Indium Phosphide and Related Materials*, Versailles, France, May 2008, pp. 1-4.

[87] J. B. Hacker, J. Bergman, G. Nagy, G. Sullivan, C. Kadow, H.-K. Lin, A. C. Gossard, M. Rodwell, B. Brar, "An ultra-low power InAs/AlSb HEMT W-band low-noise amplifier," in *IEEE MTT-S International Microwave Symposium Digest*, Long Beach, CA, Jun. 2005, pp. 1029-1032.

[88] W. R. Deal, R. Tsai, M. D. Lange, J. B. Boos, B. R. Bennett, A. Gutierrez, "A W-band InAs/AlSb low-noise/low-power amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 4, pp. 208-210, Apr. 2005.

[89] M. Schlechtweg, A. Tessmann, A. Leuther, C. Schworer, H. Massler, M. Mikulla, M. Walther, M. Riessle, "Advanced mm-wave ICs and applications," in *Proc. of the IEEE International Workshop on Radio-Frequency Integration Technology: Integrated Circuits for Wideband Communication and Wireless Sensor Networks*, Singapore, Republic of Singapore, Dec. 2005, pp. 46-49.

[90] M. Kärkkäinen, M. Varonen, M. Kantanen, T. Karttaavi, P. Kangaslahti, K. Halonen, "Low noise amplifiers for 94 GHz cloud radar," in *Proc. of the 34th European Microwave Conference*, Amsterdam, the Netherlands, Oct. 2004, pp. 33-36.

[91] A. Tessmann, A. Leuther, C. Schworer, H. Massler, W. Reinert, M. Walther, R. Losch, M. Schlechtweg, "Millimeter-wave circuits based on advanced metamorphic HEMT technology," in *Joint 29th International Conference on Infrared and Millimeter Waves and 12th International Conference on Terahertz Electronics Conference Digest*, Karlsruhe, Germany, Oct. 2004, pp. 165-166.

[92] M. Schlechtweg, A. Leuther, A. Tessman, C. Schworer, H. Massler, W. Reinert, M. Lang, U. Nowotny, O. Kappeler, M. Walther, R. Losch, "Millimeter-wave and mixed-signal integrated circuits based on advanced metamorphic HEMT technology," in *Proc. of the International Conference on Indium Phosphide and Related Materials*, Kagoshima, Japan, Jun. 2004, pp. 609-614.

[93] A. Tessmann, A. Leuther, C. Schwoerer, H. Massler, S. Kudszus, W. Reinert, M. Schlechtweg, "A coplanar 94 GHz low-noise amplifier MMIC using 0.07 µm metamorphic cascode HEMTs," in *IEEE MTT-S International Microwave Symposium Digest*, Philadelphia, PA, Jun. 2003, pp. 1581-1584.

[94] A. Leuther, A. Tessmann, M. Dammann, W. Reinert, M. Schlechtweg, M. Mikulla, M. Walther, G. Weimann, "70 nm low-noise metamorphic HEMT technology on 4 inch GaAs wafers," in *Proc. of the International Conference on Indium Phosphide and Related Materials*, May 2003, pp. 215-218.

[95] A. Tessmann, W. H. Haydl, M. Neumann, J. Rudiger, "W-band cascode amplifier modules for passive imaging applications," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 5, pp. 189-191, May 2000.

[96] A. Chamseddine, M. Klingler, M. Heddebaut, B. Bocquet, N. Rolland, P. Noirel, "Real-time low-cost passive imaging system for automotive applications," in *Proc. of the IEEE-VTS Fall VTC 52nd Vehicular Technology Conference*, Boston, MA, Sept. 2000 , pp. 2033-2038.

[97] D. L. Edgar, H. McLelland, S. Ferguson, N. I. Cameron, M. Holland, I. G. Thayne, M. R. S. Taylor, C. R. Stanley, S. P. Beaumont, "94 and 150 GHz coplanar waveguide MMIC amplifiers realized using InP technology," in *IEEE MTT-S International Microwave Symposium Digest*, Anaheim, CA, Jun. 1999, pp. 247-250.

[98] W. H. Haydl, M. Neumann, L. Venveyen, A. Bangert, S. Kudszus, M. Schlechtweg, A. Hulsmann, A. Tessmann, W. Reinert, T. Krems, "Single-chip coplanar 94-GHz FMCW radar sensors," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 2, pp. 73-75, Feb 1999.

[99] A. Werthof, T. Gravel, W. Kellner, "W-band amplifier fabricated by optical stepper lithography," in *IEEE MTT-S International Microwave Symposium Digest*, Anaheim, CA, Jun. 1999, pp. 689-692.

[100] A. Tessmann, W. H. Haydl, T. Krems, M. Neumann, H. Massler, L. Verweyen, A, Hulsmann, M. Schlechtweg, "A compact coplanar W-band variable gain amplifier MMIC with wide control range using dual-gate HEMTs," in *IEEE MTT-S International Microwave Symposium Digest*, Baltimore, MD, Jun. 1998, pp. 685-688.

[101] M. Berg, T. Hackbarth, J. Dickmann, "80-100 GHz broadband amplifier MMIC utilizing CPWs and quarter micron InP-based HEMTs," in *Proc. of the International Conference on Indium Phosphide and Related Materials*, Cape Cod, MA, May 1997, pp. 245-248.

[102] S. Weinreb, R. Lai, N. Erickson, T. Gaier, J. Wielgus, "W-band InP wideband MMIC LNA with 30 K noise temperature," in *IEEE MTT-S International Microwave Symposium Digest*, Anaheim, CA, Jun. 1999, pp. 101-104.

[103] M. Matloubian, "Advances in millimeter-wave FET MMIC technology," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Anaheim, CA, Jun. 1999, pp. 141-144.

[104] R. Lai, M. Barsky, T. Huang, M. Sholley, H. Wang, Y.-L. Kok, D. C. Streit, T. Block, P.-H. Liu, T. Gaier, L. Samoska, "An InP HEMT MMIC LNA with 7.2-dB gain at 190 GHz," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 11, pp. 393-395, Nov. 1998.

[105] J. W. Archer, R. Lai, "Ultra-low-noise InP-MMIC amplifiers for 85-115 GHz," in *Proc. of the Asia-Pacific Microwave Conference*, Sydney, Australia, 2000, pp. 173-176.

[106] V. Hoel, S. Boret, B. Grimbert, G. Aperce, S. Bollaert, H. Happy, X. Wallart, A. Cappy, "94-GHz low noise amplifier on InP in coplanar technology," in *Proc. of the European Gallium Arsenide and Related III-V Compound Applications Symposium*, Munich, Germany, Oct. 1999, pp. 257-262.

[107] M. Varonen, P. Larkoski, A. Fung, L. Samoska, P. Kangaslahti, T. Gaier, R. Lai, S. Sarkozy, "160-270-GHz InP HEMT MMIC Low-Noise Amplifiers," in *IEEE Compound Semiconductor Integrated Circuit Symposium Technical Digest*, La Jolla, CA, Oct. 2012, pp. 1-4.

[108] M. Sato, S. Shiba, H. Matsumura, T. Takahashi, T. Suzuki, Y. Nakasha, N. Hara, "Submillimeter-wave InP HEMT amplifiers with current-reuse topology," in *Proc. of the IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Austin, TX, Jan. 2013, pp. 150-152.

[109] B. Zhang; Y.-Z. Xiong, L. Wang, S. Hu, L.-W. Li, "Gain-enhanced 132-160 GHz low-noise amplifier using 0.13 µm SiGe BiCMOS," *Electronics Letters*, vol. 48, no. 5, pp. 257-259, Mar. 2012.

[110] L. Gang, H. Schumacher, "47–77 GHz and 70–155 GHz LNAs in SiGe BiCMOS technologies," in *Proc. of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Portland, OR, Oct. 3 2012, pp. 1-4.

[111] M. Kantanen, M. Varonen, M. Kärkkäinen, T. Karttaavi, R. Weber, A. Leuther, M. Seelmann-Eggebert, T. Narhi, K. A. I. Halonen, "Coplanar 155 GHz MHEMT MMIC low noise amplifiers," in *Proc. of the Asia-Pacific Microwave Conference*, Yokohama, Japan, Dec. 2006, pp. 173-176.

[112] M. Schlechtweg, I. Kallfass, A. Tessmann, C. Schworer, A. Leuther, "Millimeter-Wave Front-End Components in Metamorphic HEMT Technology," in *Proc. of the 1st European Microwave Integrated Circuits Conference*, Manchester, United Kingdom, Sept. 2006, pp. 31-34.

[113] R. Lai, H. Wang, Y. C. Chen, T. Block, P.-H. Liu, D. C. Streit, D. Tran, P. Siegel, M. Barsky, W. Jones, T. Gaier, "D-band MMIC LNAs with 12 dB gain at 155 GHz fabricated on a high yield InP HEMT MMIC production process," in *Proc. of the International Conference on Indium Phosphide and Related Materials*, Cape Cod, MA, May 1997, pp. 241-244.

[114] H. Wang; R. Lai, Y.-L. Kok, T.-W. Huang; M. V. Aust, Y. C. Chen, P. H. Siegel, T. Gaier, R. J. Dengler, B. R. Allen, "A 155-GHz monolithic low-noise amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1660-1666, Nov 1998.

[115] E. Ojefors, F. Pourchon, P. Chevalier, U. R. Pfeiffer, "A 160-GHz low-noise downconverter in a SiGe HBT technology," in *Proc. of the European Microwave Conference*, Paris, France, Sept. 2010, pp. 521-524.

[116] P. Huang, R. Lai, R. Grundbacher, B. Gorospe, "A 20-mW G-band Monolithic Driver Amplifier Using 0.07-µm InP HEMT," in *IEEE MTT-S International Microwave Symposium Digest*, Manchester, United Kingdom, Jun. 2006, pp. 806-809.

[117] M. Kantanen, M. Kärkkäinen, S. Caujolle-Bert, M. Varonen, R. Weber, M. Seelmann-Eggebert, A. Leuther, P. Jukkala, T. Närhi, K. A. I. Halonen,"Low noise amplifiers for G-band radiometers," in *Proc. of the 4th Global Symposium on Millimeter Waves*, Espoo, Finland, May 2011, pp. 1-4.

[118] H. Wang; K.-Y. Lin, Z.-M. Tsai, L.-H. Lu, H.-C. Lu; C.-H. Wang; J.-H. Tsai, T.-W. Huang, Y.-C. Lin, "MMICs in the millimeter-wave regime," *IEEE Microwave Magazine*, vol. 10, no. 1, pp. 99-117, Feb. 2009.

[119] E. Ojefors, B. Heinemann, U. R. Pfeiffer, "Subharmonic 220- and 320-GHz SiGe HBT Receiver Front-Ends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 5, pp. 1397-1404, May 2012.

[120] A. Tessmann, H. Massler, U. Lewark, S. Wagner, I. Kallfass, A. Leuther, "Fully Integrated 300 GHz Receiver S-MMICs in 50 nm Metamorphic HEMT Technology," in *IEEE Compound Semiconductor Integrated Circuit Symposium Technical Digest*, Kona, HI, Oct. 2011, pp. 1-4.

[121] Y. Zhao; E. Ojefors, K. Aufinger, T. F. Meister, U. R. Pfeiffer, "A 160-GHz Subharmonic Transmitter and Receiver Chipset in an SiGe HBT Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3286-3299, Oct. 2012.

[122] E. Laskin, M. Khanpour, S. T. Nicolson, A. Tomkins, P. Garcia, A. Cathelin, D. Belot, S. P. Voinigescu, "Nanoscale CMOS Transceiver Design in the 90–170-GHz Range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3477-3490, Dec. 2009.

[123] A. Tang, G. Virbila, D. Murphy, F. Hsiao, Y. H. Wang, Q. J. Gu, Z. Xu, Y. Wu, M. Zhu, M.-C. F. Chang, "A 144GHz 0.76cm-resolution sub-carrier SAR phase radar for 3D imaging in 65nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2012, pp. 264-266.

[124] S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Gordon, G. Xiang, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, C. H. Doan, "A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2011, pp. 164-166.

[125] E. Cohen, M. Ruberto, M. Cohen, O. Degani, S. Ravid, D. Ritter, "A CMOS Bidirectional 32-Element Phased-Array Transceiver at 60 GHz With LTCC Antenna," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1359-1375, Mar. 2013.

[126] J. Luna, A. Zevallos, A. Siligaris, C. Pujol, L. Dussopt, "A packaged 60 GHz low-power transceiver with integrated antennas for short-range communications," in *Proc. of the IEEE Radio and Wireless Symposium*, Austin, TX, Jan. 2013, pp. 355-357.

[127] A. Natarajan, S. K. Reynolds, M.-D. Tsai, S. T. Nicolson, J.-H. C. Zhan, D. G. Kam, D. Liu, Y.-L. O. Huang, A. Valdes-Garcia, B. A. Floyd, "A Fully-Integrated 16-Element Phased-Array Receiver in SiGe BiCMOS for 60-GHz Communications," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1059-1075, May 2011.

[128] K.-C. Lin, H.-K. Chiou, K.-H. Chien, T.-Y. Yang, P.-C. Wu, C.-L. Ko, Y.-Z. Juang, "A 4.2-mW 6-dB Gain 5–65-GHz Gate-Pumped Down-Conversion Mixer Using Darlington Cell for 60-GHz CMOS Receiver," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1516-1522, Apr. 2013.

[129] A. Axholt, H. Sjoland, "A 60 GHz receiver front-end with PLL based phase controlled LO generation for phased-arrays," in *Proc. of the Asia-Pacific Microwave Conference*, Melbourne, Australia, Dec. 2011, pp. 1534-1537.

[130] K.-S. Yeo, K. M. Lim, J. Gu; J. Yan, K. Wang, Y. Lu, R. Pan, W. M. Lim; J.-G. Ma, "A fully integrated 0.18 μm SiGe BiCMOS low power 60 GHz receiver & transmitter for high data rate wireless communications," in *Proc. of the IEEE International Conference of Electron Devices and Solid-State Circuits*, Tianjin, China, Nov. 2011, pp. 1-2.

[131] C.-C. Chen, Y.-S. Lin, J.-H. Lee, J.-F. Chang, "A 60 GHz CMOS receiver front-end with integrated 180° out-of-phase wilkinson power divider," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Anaheim, CA, May 2010, pp. 373-376.

[132] P. Sakian, R. Mahmoudi, P. van Zeijl, M. Lont, A. Van Roermund, "A 60-GHz double-balanced homodyne down-converter in 65-nm CMOS process," in *Proc. of the European Microwave Integrated Circuits Conference*, Rome, Italy, Sept. 2009, pp. 258-261.

[133] C.-S. Wang, J.-W. Huang, K.-D. Chu, C.-K. Wang, "A 60-GHz Phased Array Receiver Front-End in 0.13- CMOS Technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 10, pp. 2341-2352, Oct. 2009.

[134] N.-Y. Wang, H. Wu, J. Y.-C. Liu, M.-C. F. Chang, "65 nm CMOS receiver with 4.2 dB NF and 66 dB gain for 60 GHz applications," *Electronics Letters*, vol. 47, no. 1, pp. 15-17, Jan. 2011.

[135] A. Tomkins, R. A. Aroca, T. Yamamoto, S. T. Nicolson, Y. Doi, S. P. Voinigescu, "A Zero-IF 60 GHz 65 nm CMOS Transceiver With Direct BPSK Modulation Demonstrating up to 6 Gb/s Data Rates Over a 2 m Wireless Link," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2085-2099, Aug. 2009.

[136] K. Scheir, S. Bronckers, J. Borremans, P. Wambacq, Y. Rolain, "A 52 GHz Phased-Array Receiver Front-End in 90 nm Digital CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2651-2659, Dec. 2008.

[137] A. Natarajan, B. Floyd, A. Hajimiri, "A Bidirectional RF-Combining 60GHz Phased-Array Front-End," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2007, pp. 202-597.

[138] E. Cohen, C. G. Jakobson, S. Ravid, D. Ritter, "A Bidirectional TX/RX Four-Element Phased Array at 60 GHz With RF-IF Conversion Block in 90-nm CMOS Process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1438-1446, May 2010.

[139] Y. Yikun, P. Baltus, A. Van Roermund, A. de Graauw, E. van der Heijden, M. Collados, C. Vaucher, "A 60GHz digitally controlled RF-beamforming receiver front-end in 65nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium Digest of Papers*, Boston, MA, Jun. 2009, pp. 211-214.

[140] S. E. Gunnarsson, C. Karnfelt, H. Zirath, R. Kozhuharov, D. Kuylenstierna, A. Alping, C. Fager, "Highly integrated 60 GHz transmitter and receiver MMICs in a GaAs pHEMT technology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2174-2186, Nov. 2005.

[141] C.-H. Yu, P.-H. Lo, J.-Y. Lyu, H.-C. Kuo, H.-R. Chuang, "Integrated 60-GHz CMOS variable-gain low-noise amplifier and full 360° phase shifter for phased-array RF receiving system," in *Proc. of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems (SiRF)*, Newport Beach, CA, Jan. 2014, pp. 59-61.

[142] L. A. Samoska, "An Overview of Solid-State Integrated Circuit Amplifiers in the Submillimeter-Wave and THz Regime," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 9-24, Sept. 2011.

[143] Z. Durrani, M. Jones, M. Kaestner, M. Hofer, E. Guliyev, A. Ahmad, T. Ivanov, J.-P. Zoellner, I. W. Rangelow, “Scanning probe lithography approach for beyond CMOS devices,” in *Proceedings of the SPIE Advanced Lithography: Alternative Lithographic Technologies V*, Vol. 8680, San Jose, CA, Feb. 2013, pp. 1-12.

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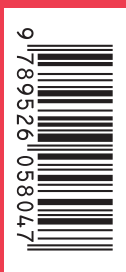


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