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Broadband filter design

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This thesis presents the design of an active filter implemented in a 65nm CMOS technology and based on super source follower. The original filter was 5th order low-pass Chebyshev-type with a cut-off frequency of 160 MHz, but it was to be changed into Butterworth-type because of the results, here both designs are shown. The architecture is fully differential and it is based on Sallen-Key biquad structures with super source follower as an active element and resistors and capacitors as passive elements.

The design process starts with a study of the super source follower and a comparison of this circuit with the normal source follower. After that the work is divided into different stages in order to get an easy design flow, starting with ideal models including limited bandwidth and gain, and then simulations with transistor level active elements are performed.

Finally, some measurements are presented to analyze the noise and linearity performance of the filter.

Keywords: broadband, filter, super source, Chebyshev, Sallen-Key

Contents

Abstract	ii
Contents	iii
List of Figures	iv
1 Introduction	1
2 Background Information	2
2.1 Source follower	2
2.2 Super source follower	2
2.3 Sallen-Key topology	3
3 Materials and Method	7
4 Filter Design	8
4.1 Ideal Design	8
4.1.1 Source Follower	8
4.1.2 Super Source Follower	9
4.1.3 Active Element	14
4.1.4 Filter	16
4.2 Real Design	16
4.2.1 Source Follower	16
4.2.2 Super Source Follower	21
4.2.3 Active Elements	29
4.2.4 Chebyshev Filter	33
4.2.5 Butterworth Filter	34
5 Filter Performance	39
References	44

List of Figures

1	Source follower schematic.	3
2	Super source follower schematic.	4
3	General Sallen-Key low-pass biquad.	4
4	Ideal source follower schematic.	9
5	Transistor width sweep. Ideal source follower. Gain vs Width.	10
6	Transistor width sweep. Ideal source follower. Transfer functions.	10
7	Transistor width sweep 2. Ideal source follower. Gain vs Width.	11
8	Transistor width sweep 2. Ideal source follower. Transfer functions.	11
9	Transistor length sweep. Ideal source follower. Gain vs Length.	12
10	Transistor length sweep. Ideal source follower. Transfer functions.	12
11	Current sweep. Ideal source follower. Gain vs Current.	13
12	Current sweep. Ideal source follower. Transfer functions.	13
13	Ideal pMOS super source follower schematic.	14
14	Ideal nMOS super source follower schematic.	14
15	Ideal filter schematic.	15
16	Ideal filter transfer function	15
17	Current mirror transistors width sweep. Source follower. Gain vs Width.	17
18	Current mirror transistors width sweep. Source follower. Transfer functions.	17
19	Current mirror transistors length sweep. Source follower. Gain vs Length.	18
20	Current mirror transistors length sweep. Source follower. Transfer functions.	18
21	Current sweep. Source follower. Gain vs Current.	19
22	Current sweep. Source follower. Transfer functions.	19
23	Bias voltage sweep. Source follower. Gain vs Bias voltage.	20
24	Bias voltage sweep. Source follower. Transfer functions.	20
25	pMOS super source follower schematic.	22
26	Current sweep. pMOS super source follower	22
27	Current ratio sweep. pMOS super source follower. Gain vs Current Ratio.	23
28	Current ratio sweep. pMOS super source follower. Transfer functions.	23
29	Width coefficient sweep. pMOS super source follower. Gain vs Width coefficient.	24
30	Width coefficient sweep. pMOS super source follower. Transfer functions.	24
31	Ideal version vs Real version. pMOS super source follower	25
32	Ideal version vs Real version. nMOS super source follower	25
33	Main transistors length sweep. nMOS super source follower. Gain vs Length.	27
34	Main transistors length sweep. nMOS super source follower. Transfer functions.	27

35	M4 transistor width sweep. nMOS super source follower. Gain vs Width.	28
36	M4 transistor width sweep. nMOS super source follower. Transfer functions.	28
37	Circuit schematic of the pMOS version of the complete active element.	30
38	Circuit schematic of the nMOS version of the complete active element.	30
39	M7 transistor width sweep. pMOS super source follower. Gain vs Width.	31
40	M7 transistor width sweep. pMOS super source follower. Transfer functions.	31
41	M7 transistor width sweep. nMOS super source follower. Gain vs Width.	32
42	M7 transistor width sweep. nMOS super source follower. Transfer functions.	32
43	Chebyshev filter transfer function	33
44	Butterworth filter transfer function	35
45	Butterworth filter transfer function without extra capacitors	36
46	Circuit schematic of the Butterworth filter.	36
47	Transfer functions of both Butterworth-type filter versions	37
48	Transfer functions of both Butterworth-type filter versions (Zoom) . .	37
49	Output noise. Super source follower filter	40
50	Output noise. Source follower filter	40
51	Difference between the fundamental frequency component and the third harmonic component	41
52	IIP3 graph. Super source follower filter.	41
53	Phase and group delay. Super source follower filter.	42
54	Detail of the group delay peak. Super source follower filter.	42
55	Phase and group delay. Source follower filter.	43
56	Detail of the group delay peak. Source follower filter.	43

1 Introduction

Low-pass filters are quite usual as the first stage in different systems. In applications where frequencies above some cut-off point have to be eliminated from the input signal, this kind of filters becomes necessary. There are several ways for implementing a filter and they could be divided into two major groups: passive and active filters. The first type utilize resistances, capacitances and inductances to create RLC networks, or whatever combination of these components. The second one uses the same passive components and also active elements, as a simple transistor or more complex amplifiers. Since the filter had to be included in an Integrated Circuit (IC) and the integration of inductances with a high Q factor is not straight forward, the design was implemented as an active filter using resistors and capacitors with amplifiers.

Active filters can be built by using different architectures, Someone presented in [1] the idea of employing the well-know topology described by R.P. Sallen and E. L. Key in [2] with an active element based on a super source follower. This topology is less sensitive to the bandwidth of its active element than others, e.g. gm-C filters, and the use of the super source follower reduces the output impedance of the active element [1]. These characteristics make the super source follower variant of the Sallen-Key topology a good option for designing a broadband filter, as it could achieve large bandwidth and very low output impedance that implies a better transfer function. The higher the output impedance, the lower the Q-factor and the lower the cut-off frequency [1].

The aim of this thesis was to design a 5th order low-pass Chebyshev-type filter with a cut-off frequency of 160 MHz by using the topology described by Someone in [1], making a practical implementation for our purpose, a radar application. The filter pass-band ripple should be smaller than ± 0.5 dB and the input amplitude was 400 mVpp with a 1.2 V power supply. Furthermore, the current consumption was minimized so it was less than 50 mA for the whole filter.

These specifications were not fulfilled with the Chebyshev-type filter due to an excessive peaking near the cut-off frequency. As that peaking effect was related to the high Q-factor needed in the second stage of the filter, the type was changed so the original filter was redesigned to be Butterworth-type.

2 Background Information

2.1 Source follower

The source follower schematic is shown in Figure 1 [3].

In the common-drain configuration (or source follower) the input signal is applied to the gate and the output is taken from the source. From a large-signal standpoint, the output voltage is equal to the input voltage minus the gate-source voltage. The gate-source voltage consists of two parts: the threshold and the overdrive. If both parts are constant, the resulting output voltage is simply offset from the input, and the small-signal gain would be unity. In practice, the body effect changes the threshold voltage, and the overdrive depends on the drain current, which changes as the output voltage changes unless $R_L \rightarrow \infty$. [3, p.195]

When $r_o \rightarrow \infty$ and $R_L \rightarrow \infty$ the expressions for the output resistance and gain of the source follower are [3] :

$$R_o = \frac{1}{g_m + g_{mb}} \quad (1)$$

$$\frac{v_o}{v_i} = \frac{g_m}{g_m + g_{mb}} \quad (2)$$

in which g_m is the transconductance of M1 and g_{mb} is the bulk transconductance of M1. Since the source follower has low output resistance, it is often used as an output stage, that is why it was considered as an alternative to the super source follower, so it was placed in the active element of the Sallen-Key biquad as the output stage.

2.2 Super source follower

One way to reduce the output resistance (of the source follower) is to increase the transconductance by increasing the W/L ratio of the source follower and its dc bias current. However, this approach requires a proportionate increase in the area and power dissipation to reduce R_o . To minimize the area and power dissipation required to reach a given output resistance, the super source follower configuration shown in Figure 2 is sometimes used. This circuit uses negative feedback through M2 to reduce the output resistance. From a qualitative standpoint, when the input voltage is constant and the output voltage increases, the magnitude of the drain current of M1 also increases, in turn increasing the gate-source voltage of M2. As a result, the drain current of M2 increases, reducing the output resistance by increasing the total current that flows into the output node under these conditions. From a dc standpoint, the bias current in M2 is the difference between I_1 and I_2 ; therefore, $I_1 > I_2$ is required for proper operation. [3, p.213]

Assuming ideal current sources, the expressions for the output resistance and gain of the super source follower simplify to [3] :

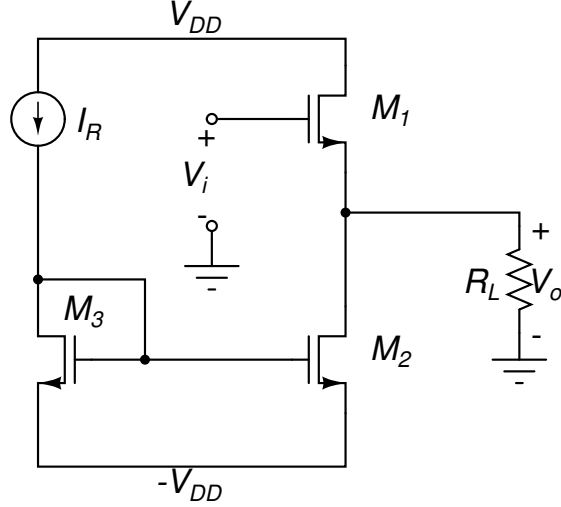


Figure 1: Source follower schematic.

$$R_o = \frac{1}{g_{m1} + g_{mb1}} \left(\frac{1}{g_{m2}r_{o1}} \right) \quad (3)$$

$$\frac{v_o}{v_i} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{1}{g_{m2}r_{o2}}} \quad (4)$$

in which g_{m1} is the transconductance of M1, g_{m2} is the transconductance of M2, r_{o1} is the output resistance of M1, r_{o2} is the output resistance of M2 and g_{mb1} is the bulk transconductance of M1. Comparing these two equations with (1) and (2) respectively, show on the one hand that the negative feedback through M2 reduces the output resistance by a factor of $g_{m2}r_{o1}$ and, on the other hand, that the deviation of the gain of the super source follower from unity is greater than with a normal source follower [3].

2.3 Sallen-Key topology

R. P. Sallen and E. L. Key presented in 1955 a practical method to design filters by means of different biquad circuits [2]. These circuits are composed by a RC passive network, which generally has two capacitors and two resistors, and one or two active elements. Second-order transfer functions can be realized by using the appropriate biquad circuit from the catalog presented in [2], it has to be selected depending on the form of the function that has to be implemented, i.e. the type of the filter. With each network in the catalog there is a short table that specifies, for a given choice of parameters, the suitable group of design relations for d , being $d = 1/Q$. The relationships between the variables that are independent of d are also given with each network.

The purpose of this thesis was to design a low-pass filter, so the transfer function

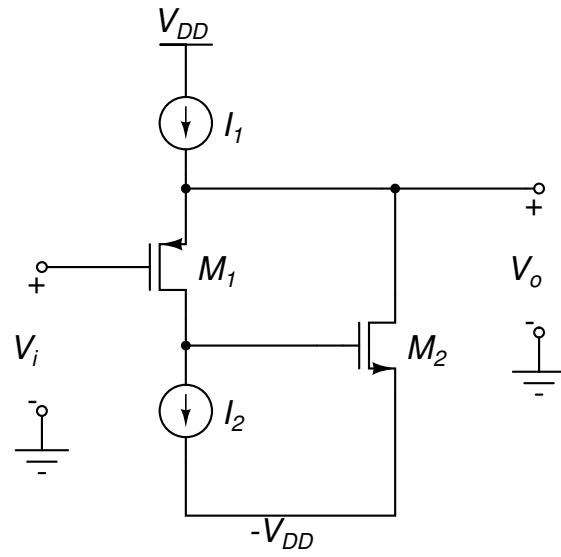


Figure 2: Super source follower schematic.

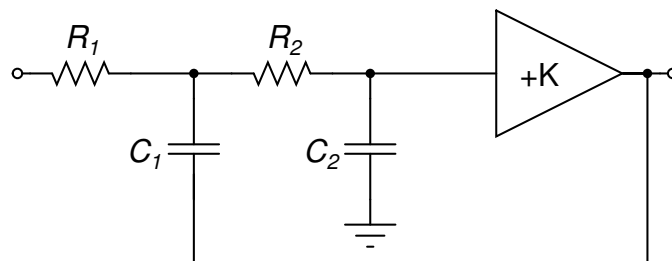


Figure 3: General Sallen-Key low-pass biquad.

was of the form

$$\frac{h}{s^2 + ds + 1}.$$

Between the different biquads that implement this type of transfer function, the first one was chosen (see Figure 3). The design parameters and relationships that the catalog gives for this network are:

$$T_1 = R_1 C_1 \quad (5)$$

$$T_2 = R_2 C_2 \quad (6)$$

$$\rho = \frac{R_1}{R_2} \quad (7)$$

$$\gamma = \frac{C_2}{C_1} \quad (8)$$

$$h = k \quad (9)$$

$$T_1 T_2 = 1 \quad (10)$$

Furthermore, the table with the appropriate groups of design relations for d shows that there are four different groups that can be used. Depending on the parameters that have been selected, groups I, II, III and IV can be employed to determine the correct values of R_1 , R_2 , C_1 and C_2 that perform the targeted transfer function with the desired d , or Q-factor.

As an example of the design flow described in [2], the calculations that are needed to create a 5th order low-pass Chebyshev-type filter are going to be presented. Before that, the complete description of the parameters that define the transfer function of the filter has to be known.

The frequency-scaling factors (FSF) and the Q-factors of the three stages that are necessary to implement the 5th order Chebyshev-type filter are extracted from Table 1. As the third stage is only a single RC pole, the calculations are going to be made for the first two stages.

First of all, two design parameters have to be chosen in order to select the appropriate group of formulas, in this case the parameters were ρ and T_2 in order to control easily the ratio of the resistors and the value of R_2 ; this selection means that group I has to be used. The design flow starts with a formula that gives K_{min} , i.e. the minimum gain of the active element, and assuming $\rho = 1$ and knowing that $d = 0.7149$ for stage 1, the result is:

$$K_{min} = \frac{4(1 + \rho) - d^2}{4(1 + \rho)} = \frac{4(1 + 1) - (0.7149)^2}{4(1 + 1)} = 0.936 \quad (11)$$

FILTER ORDER	Stage 1		Stage 2		Stage 3	
	FSF	Q	FSF	Q	FSF	Q
2	1.0500	0.9565				
3	0.9971	2.0176	0.4942			
4	0.5286	0.7845	0.9932	3.5600		
5	0.6552	1.3988	0.9941	5.5538	0.2895	
6	0.3532	0.7608	0.7468	2.1977	0.9953	8.0012

Table 1: 1-dB Chebyshev Filter Table [4]

Now $K = 1.2$ is set and the next formula can be employed getting:

$$\begin{aligned}
T_2 &= \frac{d}{2(1+\rho)} \left[1 \pm \sqrt{1 - \frac{4(1+\rho)(1-K)}{d^2}} \right] \\
&= \frac{0.7149}{2(1+1)} \left[1 \pm \sqrt{1 - \frac{4(1+1)(1-1.2)}{(0.7149)^2}} \right] = 0.542
\end{aligned} \tag{12}$$

The second solution for the second grade equation was ignored because it was a negative value. In this point $R_2 = 10^6$, $R_1 = R_2$ and $T_2 = 0.542$, so making use of (6) and (10) the rest of the parameters are calculated, being $C_2 = 542 \text{ nF}$, $C_1 = 1.845 \text{ }\mu\text{F}$ and $\gamma = 0.2938$. These results give a normalized transfer function on the basis of 1 radian per second, so the frequency has to be shifted to get the desired one. This is made by altering the passive elements in such a way that ρ and γ stay invariant [2]. Using (13) [4] with $FSF = 0.6552$ and $f_c = 160 \text{ MHz}$ and changing R_2 to $1 \text{ k}\Omega$ these are the new results: $R_1 = R_2 = 1 \text{ k}\Omega$, $C_1 = 2.8 \text{ pF}$ and $C_2 \approx 823 \text{ fF}$. Finally an adjustment of the values might be required to get the correct cut-off frequency.

$$FSF \times f_c = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} = \frac{1}{2\pi R_2 C_1 \sqrt{\rho\gamma}} \tag{13}$$

Repeating all the process for the stage 2 ($FSF = 0.9941$, $d = 0.1806$ and $K = 1.2$), these are the results that were obtained: $R_1 = R_2 = 1 \text{ k}\Omega$, $C_1 = 2.75 \text{ pF}$ and $C_2 \approx 364 \text{ fF}$.

3 Materials and Method

As the purpose of this thesis was to design a filter, the materials employed to carry out the design process were CAD tools and simulators for circuit design and capable to work in transistor level. The procedure followed in every step of the design process was the same. First, the schematic of the circuit that was going to be considered was introduced into the computer by means of Cadence® Virtuoso® Schematic Editor. Second, different simulations were made to verify the circuit or compare its performance with that of a previous one. They could be AC (small signal), DC (operating point), transient, noise and steady-state (SST) analyses, and these can also be done with one or several circuit parameters being swept. Cadence® Virtuoso® Analog Design Environment (ADE), or simply the Linux command line, was used to run the Mentor Graphics® Eldo™ simulator (Eldo™ RF for steady-state analysis). The test bench that was used in the simulations included an output load of a 1 pF capacitor with a $2\text{ k}\Omega$ resistor in parallel to emulate the stage that would be connected to the output of the circuit that was going to be analyze. Finally, some of the results of the analyses were plotted to see the circuit behavior by using either Cadence® WaveScan Waveform Tool or Mentor Graphics® EZwave.

This process was followed through the entire design flow that consisted of several steps that made the filter design easier, avoiding to work with a unique block that would have supposed to consider many variables and parameters at the same time. These steps are divided into two phases: during the first one an intermediate filter was obtained by using ideal current sources and ideal gain blocks, the result was an approximated version of the filter that was useful to have a starting point for the real filter design; after the second phase of the design, the final version of the filter was obtained and, after checking that the specifications were not being fulfilled, the type of the filter was changed and some of the final steps were repeated in order to redesign the filter.

The first step inside each of the phases of the filter design consisted of a study of the source follower and the super source follower, making a comparison between them and trying to get a gain as close to one as possible and a bandwidth of about 1600 MHz . The large bandwidth is needed to minimize the effect of the active element of the Sallen-Key biquad on the filter transfer function, and a gain of one is usually used in the active element of this type of filters. As expected in the real design, the gain of the source follower and the super source follower was not very close to one. Furthermore, a gain greater than one made more flexible the values of the other parameters, so, a gain stage was added to the source follower and super source follower in the second step of the design flow. After obtaining the complete active element that was going to be used in each stage of the filter, the two Sallen-Key biquad sections and the RC single pole were created and analyzed in order to verify individually each one of the transfer functions. Finally, these three stages were putted together to form the complete filter structure.

4 Filter Design

The design flow consisted of several steps that made the filter design easier. Those steps were grouped into two different parts: an ideal one, where ideal current sources and ideal gain blocks were used, and a real one in which the ideal current sources were replaced with current mirrors, and the gain blocks were implemented with real amplifiers.

4.1 Ideal Design

In this part of the design the source follower and the super source follower were studied in order to compare their characteristics. After that, the active elements for the first and second stage of the filter were created by adding a certain gain to the super source follower. Following that, the three stages of the filter were made and analyzed to check their transfer functions. Finally, the entire Chebyshev-type filter was obtained.

4.1.1 Source Follower

The circuit schematic of the source follower that was used in this section is shown in Figure 4. It has equal magnitude (1.2 V) positive and negative power supply and a fully differential architecture, this pattern was used in every single circuit of the filter.

In order to get a gain as close to one as possible and large bandwidth, several parametric simulations were made to see how the gain and the transfer function varied when, the width and length of both transistors, and the current that flow through them, were swept (see Figures 5, 6, 7, 8, 9, 10, 11 and 12).

The first simulation shows an increase in the gain of the source follower caused by an increase in the transistor width, or, being more exact, by an increase in the W/L ratio of the transistor that produces an increase in the transistor transconductance, as equation (14) [5] shows. The higher the transconductance, the closer to one the gain, as relation (2) reveals. The same occurs in the last simulation, where the gain gets closer to one as the current I_D increases because of an increase in the transconductance.

$$g_m \cong \sqrt{(2K'W/L) |I_D|} \quad (14)$$

However, the third simulation shows an increase in the gain until a length of about $0.12 \mu m$, which means that an increase in the gain is now caused by a decrease in the W/L ratio, but that seems to be incorrect according to (14). One possible explanation of this fact could be in the assumption that was done in (2). If $r_o \rightarrow \infty$ is now not assumed, the higher the output resistance of the transistor, the closer to (2) the gain. As $r_o \approx 1/I_D \lambda$ and $\lambda \propto 1/L$, if the length of the transistor increases, the output resistance would also increase and then the gain would rise up. However this explanation only fits with a length up to $0.12 \mu m$, values greater than that will

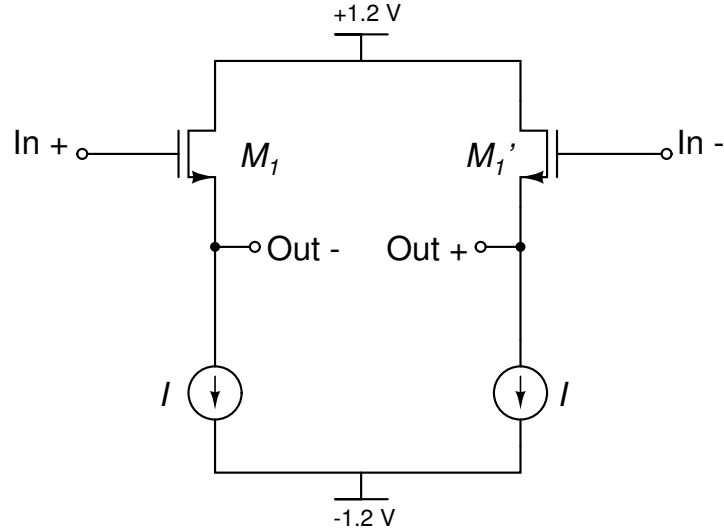


Figure 4: Ideal source follower schematic.

suppose a decrease in the gain, so, maybe the W/L ratio becomes more relevant in that point.

4.1.2 Super Source Follower

The super source follower consists of two transistors and two current sources, which means more parameters to be considered in the simulations. A pMOS version (Figure 13) and an nMOS version (Figure 14) of the super source follower were designed and analyzed because they were employed in the first and the second stage, respectively, of the filter. This is explained later in § 4.2.3.

As it was done with the source follower in the previous section, diverse parametric simulations were done to study the behavior of this circuit when some of its design parameters were swept.

The results of the simulations that were done with the ideal pMOS version of the super source follower show very irregular profiles, with several sharp peaks, which leads not to consider them as valid results to make a comparison with the results of the ideal source follower. However, these results are valuable as a point of departure for the real design of the super source follower. These are the values of the parameters that were chosen to reach a gain of 0.9822 and a bandwidth of about 716 MHz with the pMOS version of the super source follower: $W_1/L_1 = 16/0.12$, $W_2/L_2 = 12/0.12$, $I_1 = 1.5\text{ mA}$, $I_2 = 125\text{ }\mu\text{A}$ and a bias voltage of 0.25 V. These values were selected not to get transistors that were too big and trying to minimize the current consumption.

After the pMOS version of the super source follower had been simulated, the same analyzes were performed with the nMOS version of that circuit, due to the importance of being used in the second stage of the filter. In this case, the results of

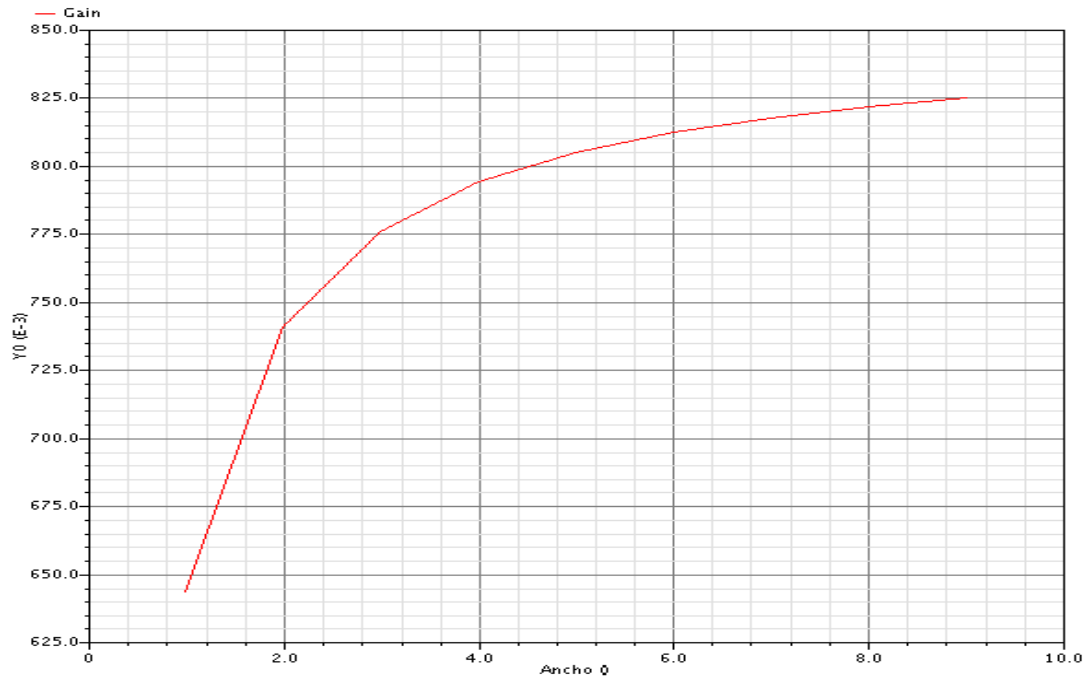


Figure 5: Transistor width sweep from 1 to 9 μm with an increment of 1 μm . Gain vs Width.

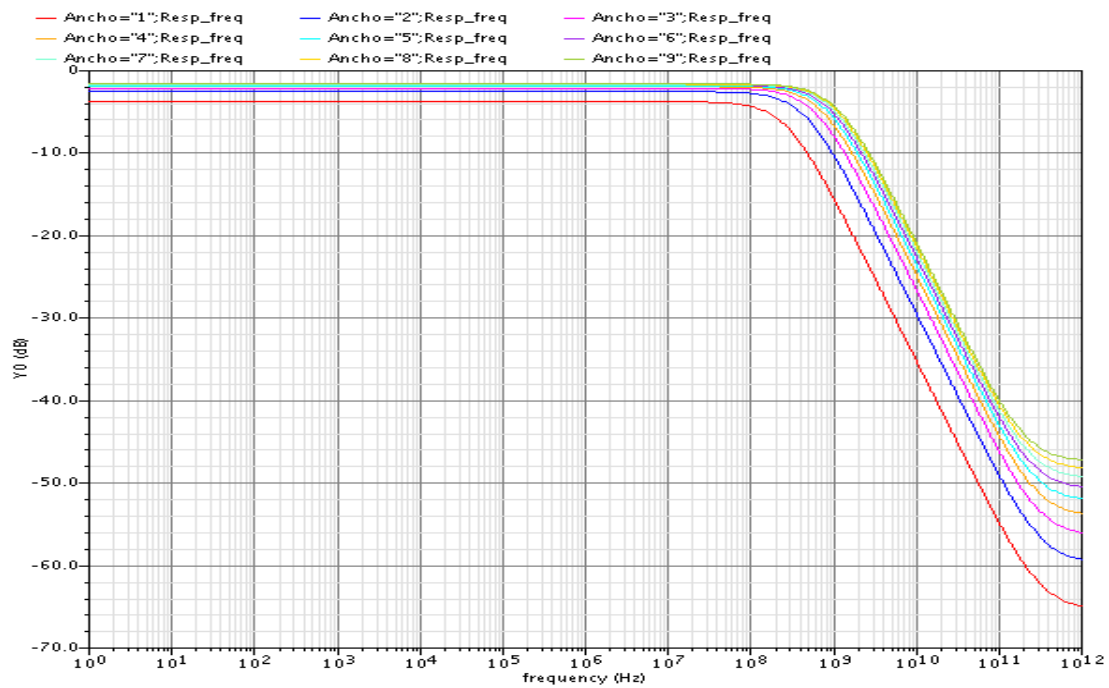


Figure 6: Transistor width sweep from 1 to 9 μm with an increment of 1 μm . Transfer function for each width value.

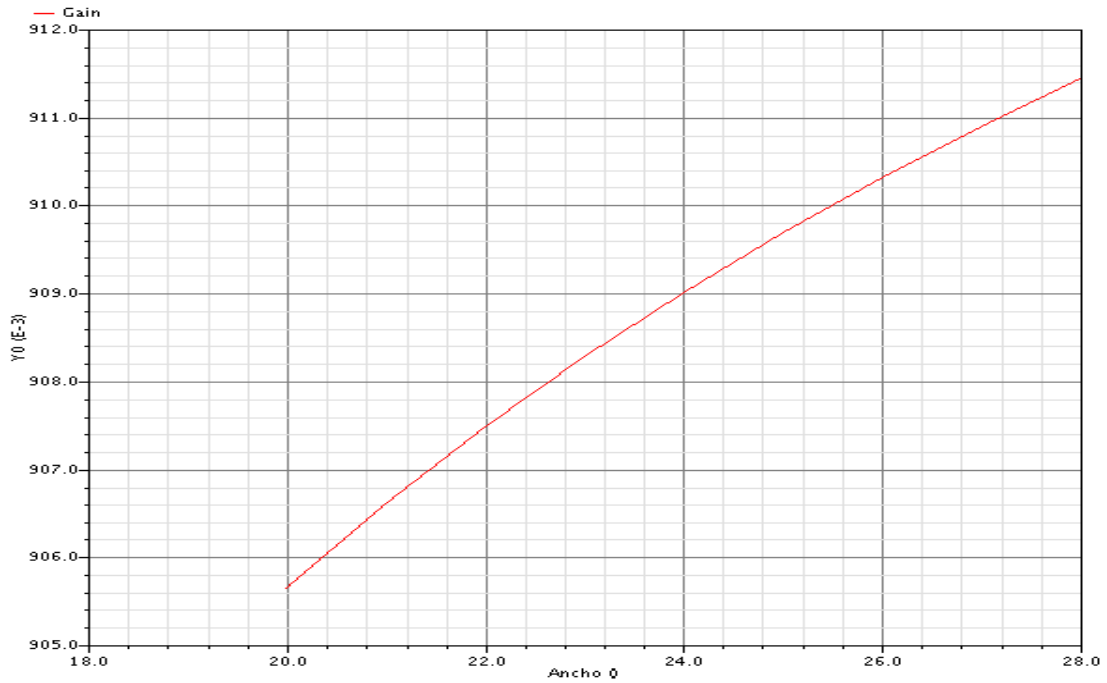


Figure 7: Transistor width sweep from 20 to 28 μm with an increment of 1 μm . Gain vs Width.

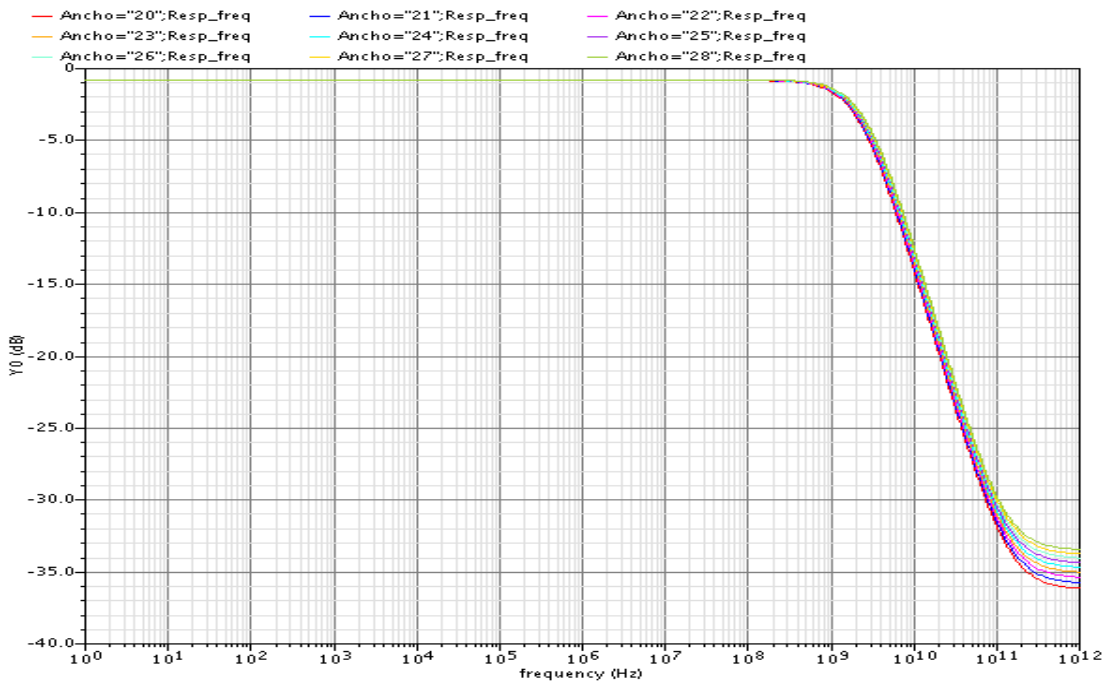


Figure 8: Transistor width sweep from 20 to 28 μm with an increment of 1 μm . Transfer function for each width value.

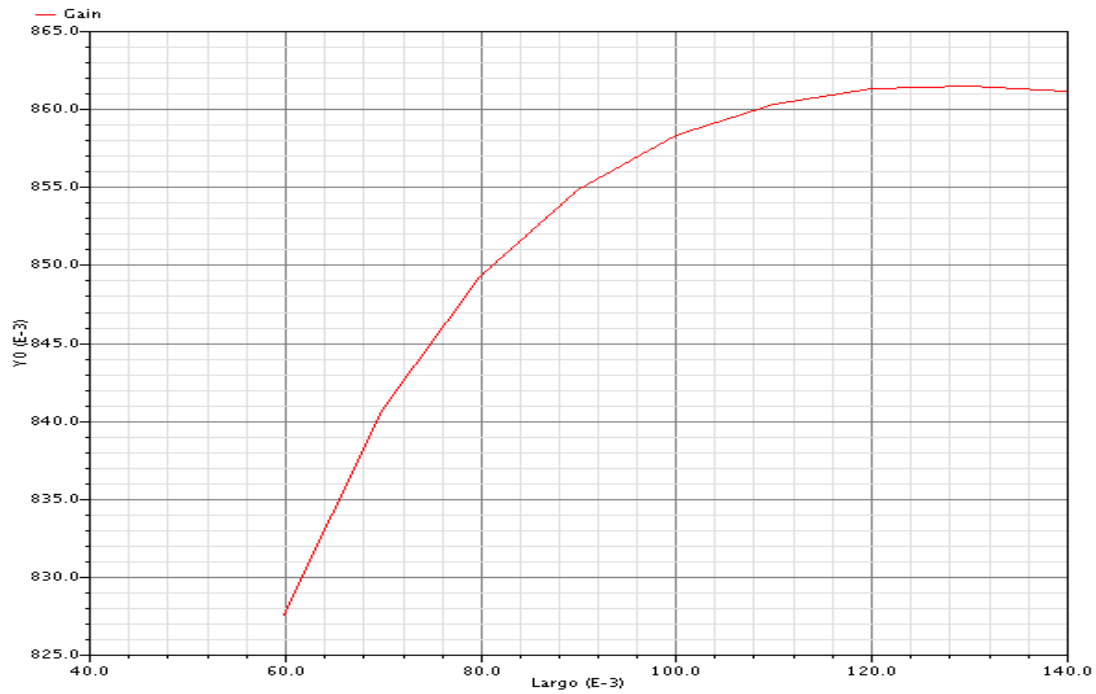


Figure 9: Transistor length sweep from 0.06 to 0.14 μm with an increment of 0.01 μm . Gain vs Length.

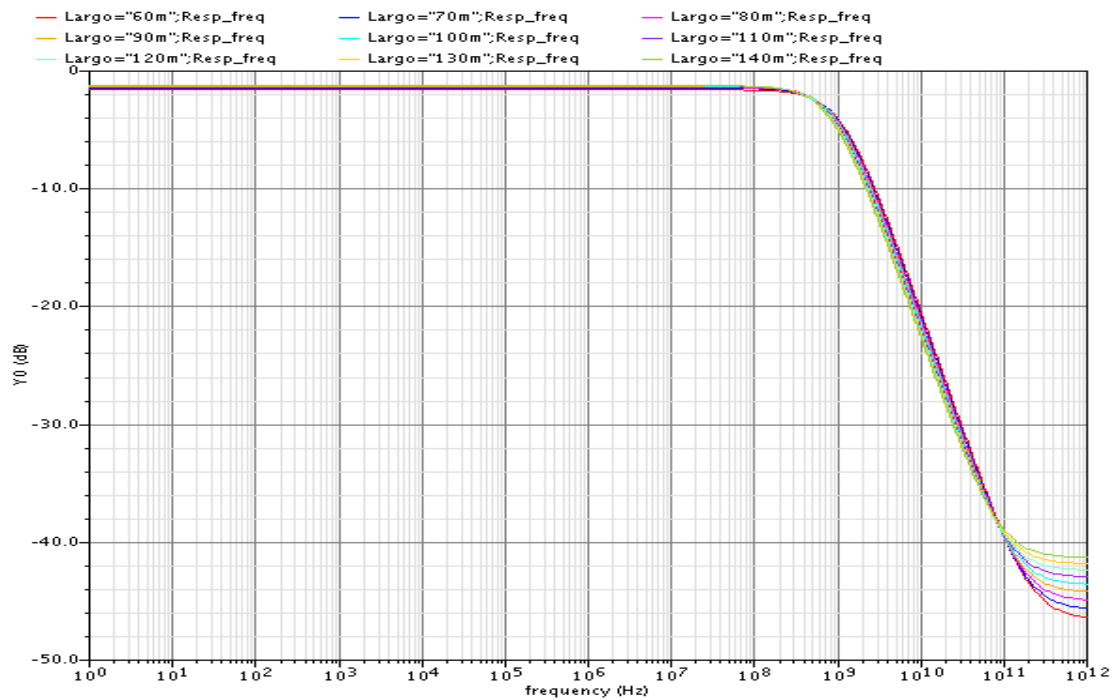


Figure 10: Transistor length sweep from 0.06 to 0.14 μm with an increment of 0.01 μm . Transfer function for each length value.

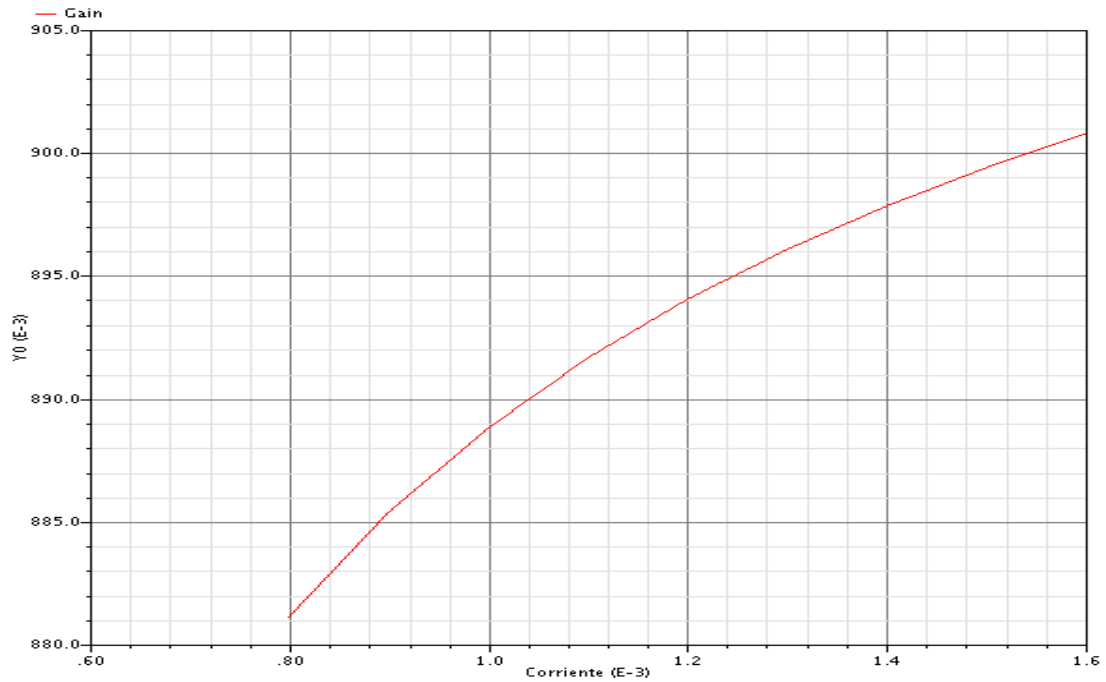


Figure 11: Current sweep from $800 \mu A$ to $1.6 mA$ with an increment of $0.1 mA$ with a transistor width of $26 \mu m$ and length of $0.12 \mu m$. Gain vs Current.

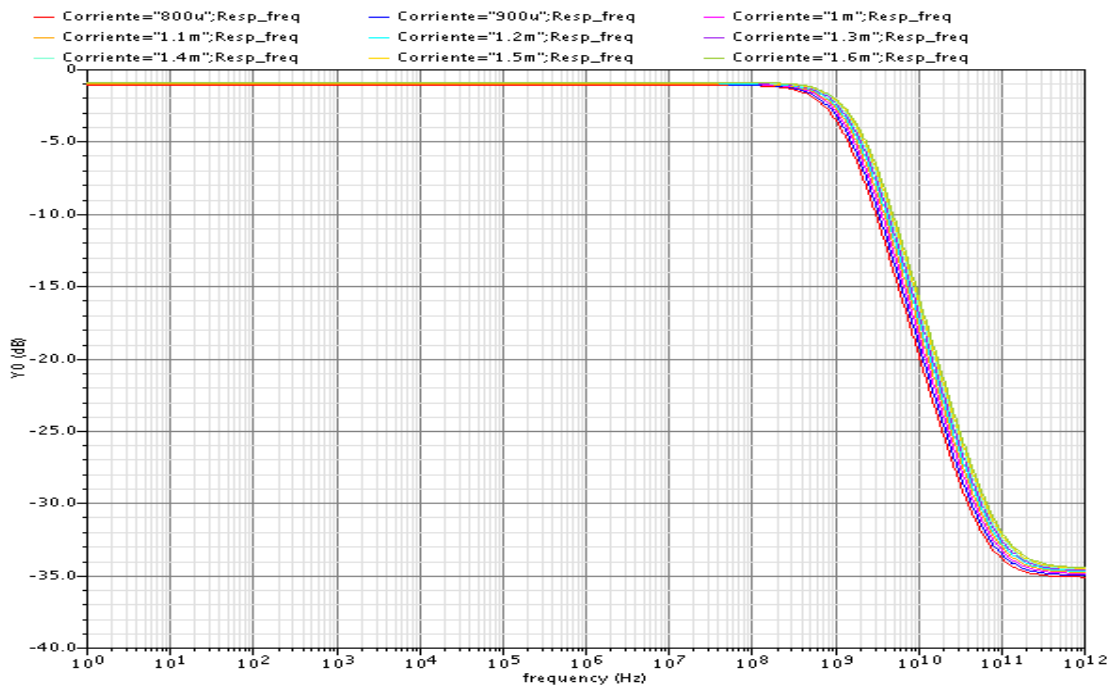


Figure 12: Current sweep from $800 \mu A$ to $1.6 mA$ with an increment of $0.1 mA$ with a transistor width of $26 \mu m$ and length of $0.12 \mu m$. Transfer function for each current value.

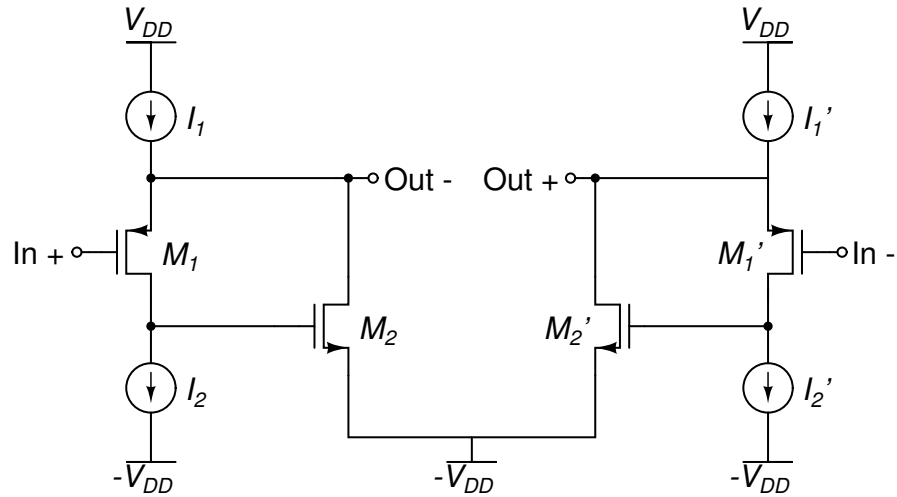


Figure 13: Ideal pMOS super source follower schematic.

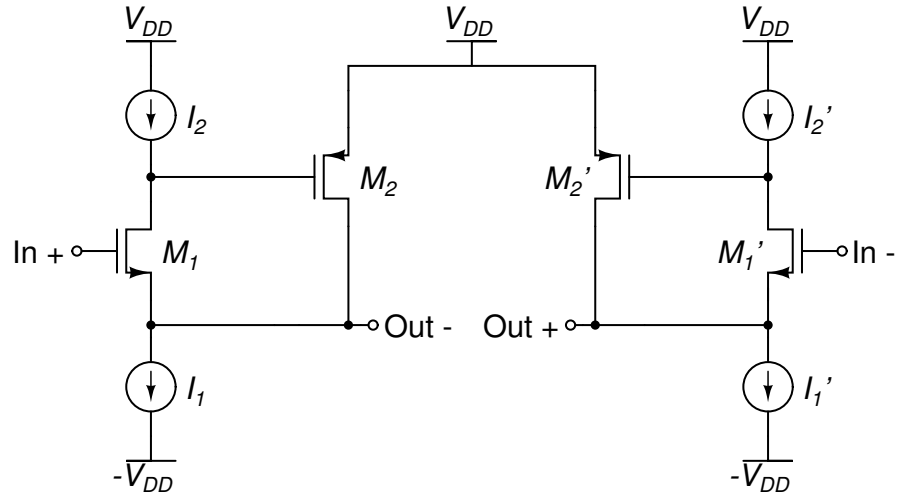


Figure 14: Ideal nMOS super source follower schematic.

the simulations were not as irregular as the pMOS version ones, and the maximum affordable gain was 0.9028 with an approximated bandwidth of 1 GHz. These are the values of the design parameters that were selected to have that gain and bandwidth: $W_1/L_1 = 16/0.2$, $W_2/L_2 = 9/0.2$, $I_1 = 1.5\text{ mA}$, $I_2 = 1.2\text{ mA}$ and a bias voltage of -0.25 V .

4.1.3 Active Element

The filter was chosen to be designed according to the Sallen-Key topology, which means to use biquads, i.e. second order sections, that consist of resistors, capacitors and active elements. In this particular design that is being considered, the active elements were based on the super source follower, but, as it was explained in § 3,

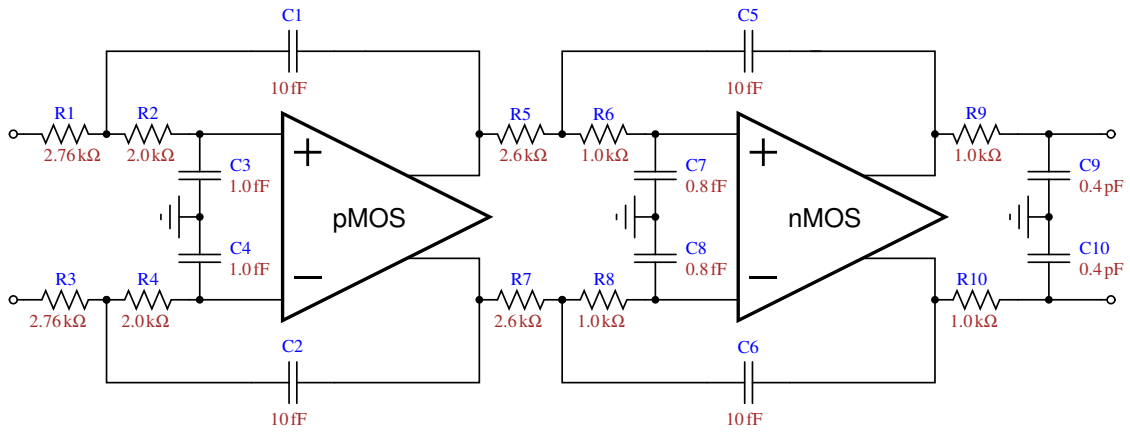


Figure 15: Ideal filter schematic.

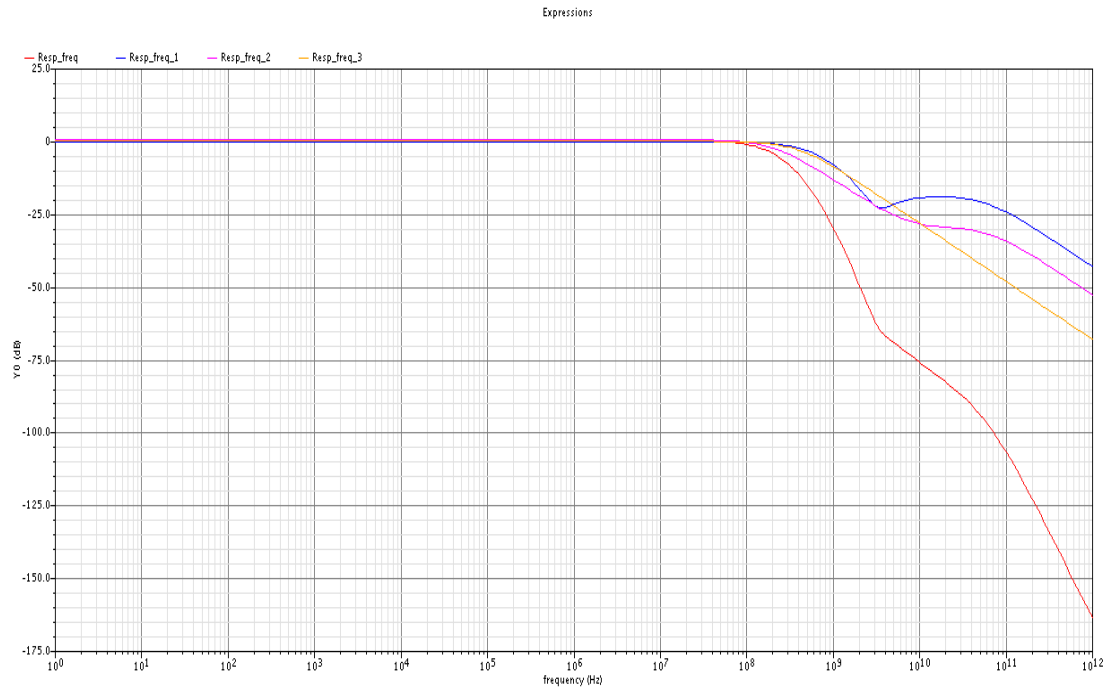


Figure 16: Filter transfer function (Red). Stage 1 transfer function (Blue). Stage 2 transfer function (Pink). Stage 3 transfer function (Yellow).

the gain of the super source follower was going to be always less than unity and that could not be enough to create an stable design. So, a previous gain stage was added to the super source follower in those cases where the gain was not enough.

In this part of the design in which several components were considered ideal, it was only necessary to include the gain stage in the second active element, i.e. the active element with the nMOS version of the super source follower, as the pMOS version had reached a gain of 0.9822 and it was enough to create the first stage of the filter, the one with the lowest Q-factor. Since the nMOS version had achieved a gain of only 0.9028 and it had to implement the stage of the filter with the highest Q-factor, a previous stage with a gain of 1.2 was added to the active element of the second stage of the filter, obtaining an overall gain of 1.083.

4.1.4 Filter

As the gain of the active elements was different to the gain that was assumed in the calculations of § 2.3, the process had to be repeated and new values were obtained for the design parameters. On the one hand, these are the values that were used to implement the first stage of the ideal filter: $\rho = 1.3789$, $\gamma = 0.1$, $R_2 = 2\text{ k}\Omega$ and $C_1 = 10\text{ fF}$. On the other hand, the values that were used in the second stage are the following: $\rho = 2.6246$, $\gamma = 0.083$, $R_2 = 1\text{ k}\Omega$ and $C_1 = 10\text{ fF}$. Finally, the single pole was implemented with a resistor of $1\text{ k}\Omega$ and a capacitor of 0.4 pF . The schematic of the complete ideal filter is shown in Figure 15, the transfer functions of the filter and the intermediate stages are shown in Figure 16.

4.2 Real Design

The ideal filter design was done to prepare this phase of the design flow, the real filter design. In this point, the same process was followed, so the source follower and the super source follower were considered again. However, the ideal current sources were replaced with current mirrors and the ideal gain stages with differential amplifiers. The result of this replacement was a lower gain in all the circuits, which implied to make several readjustments in the design parameters.

4.2.1 Source Follower

The source follower was firstly considered as it was done in the ideal design. The circuit schematic of the real source follower that was analyzed was a fully differential version of the schematic shown in Figure 1. The same simulations that had been done with the ideal source follower were done with the real one, taking into account the result of the previous simulations. As the circuit that was used in this point had some new components, another simulations had to be done, in order to analyze the effect of the transistors that composed the current mirror on the source follower transfer function. Figures 17, 18, 19, 20 21, 22, 23 and 24 show the result of the new simulations, and also, of those that were relevant from the simulations that had been repeated.

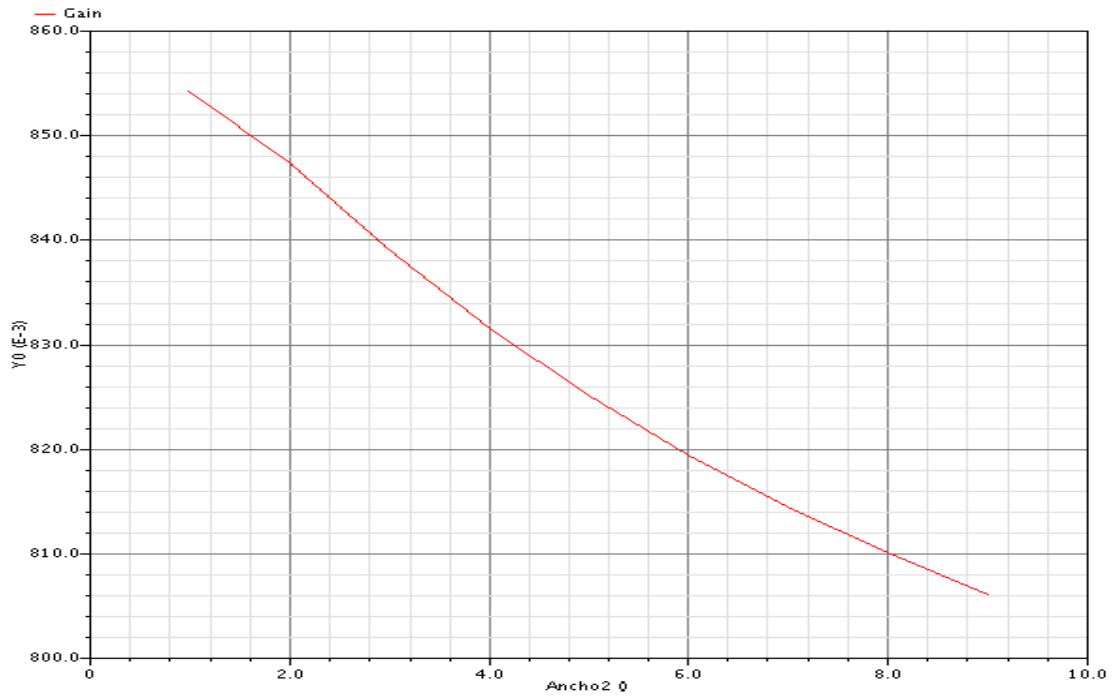


Figure 17: Current mirror transistors width sweep from 1 to 9 μm with an increment of 1 μm . Gain vs Width.

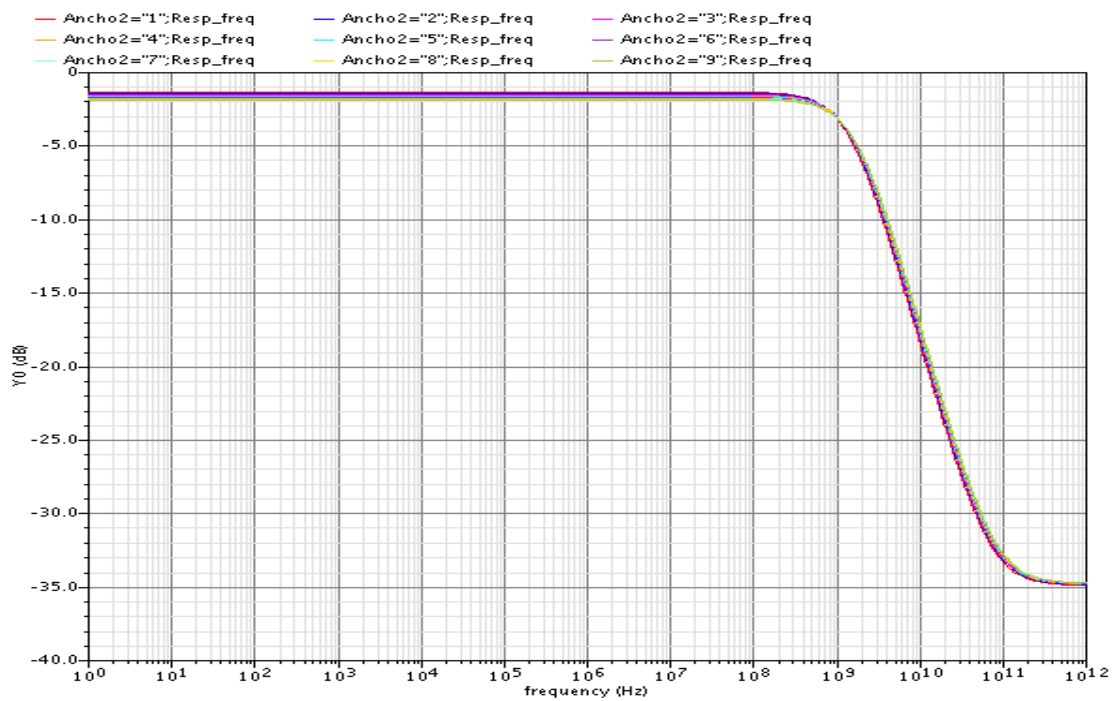


Figure 18: Current mirror transistors width sweep from 1 to 9 μm with an increment of 1 μm . Transfer function for each width value.

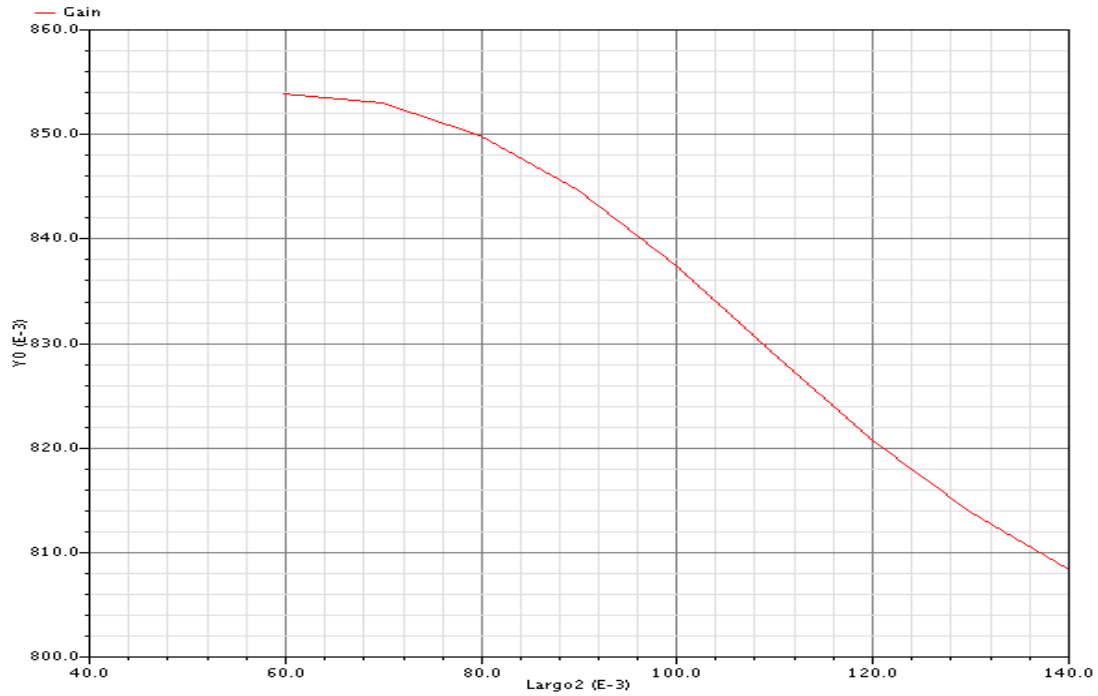


Figure 19: Current mirror transistors length sweep from 0.06 to $0.14 \mu m$ with an increment of $0.01 \mu m$. Gain vs Length.

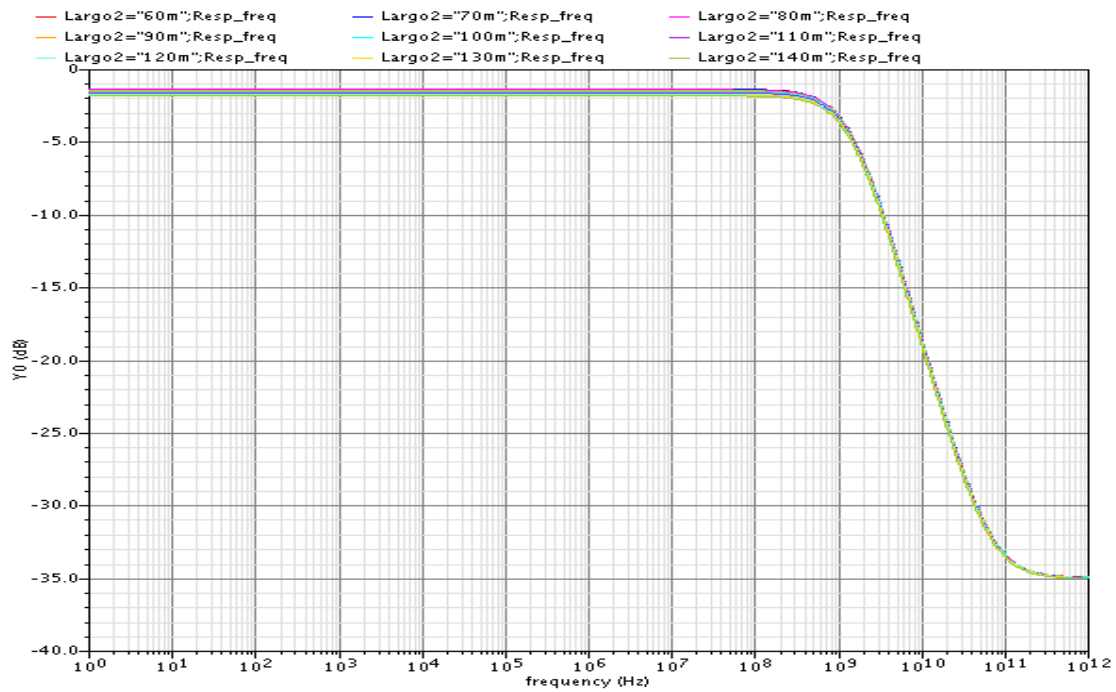


Figure 20: Current mirror transistors length sweep from 0.06 to $0.14 \mu m$ with an increment of $0.01 \mu m$. Transfer function for each length value.

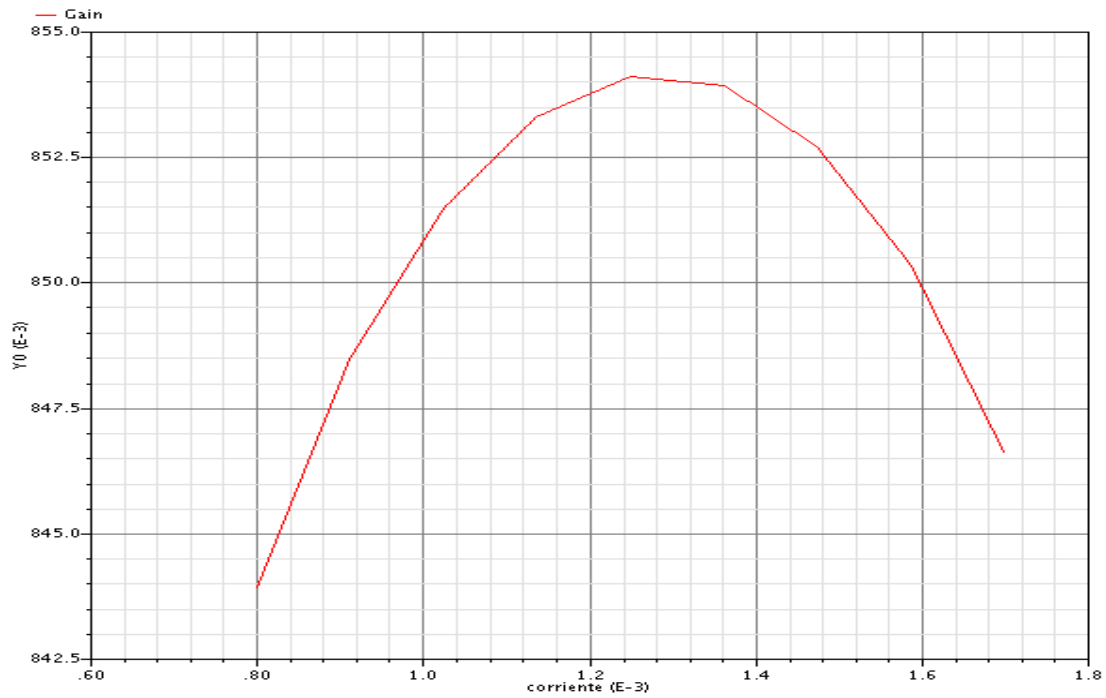


Figure 21: Current sweep from 0.8 to 1.7 mA with an increment of $112.5 \mu A$. Gain vs Current.

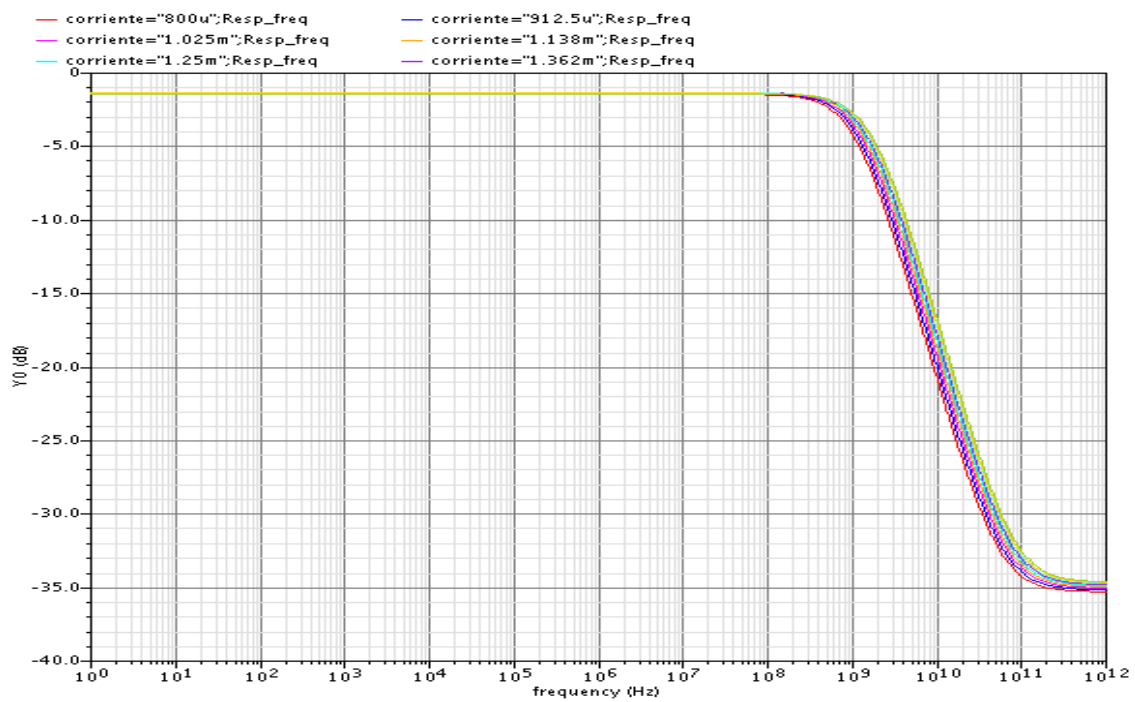


Figure 22: Current sweep from 0.8 to 1.7 mA with an increment of $112.5 \mu A$. Transfer function for each current value.

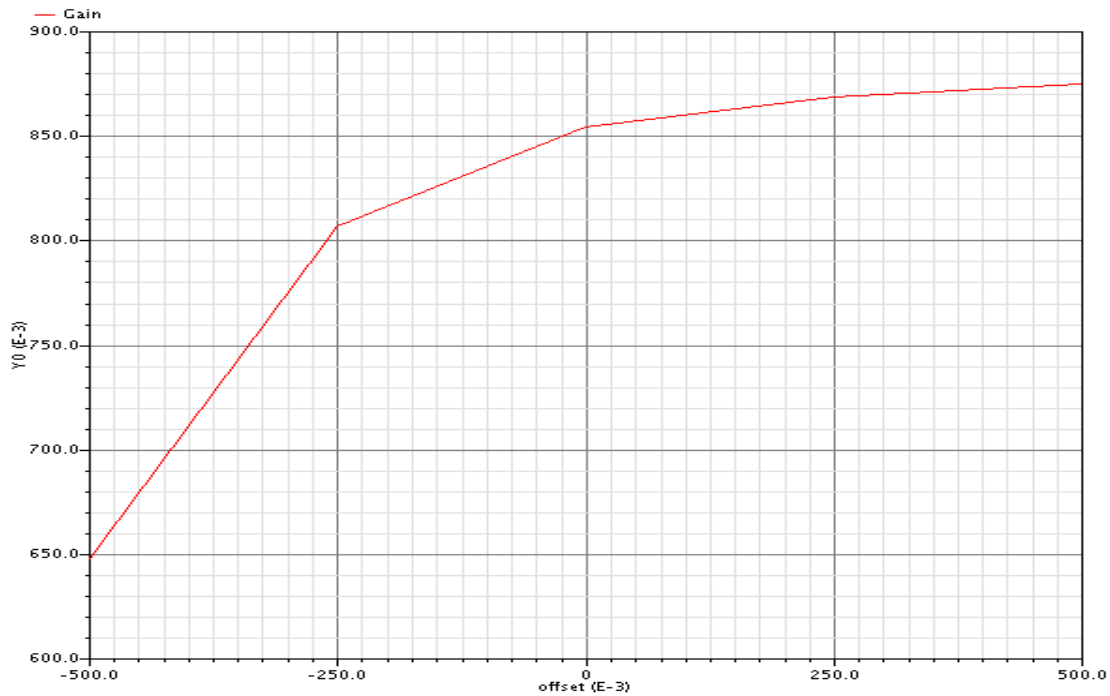


Figure 23: Bias voltage sweep from -0.5 to 0.5 V with an increment of 250 mV. Gain vs Bias voltage.

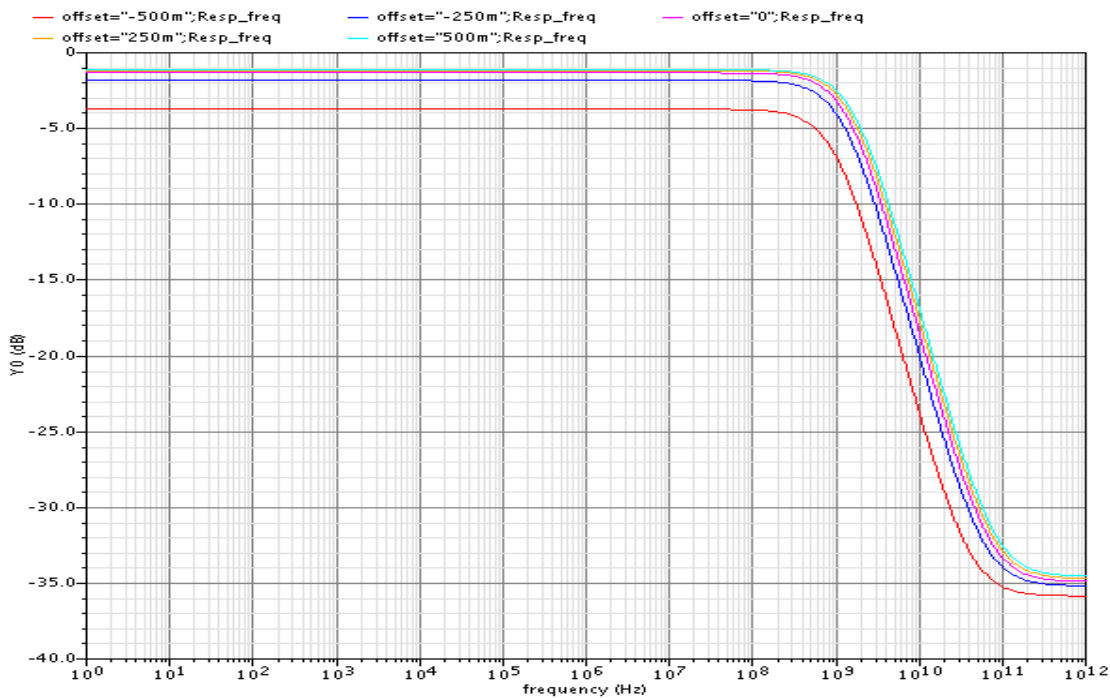


Figure 24: Bias voltage sweep from -0.5 to 0.5 V with an increment of 250 mV. Transfer function for each voltage value.

This results showed that the best choice for the transistors that composed the current mirror was to keep their width and length minimum values. They also revealed that a positive bias voltage was needed to get a gain closer to the maximum achievable value, which had been obtained with the ideal version of the source follower. The result of the simulation with the current sweep showed a different response to that shown in Figure 11, which was obtained with the ideal version of the circuit. As it can be appreciated in the new current response, a current value of about 1.25 mA made the gain to be maximum. A gain of 0.8539 and a bandwidth of approximately 1.2 GHz were selected for the source follower to be included in the filter design. They were achieved with the following values: $W_1/L_1 = 26/0.12$, $W_2/L_2 = 0.9/0.06$, $W_3/L_3 = 0.9/0.06$ and $I = 1.2\text{ mA}$.

4.2.2 Super Source Follower

The circuit schematic of the pMOS version with the ideal current sources replaced with a current mirror is shown in Figure 25. The same simulations that have been done in pMOS version with ideal current sources were also done in this case, in order to check the behavior of the circuit with the new components, and if the sensitivity to the design parameters was still the same. Furthermore, as it was done with the real version of the source follower, new simulations were done to calculate the optimum values for the parameters of the transistors that composed the current mirror.

After these simulations have been done, the only parameter that gave a different response was the current that flowed through the main transistors of the super source follower. On the one hand, a new value of $800\text{ }\mu\text{A}$ was chosen for the current through the M1 transistor in order to get the maximum gain (see Figure 26). On the other hand, a value of 4 was selected for the ratio I_1/I_2 , i.e the current through the M1 transistor divided by the current through M2, to minimize the peak that appeared in the transfer function of the new super source follower circuit, before the cut-off frequency, without getting a gain too low (see Figures 27 and 28). The size of the transistors that composed the two current mirrors were also chosen to minimize that peak. A length of $0.12\text{ }\mu\text{m}$ and a width of $0.72\text{ }\mu\text{m}$ (six times the length) were selected for M6, and a length of $0.12\text{ }\mu\text{m}$ and a width of $2.88\text{ }\mu\text{m}$ for M3, M4 and M5 in order to keep the current ratio of 4. Finally, these width values were multiplied by a factor of 3 to achieve a greater gain, as shown in Figures 29 and 30.

Finally, the selected values for the parameters to achieve a gain of 0.876 with a bandwidth of approximately 3 GHz and a peak of 2 dB at a frequency of 1.9 GHz were: $W_1/L_1 = 16/0.12$, $W_2/L_2 = 12/0.12$, $W_3/L_3 = W_4/L_4 = W_5/L_5 = 8.64/0.12$, $W_6/L_6 = 2.16/0.12$, $I = 800\text{ }\mu\text{A}$ and a bias voltage of 250 mV . The transfer function of the ideal version of the pMOS super source follower is compared with the transfer function of the real one in Figure 31.

The same simulations that have been done with the pMOS version of the super source follower were also done with the nMOS version, as it was necessary to implement the second stage of the filter. Some of the results of these simulations were

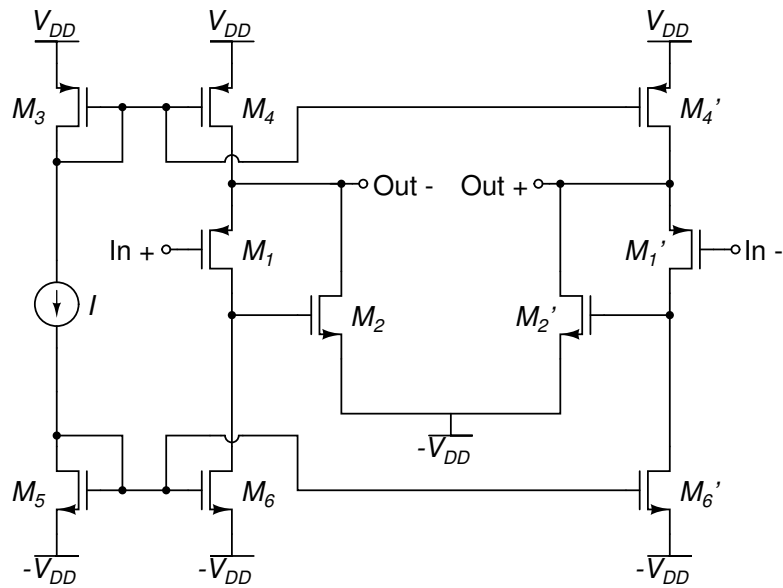


Figure 25: pMOS super source follower schematic.

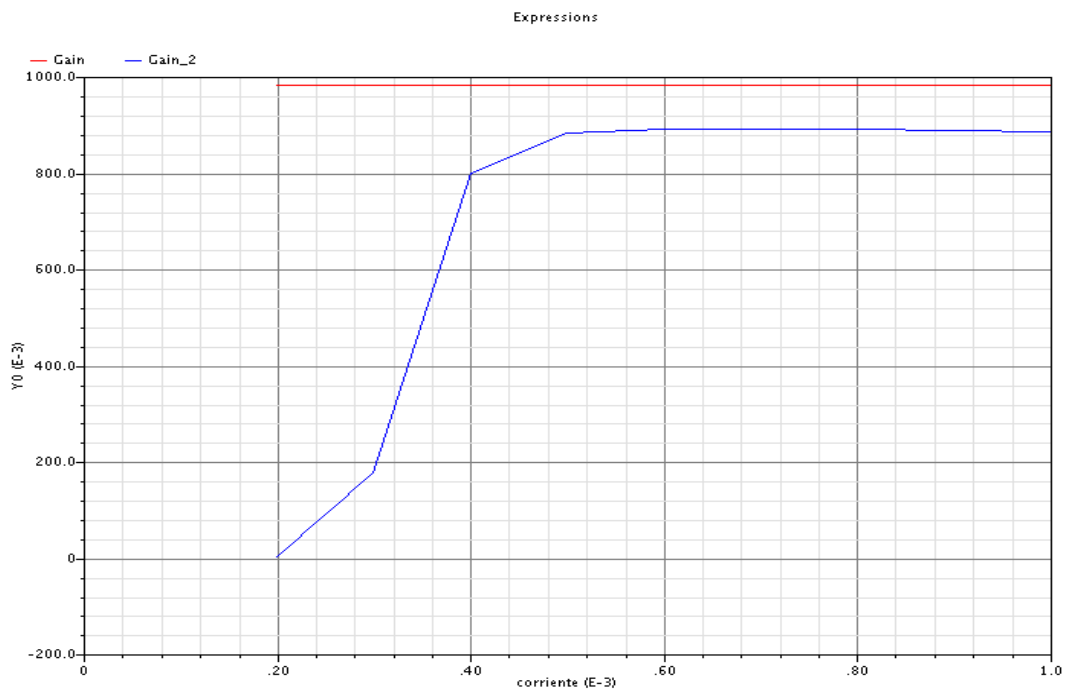


Figure 26: Current sweep from 0.2 to 1 mA with an increment of 0.1 mA. The gain of the ideal version of the pMOS super source follower is represented in red, as a point of reference, and the gain of the real version in blue.

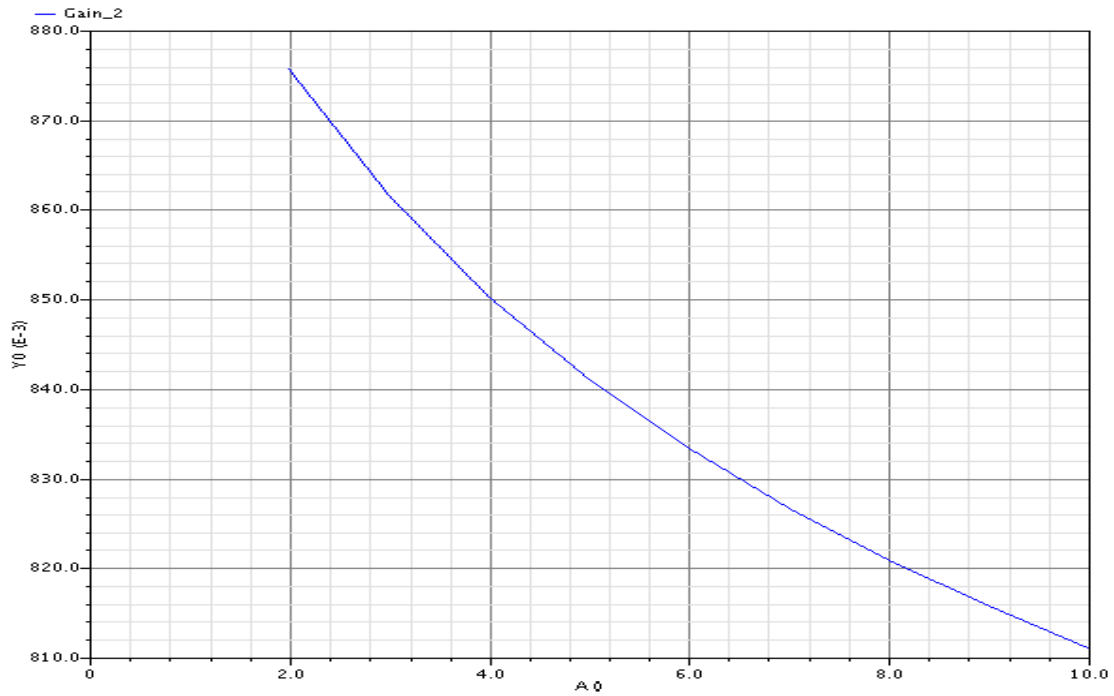


Figure 27: Current ratio sweep from 2 to 10 with an increment of 1. Gain vs Current Ratio.

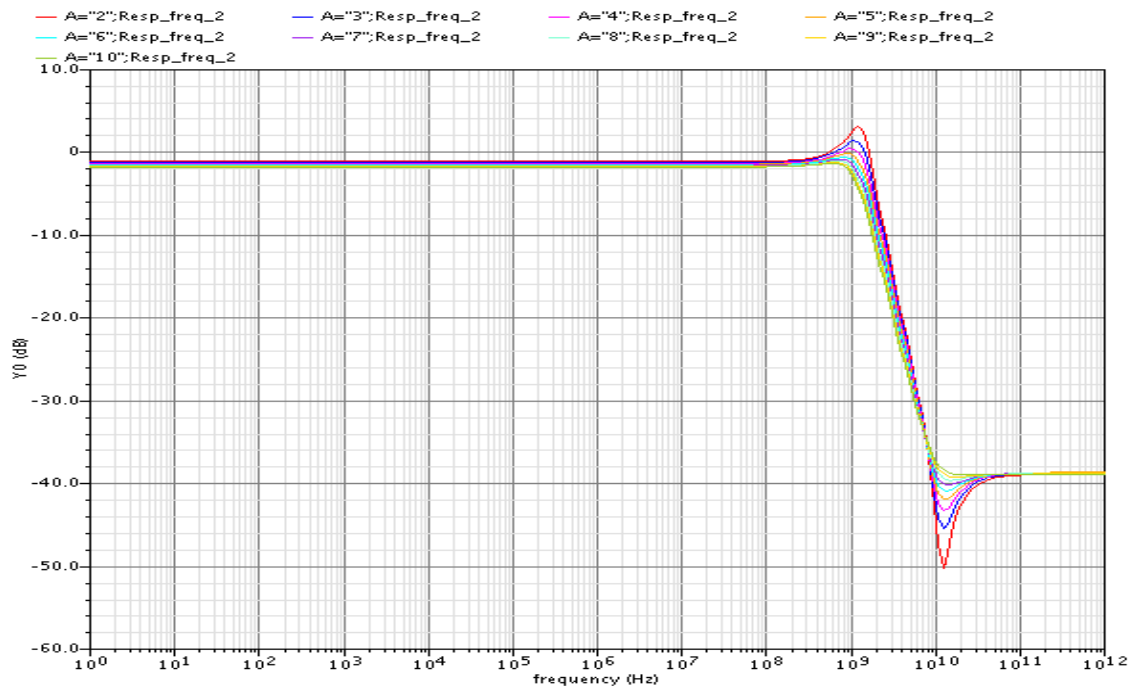


Figure 28: Current ratio sweep from 2 to 10 with an increment of 1. Transfer function for each current ratio value.

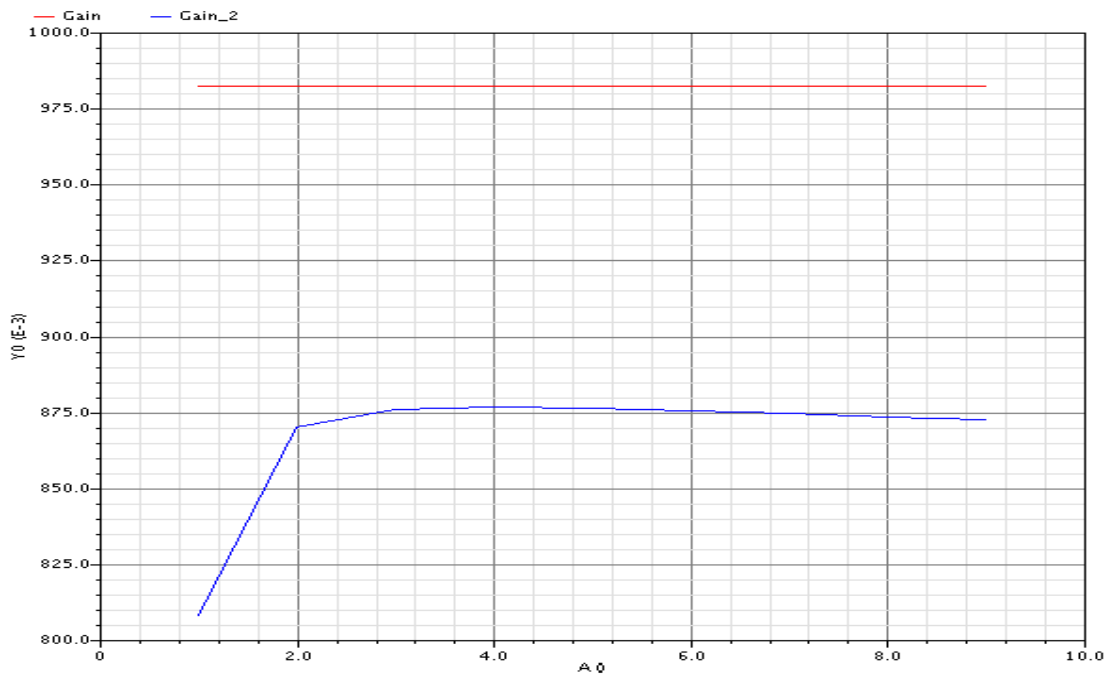


Figure 29: Width coefficient sweep from 1 to 9 with an increment of 1. Gain vs Width coefficient is represented in blue, the gain of the ideal version is represented in red.

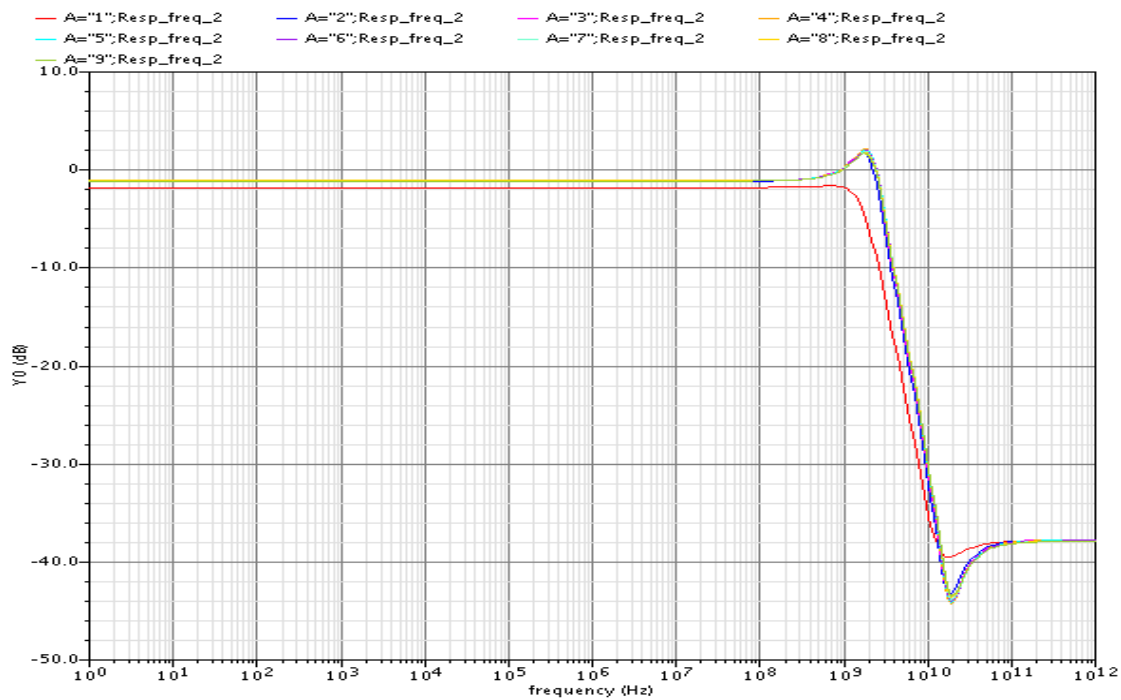


Figure 30: Width coefficient sweep from 1 to 9 with an increment of 1. Transfer function for each width coefficient.

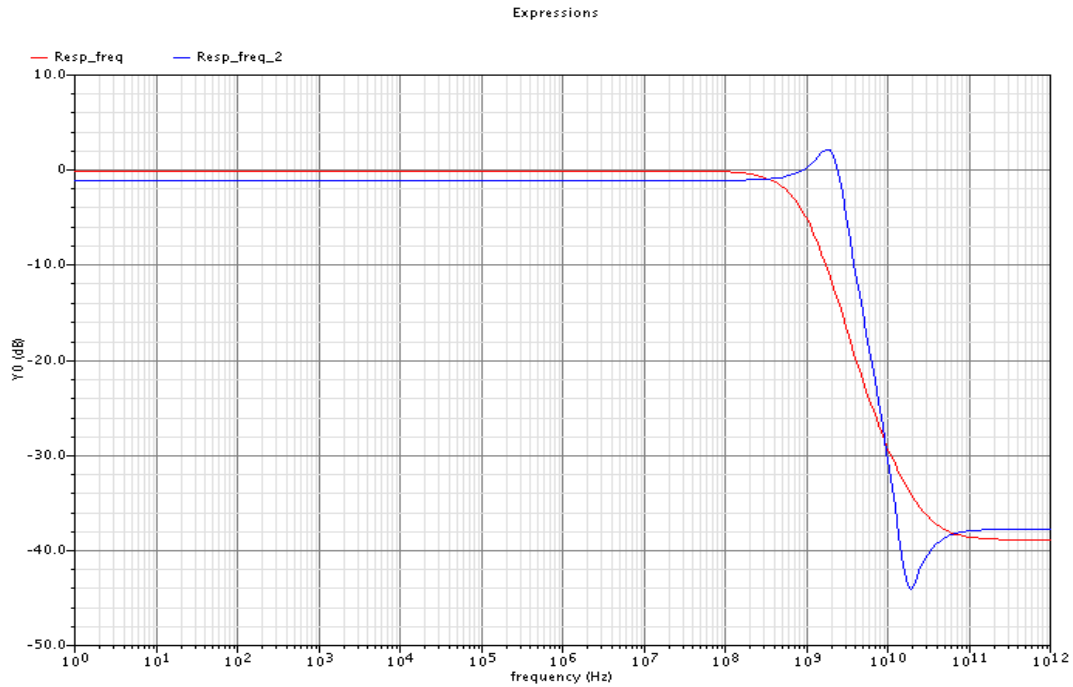


Figure 31: Transfer function of the ideal version of the pMOS super source follower (Red). Transfer function of the real version (Blue).

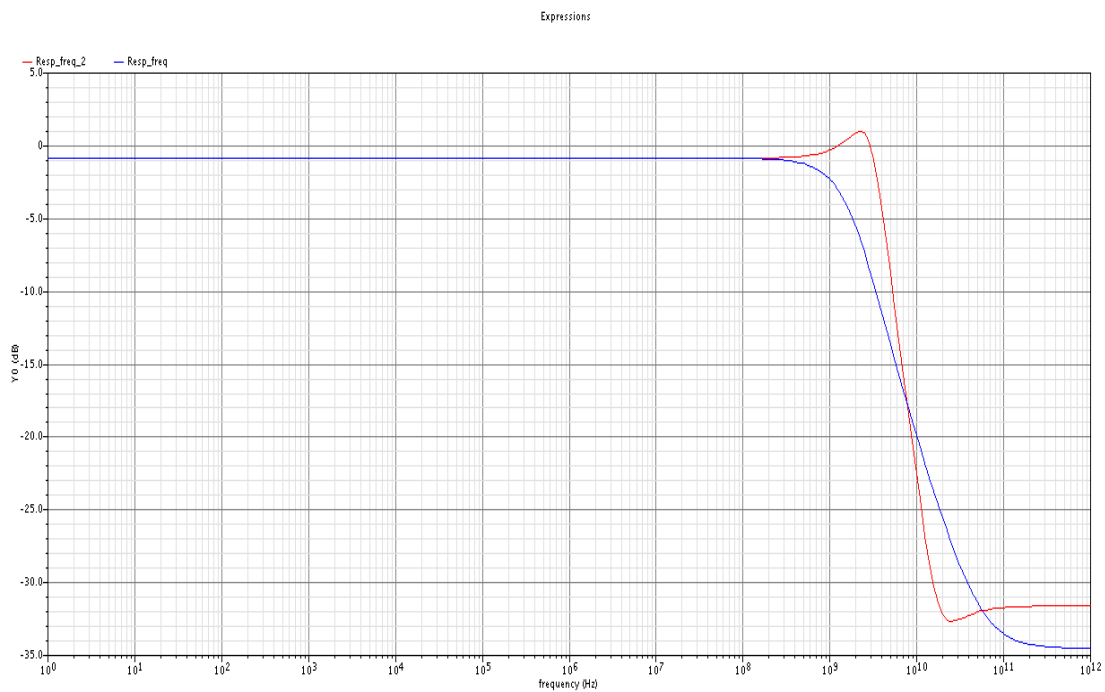


Figure 32: Transfer function of the real version of the nMOS super source follower (Red). Transfer function of the ideal one (Blue).

similar to those extracted from the simulations with the ideal version of the nMOS super source follower. However, despite the fact the response to the sweep of certain parameters was the same, the gain was lower and the size of the main transistors had to be increased. In other cases, the result differed from that gotten with the ideal version of the circuit so the optimum value was different. The maximum gain had been achieved with a length value of $0.2 \mu m$ for the main transistors in the ideal design, but it changed to $0.15 \mu m$ in the real one as it is shown in Figures 33 and 34. The size of the M3, M5 and M6 transistors was taken from the design of the previous pMOS version, while the width of the M4 was chosen from a simulation result in order to minimize the high frequency peak and get a gain as close to the ideal one as possible (see Figures 35 and 36).

The final design presented the following values: $W_1/L_1 = 28/0.15$, $W_2/L_2 = 28/0.15$, $W_3/L_3 = W_5/L_5 = W_6/L_6 = 2.88/0.12$, $W_4/L_4 = 1.5/0.12$, $I = 1.2 mA$ and a bias voltage of $-250 mV$. A gain of 0.9034 with a bandwidth of approximately 4 GHz and a peak of 1 dB at a frequency of 2.29 GHz was achieved with these values. The transfer function of the ideal version of the nMOS super source follower is compared with the transfer function of the real one in Figure 32.

After having simulated the source follower and the super source follower, and having designed both of them, the comparison can be done. As the source follower is actually an nMOS source follower, the comparison has to be done with the nMOS version of the super source follower. The main difference between these circuits is the high frequency peak that appears in the super source follower and not in the normal source follower. This peak seems to be caused by the feedback loop that exists only in the super source follower and that may become resonant at the frequency where the peak shows up. Another fact is that it appears when the gain of the super source follower is close to the maximum achievable gain, as Figures 35 and 36 show clearly for the real version of the nMOS super source follower. As the peak is at a frequency far enough from the desired bandwidth it can be acceptable, but as it can also affect the linearity of the filter, it has to be minimized.

Another aspect to be compared between these two circuits is the gain that they can achieve. On the one hand, if the ideal design is considered, the source follower could have a greater gain than the nMOS super source follower, as the maximum gain for the super source follower was fixed to 0.9028 and this value was exceeded by the source follower in Figure 7. This would be in keeping with the theoretical behavior explained in § 2.2. On the other hand, if the real design is considered, the super source follower was able to reach a gain of 0.9034, while the source follower gain stopped at a top value of 0.8539. However, it also has to be considered that the super source follower is implemented with a higher number of transistors, which means a higher power consumption, and if the high frequency peak was not acceptable, the gain of the super source follower would decrease and it would be similar to the source follower gain.

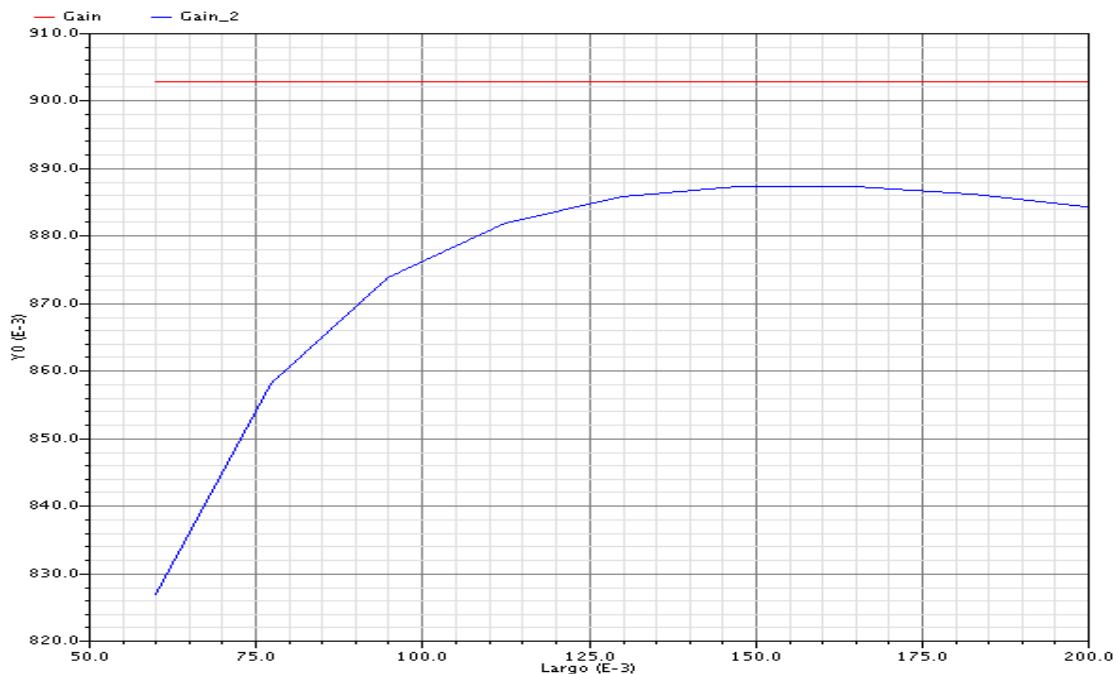


Figure 33: Main transistors length sweep from 0.06 to $0.2 \mu m$ with an increment of $0.0175 \mu m$. Gain vs Length is represented in blue and the gain obtained with the ideal version is represented in red (Left).

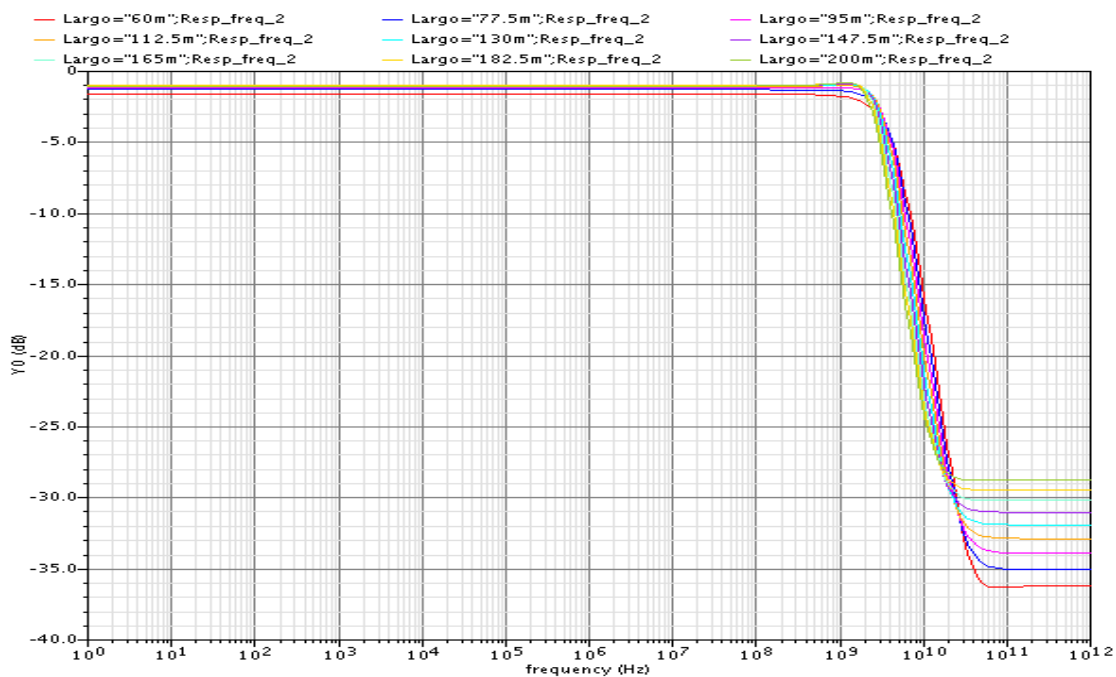


Figure 34: Main transistors length sweep from 0.06 to $0.2 \mu m$ with an increment of $0.0175 \mu m$. Transfer function for each length value.

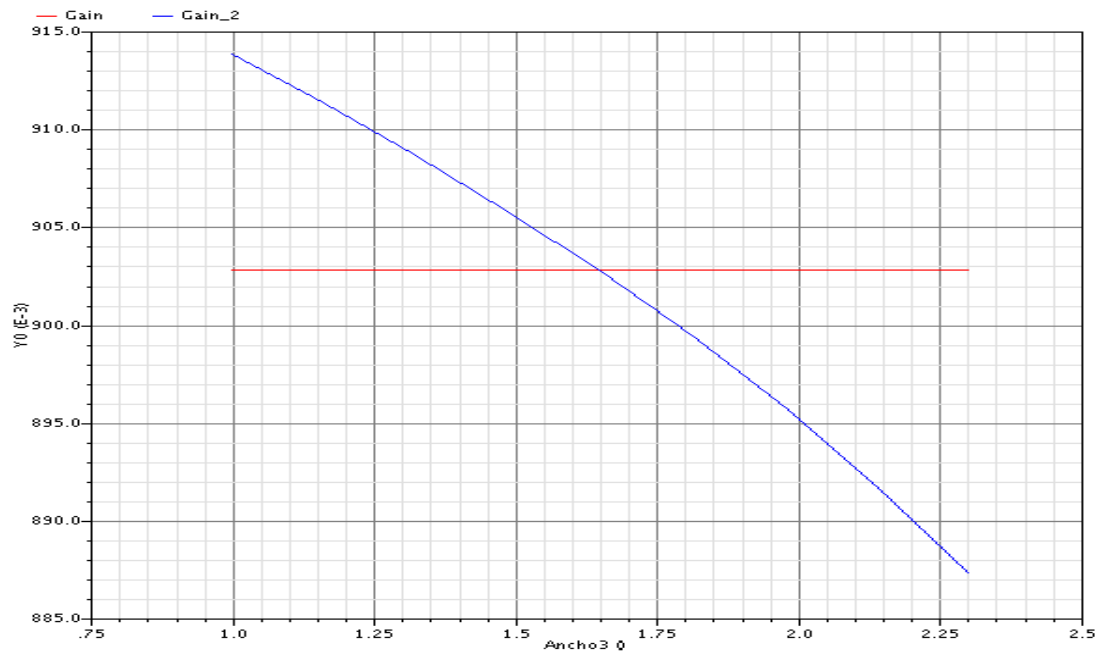


Figure 35: M4 transistor width sweep from 1 to 2.3 μm with an increment of 0.163 μm . Gain vs Width is represented in blue and the gain obtained with the ideal version is represented in red (Left).

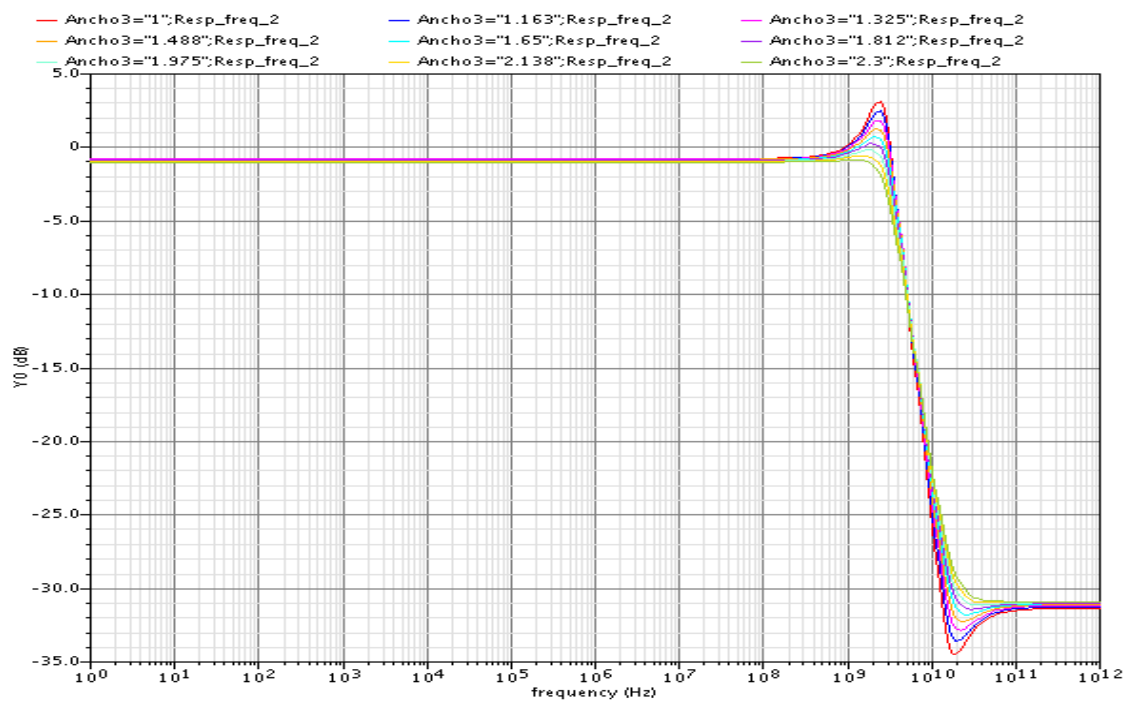


Figure 36: M4 transistor width sweep from 1 to 2.3 μm with an increment of 0.163 μm . Transfer function for each width value.

4.2.3 Active Elements

The filter had to be designed following the Sallen-Key topology, so an active element was included in the biquads that composed each of the filter stages. As it was explained in the introduction, these active elements were going to be based on the super source follower, and they were also going to be compared with the normal source follower. Both versions of the super source follower and the normal source follower had been previously designed, and, at this point, the active elements had to be created in order to get the desired gain so the filter could be implemented without using extremely low values for the capacitors and resistors, or large component ratios that could have meant to obtain an unstable filter.

In § 4.1.3 the active elements were designed by using ideal gain stages to get the desired gain. Furthermore, as the super source followers had been implemented with ideal current sources, the gain achieved by themselves was enough in the first filter stage and the previous gain stage was not needed in both stages. However, this is not the situation in the real implementation of the super source follower, and then, the active elements. Here, both filter sections needed the gain stage: the first one to get a gain close to unity, and the second one to reach a gain a little higher than unity, because of the large value of the Q-factor that is needed in the second filter stage. A positive common mode input had been assumed in the first stage of the filter and, for that reason, the first active element had to be implemented by using the pMOS version of the super source follower, as a positive common mode input defined a better bias point for that circuit. As the common mode output of the first filter stage was -350 mV , the second active element had to be implemented with the nMOS version of the circuit. The circuit schematic of the complete active element with the pMOS version of the super source follower is shown in Figure 37, while the active element with the nMOS version is shown in Figure 38.

The gain stage was implemented with a fully differential amplifier that employed diode-connected transistors for biasing the main transistors. As the size of the diode-connected transistors was fixed, and the length of the main transistors as well, the gain of the amplifier was controlled with the M7 transistor width. The first active element was created to have a gain of 1.011 by selecting a width of $2.06\text{ }\mu\text{m}$ (see Figures 39 and 40), as the pMOS super source follower achieved a gain of 0.8797 in the active element, and a gain of 1.149 was needed for the differential amplifier in order to get the desired overall gain. The complete description of the design parameters is the following: $I_2 = 100\text{ }\mu\text{A}$, $W_7/L_7 = 2.06/0.06$ and $W_8/L_8 = W_9/L_9 = W_{10}/L_{10} = 0.9/0.06$. A bandwidth of approximately 3 GHz with a peak of 7.6 dB at a frequency of 1.9 GHz was obtained with these values.

The nMOS super source follower got a gain of 0.8883 when it was put together with the differential amplifier in the second active element. That made to select a gain of 1.25 in the differential amplifier to obtain the overall gain of 1.11 (see Figures 41 and 42). The values that were chosen to fulfill these requirements were: $I_2 = 100\text{ }\mu\text{A}$, $W_7/L_7 = 4/0.06$ and $W_8/L_8 = W_9/L_9 = W_{10}/L_{10} = 0.9/0.06$. The bandwidth of the second active element was the same than the obtained with the first active element, and the peak also appeared at the same frequency, but in this

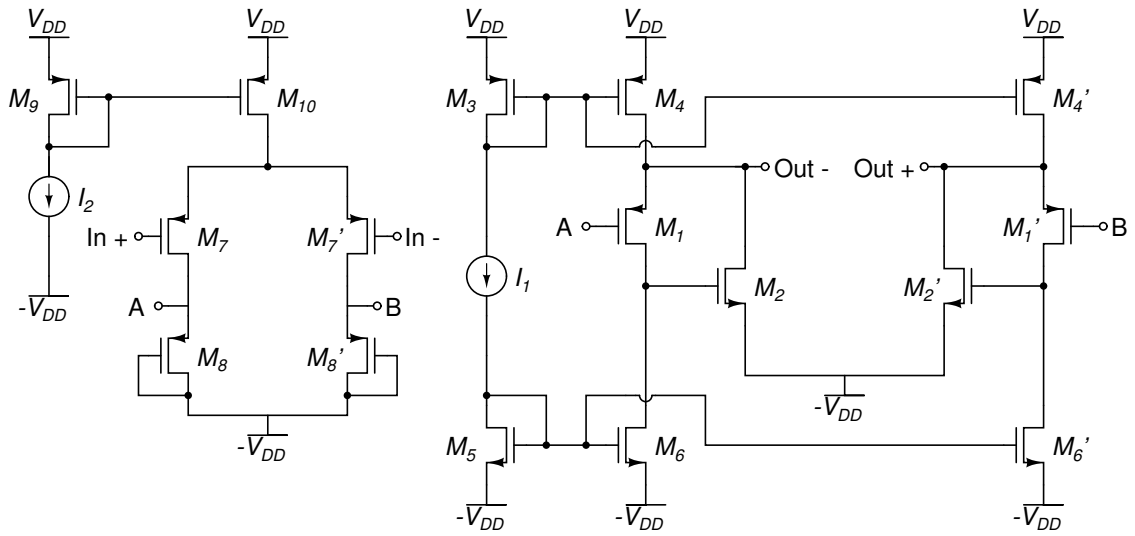


Figure 37: Circuit schematic of the pMOS version of the complete active element.

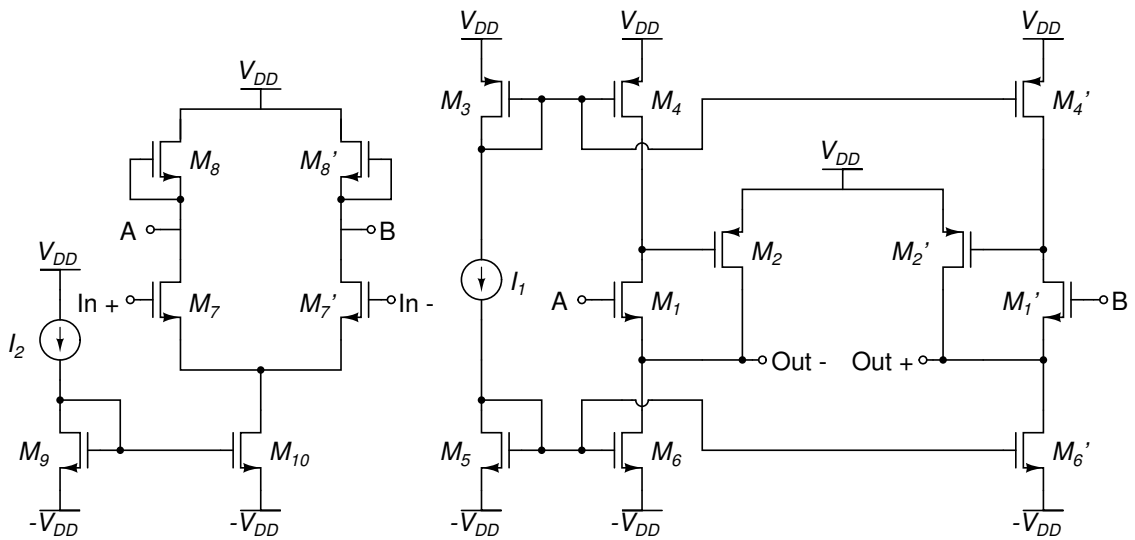


Figure 38: Circuit schematic of the nMOS version of the complete active element.

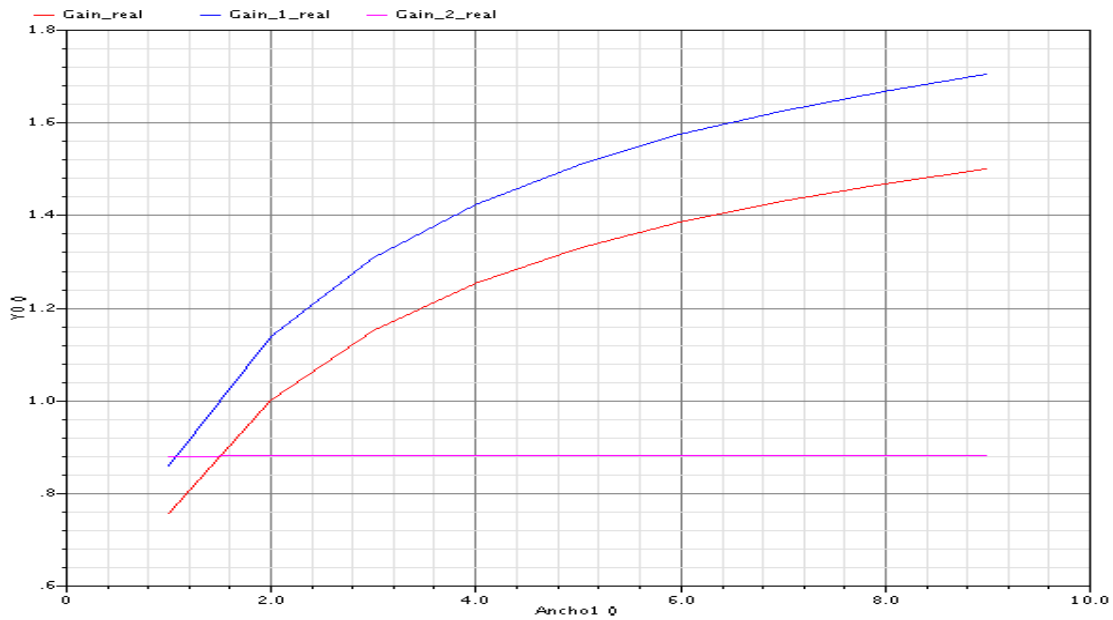


Figure 39: M7 transistor width sweep from 1 to 9 μm with an increment of 1 μm . Gain vs Width is represented in red, Gain 1 vs Width in blue and Gain 2 vs Width in pink, where Gain is the overall gain of the active element, Gain 1 is the gain of the differential amplifier and Gain 2 is the gain of the pMOS super source follower.

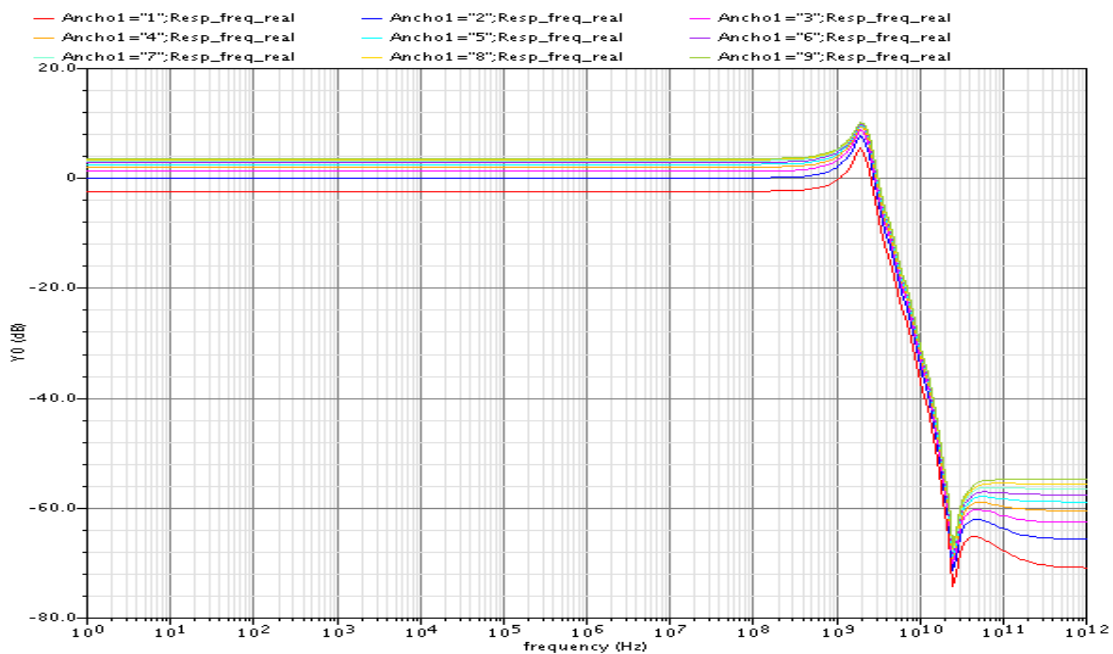


Figure 40: M7 transistor width sweep from 1 to 9 μm with an increment of 1 μm . Transfer function for each width value.

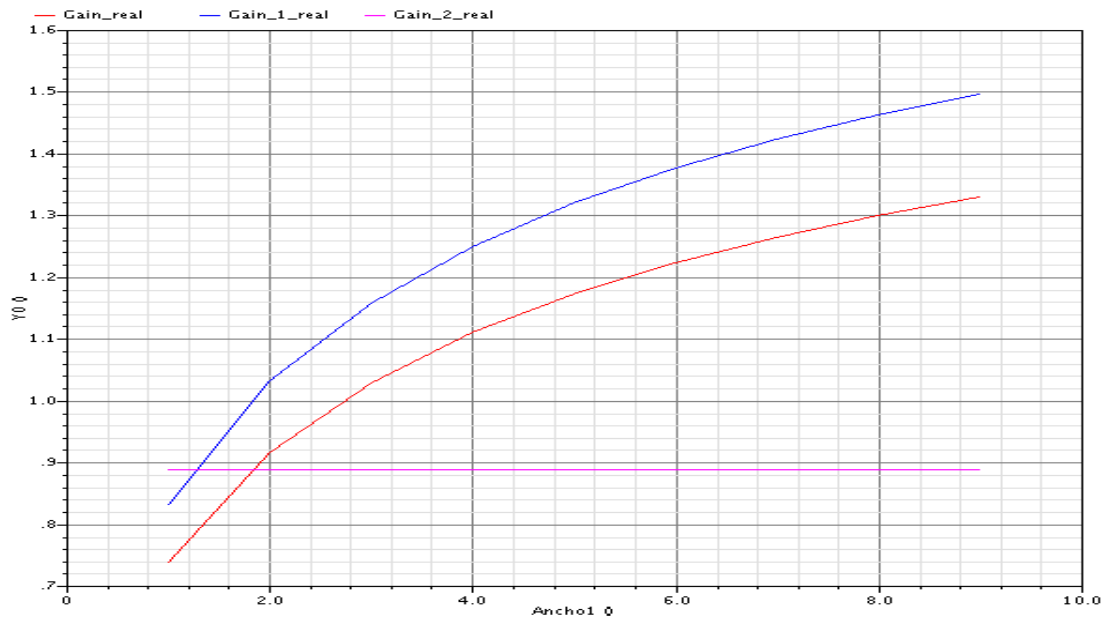


Figure 41: M7 transistor width sweep from 1 to 9 μm with an increment of 1 μm . Gain vs Width is represented in red, Gain 1 vs Width in blue and Gain 2 vs Width in pink, where Gain is the overall gain of the active element, Gain 1 is the gain of the differential amplifier and Gain 2 is the gain of the nMOS super source follower.

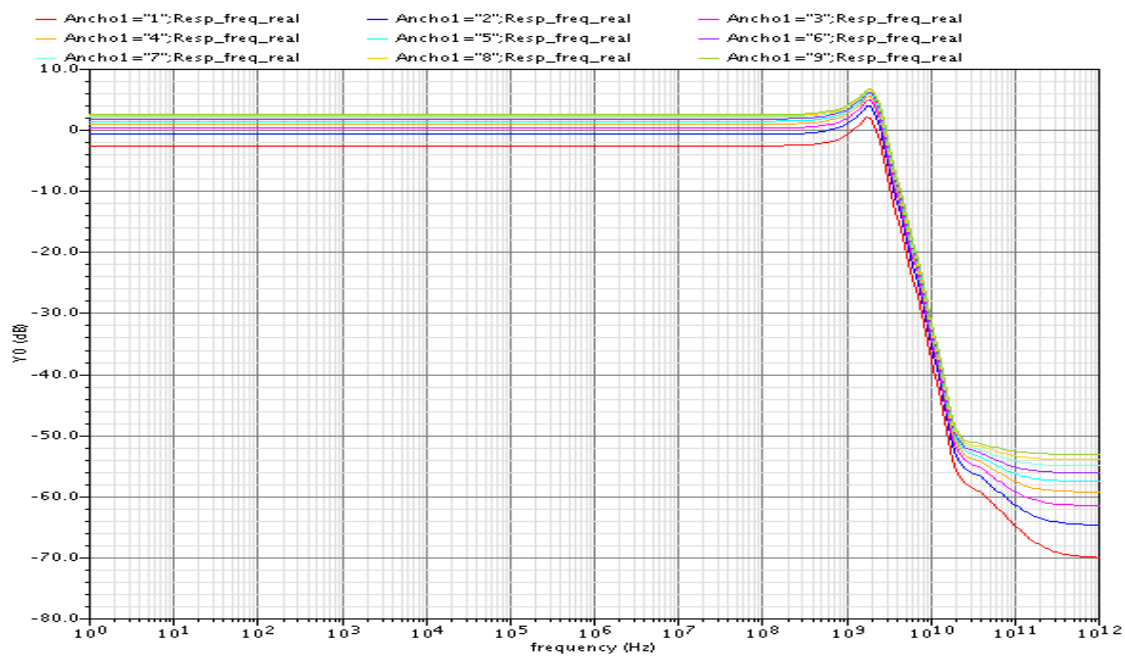


Figure 42: M7 transistor width sweep from 1 to 9 μm with an increment of 1 μm . Transfer function for each width value.

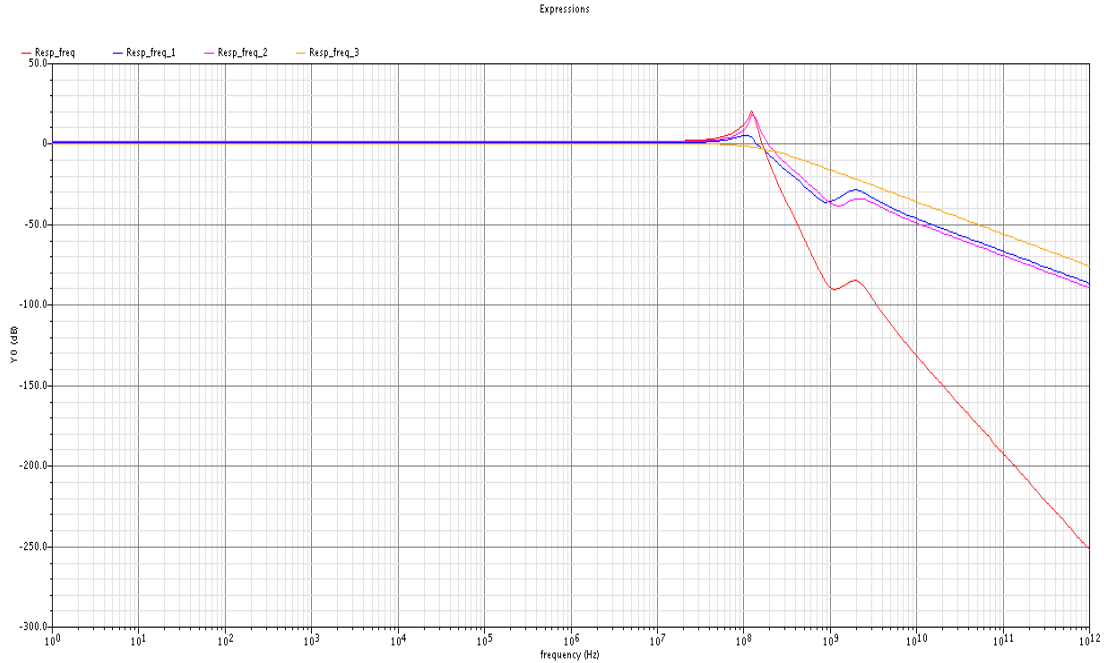


Figure 43: Chebyshev filter transfer function (Red). Stage 1 transfer function (Blue). Stage 2 transfer function (Pink). Stage 3 transfer function (Yellow).

case with a value of 5.46 dB.

4.2.4 Chebyshev Filter

The final design of this thesis had to be a 5th order Chebyshev-type filter implemented by following the Sallen-Key topology. After having designed all the previous steps, it only remained to put the active elements together with the RC networks to create the Sallen-Key biquads, and to put these biquads together with the single RC pole to obtain the final filter. As the gain of the active elements was adapted according to the Q-factor of each filter stage, the gain of the first active element was different to the gain of the second active element, so the values of the passive components had to be redesigned following the process described in § 2.3.

On the one hand, the first filter stage was implemented by using the following values: $\rho = 0.5648$, $\gamma = 0.125$, $R_2 = 5.5 \text{ k}\Omega$ and $C_1 = 100 \text{ fF}$. On the other hand, the values that were used in the second filter stage were: $\rho = 2.1249$, $\gamma = 0.1$, $R_2 = 2170 \Omega$ and $C_1 = 100 \text{ fF}$. Finally, the single pole was implemented with a resistor of $2.5 \text{ k}\Omega$ and a capacitor of 0.4 pF . The transfer functions of the filter and the intermediate stages are shown in Figure 43.

As it can be appreciated, the transfer functions of the first and the second filter stage show a peak, similar to that which had appeared in the super source follower transfer function, and also, in the active element transfer function. As it can also be observed, the peak of the second filter stage is greater than the peak of the first

FILTER ORDER	Stage 1		Stage 2		Stage 3	
	FSF	Q	FSF	Q	FSF	Q
2	1.000	0.7071				
3	1.000	1.0000	1.000			
4	1.000	0.5412	1.000	1.3065		
5	1.000	0.6180	1.000	1.6181	1.000	
6	1.000	0.5177	1.000	0.7071	1.000	1.9320

Table 2: Butterworth Filter Table [4]

one. This happens because the Q-factor of the first stage (1.3988) is lower than the Q-factor of the second one (5.5538), so, the higher the Q-factor the larger the peak. The reason for that peak is the tendency of the active RC networks, which are employed in the Sallen-Key biquads, to become oscillators. Furthermore, this tendency is more prevalent when the value of d is small [2]. The normalized value of the peak is given by the expression (15), while the frequency where this peak appears is given by (16). Both expressions were extracted from [2].

$$\frac{2}{d\sqrt{4-d^2}} \quad (15)$$

$$\frac{\omega_o\sqrt{2-d^2}}{\sqrt{2}} \quad (16)$$

Using (15) and denormalizing the results, the theoretical peak value for the first stage of the Chebyshev filter would be 3.6038 dB, while the peak value for the second stage would be 15.8179 dB. Figure 43 reveals that the practical peak values are quite similar to the theoretical ones, and shows that the overall filter transfer function reaches a peak of approximately 20 dB, which is too large to be acceptable.

As the high Q-factor of the Chebyshev filter had made it not to be suitable for the purpose of the filter, it was decided to change the filter to a Butterworth-type one because the Q-factors were lower than those that had been used previously in the Chebyshev-type filter (see Table 2).

4.2.5 Butterworth Filter

As all the previous steps in the filter design flow were still valid, it was only necessary to change the value of the passive components that composed the RC networks in the Sallen-Key biquads. The design process described in § 2.3 was repeated again, considering a Q-factor of 0.6180 and an active element gain of 1.011 for the first stage of the filter, and a Q-factor of 1.6181 and an active element gain of 1.08 for the second stage. After all this process, the required values for creating the first stage of the Butterworth-type filter were: $\rho = 1$, $\gamma = 0.6655$, $R_2 = 1 k\Omega$ and $C_1 = 400 fF$. The values that were needed to create the second stage of the filter were in this case: $\rho = 1$, $\gamma = 0.1658$, $R_2 = 1 k\Omega$ and $C_1 = 400 fF$. The single RC pole was not needed

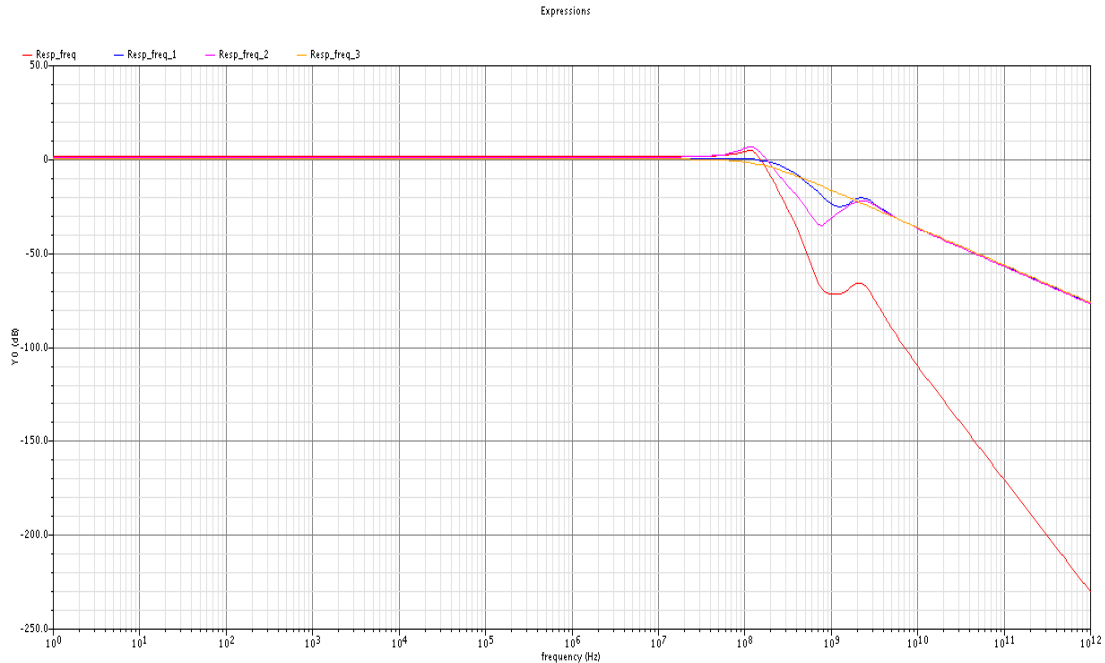


Figure 44: Butterworth filter transfer function (Red). Stage 1 transfer function (Blue). Stage 2 transfer function (Pink). Stage 3 transfer function (Yellow).

to be changed, so the values were the same that had been used in the design of the Chebyshev-type filter: a resistor of $2.5\text{ k}\Omega$ and a capacitor of 0.4 pF .

The transfer functions of the filter and the intermediate stages are shown in Figure 44, which also reveals a dominant peak of approximately 6 dB that comes from the second stage of the filter. The theoretical value for that peak according to (15) is 5.5 dB. The circuit schematic that corresponds with the transfer functions of Figure 44 is shown in Figure 46. This schematic has four more capacitors than the circuit schematic from Figure 15. These four capacitors have a value of 1.0 pF and they were added to improve the high-frequency response, as it can be seen by comparing Figures 44 and 45.

At this point, the final Butterworth-type filter design had been already obtained, but one last thing was done. In order to make a better comparison between the super source follower and the normal source follower, the entire filter was redesigned by using in this case the source follower instead of the super source follower. Then, the active elements were redone to achieve the same gain values than those based on the super source follower but employing the source follower described in 4.2.1. In this case, both active elements were done with the nMOS version of the source follower by adding the required gain stage in order to get the desired gain values. A gain of 1.014 was achieved with the first active element by using a differential amplifier with a gain of 1.158, while the second active element achieved a gain of 1.084 by using an amplifier with a gain of 1.238. The transfer function of both filters is shown in Figures 47 and 48.

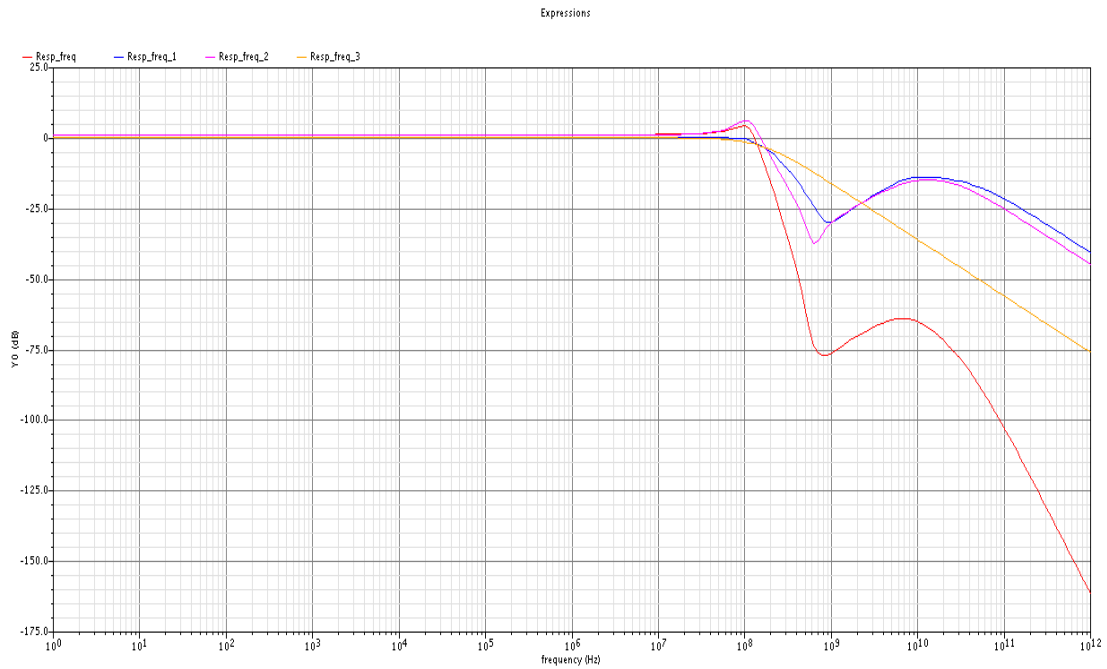


Figure 45: Butterworth filter transfer functions without extra capacitors

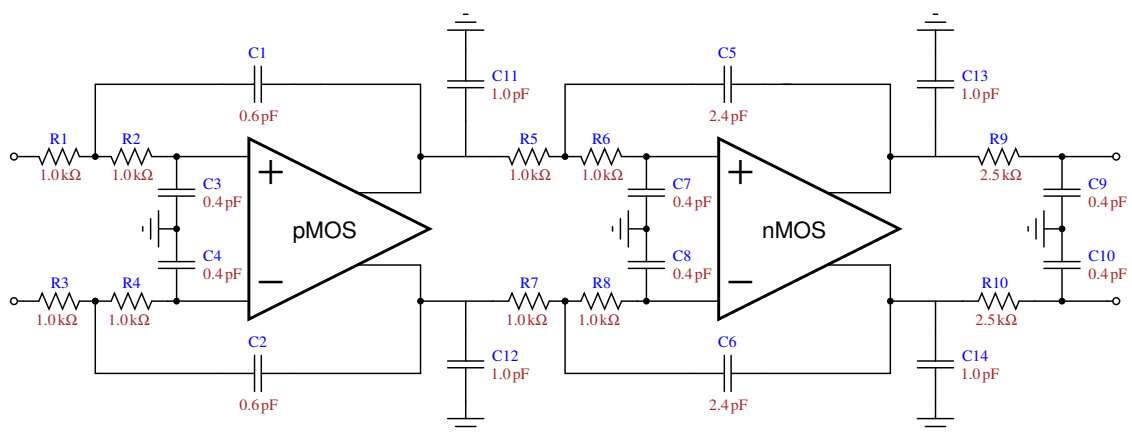


Figure 46: Circuit schematic of the Butterworth filter.

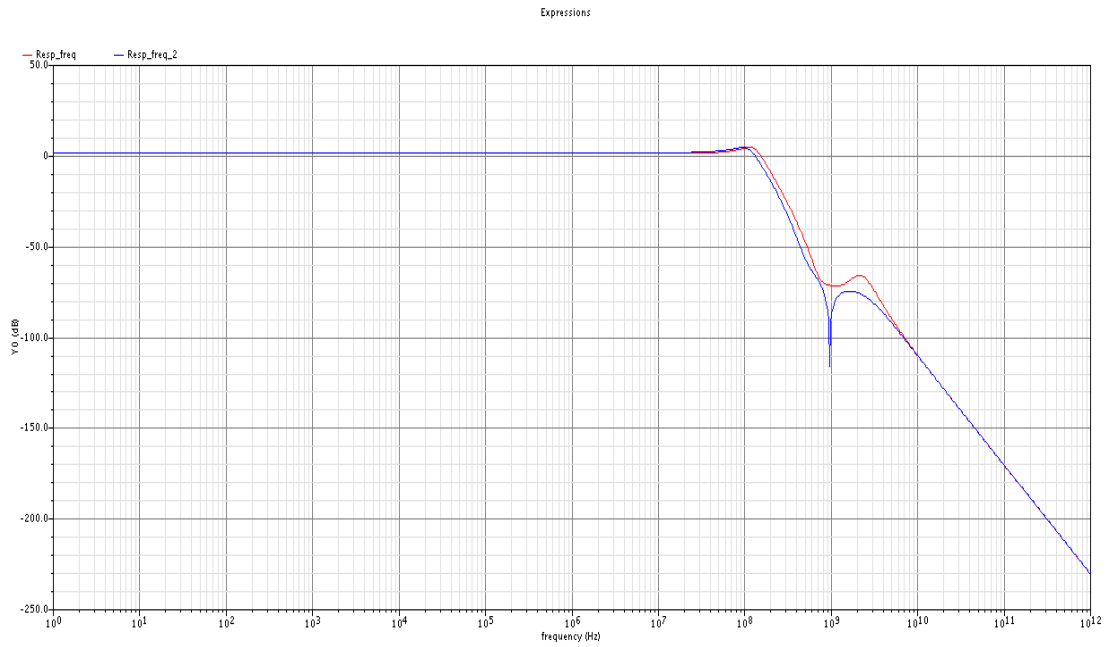


Figure 47: Transfer function of the Butterworth filter based on the super source follower (Red). Transfer function of the Butterworth filter based on the source follower (Blue).

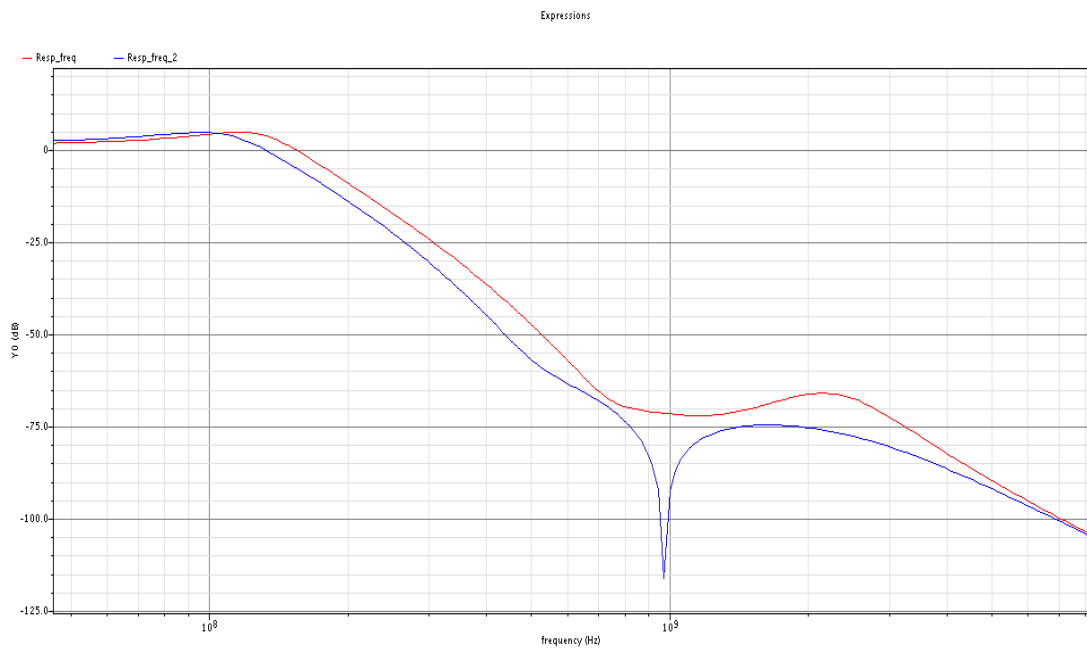


Figure 48: Zoom of the transfer function of the Butterworth filter based on the super source follower (Red). Zoom of the transfer function of the Butterworth filter based on the source follower (Blue).

There is a little difference between the transfer function of the Butterworth filter based on the super source follower and the transfer function of the Butterworth filter based on the source follower. This difference can be better appreciated in Figure 48, where only the peak around the cut-off frequency is shown. As it can be seen, the cut-off frequency of the source follower version of the filter is lower than the cut-off frequency of the super source follower one, and the value of the peak is greater in the super source follower version than in the source follower one, which means that the Q-factors of the super source follower version of the filter are greater than those of the source follower version. As it was explained in the introduction, the higher the output impedance, the lower the Q-factor and the lower the cut-off frequency. The output impedances of the active elements based on the super source follower are $41.45\ \Omega$ and $49.91\ \Omega$, while the output impedance of the active element based on the source follower is $187.55\ \Omega$.

5 Filter Performance

After all the design process had been done it was necessary to study the performance of the Butterworth filter, and also to compare the performance of the filter based on the super source follower with the filter that had been done by using the normal source follower. The performance of these filters was analyzed by making some measurements related to noise and linearity.

Figures 49 and 50 show the noise at the output of the filter based on the super source follower and the one based on the source follower, respectively. The total RMS noise voltage was also calculated, giving a value of $7.7974 \times 10^{-4} \text{VRMS}$ for the first one and $7.5288 \times 10^{-4} \text{VRMS}$ for the second one.

After the noise performance had been analyzed, the linearity of the filter was studied with several steady-state simulations in which the harmonics of the output signal were taken into account. First, the difference between the fundamental frequency component and the third harmonic one was calculated while the amplitude of the input signal was swept. As the desired value for this difference was around 50 dB, the input signal should have an amplitude of 100 mV and not of 200 mV as had been thought for the design (see Figure 51). Second, a two-tone linearity analysis was done by calculating the third order intercept point (IIP3) in both circuits. The results extracted from the simulations gave an IIP3 of 881.31 mV (-1.0974 dB) for the super source follower version of the Butterworth filter and an IIP3 of 902.98 mV (-0.88641 dB) for the source follower version of the filter. The result of the simulation for the first case is shown in Figure 52, while the result of the second simulation has been omitted as they were quite similar. As the IIP3 cannot be shown directly from the result of the simulation, the output data was imported into MatLab and processed to expand the result so it could reveal the intercept point.

Finally, the phase and group delay of both filters were calculated to provide more information related to the performance of these filters. Figure 53 shows the phase and group delay of the filter based on the super source follower, while the phase and group delay of the filter based on the source follower are shown in Figure 55. The remarkable detail of the group delay of these filters is the peak that appears around the cut-off frequency and it is shown in Figures 54 and 56.

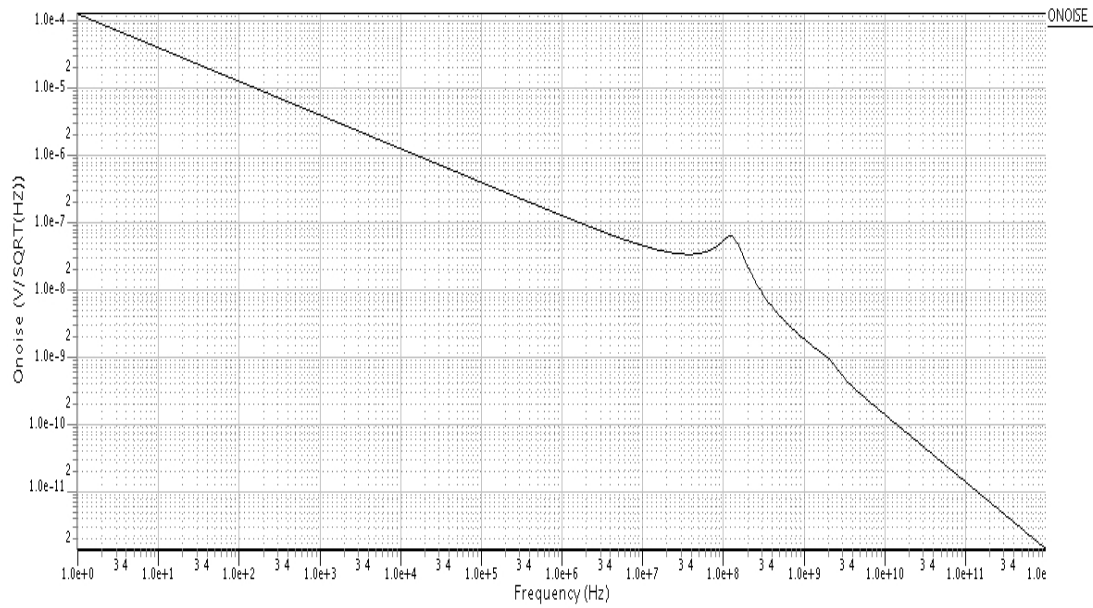


Figure 49: Noise at the output of the filter based on the super source follower.

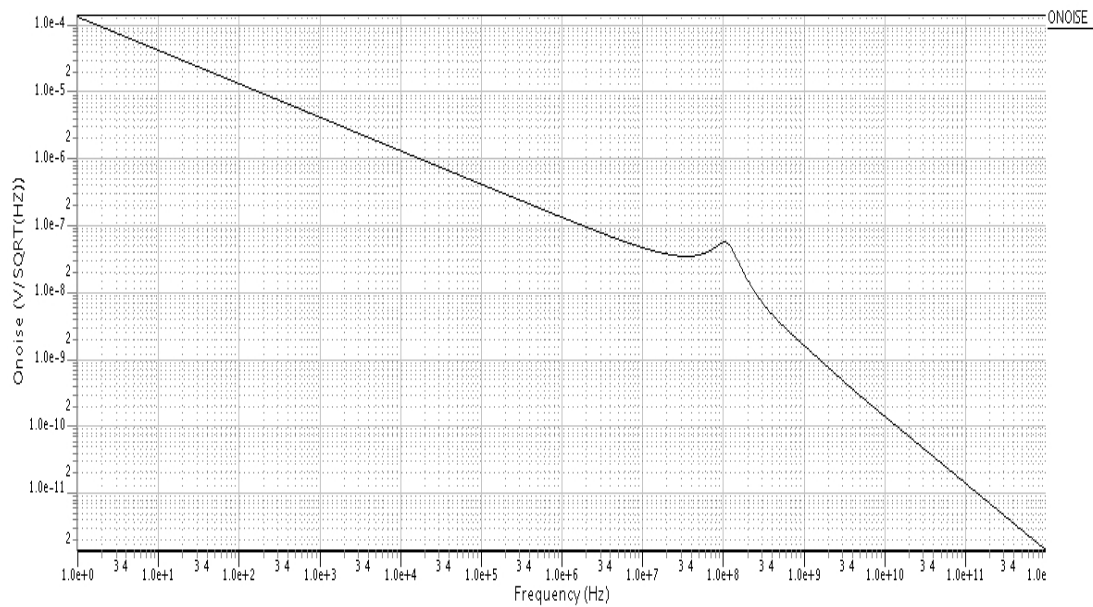


Figure 50: Noise at the output of the filter based on the source follower.

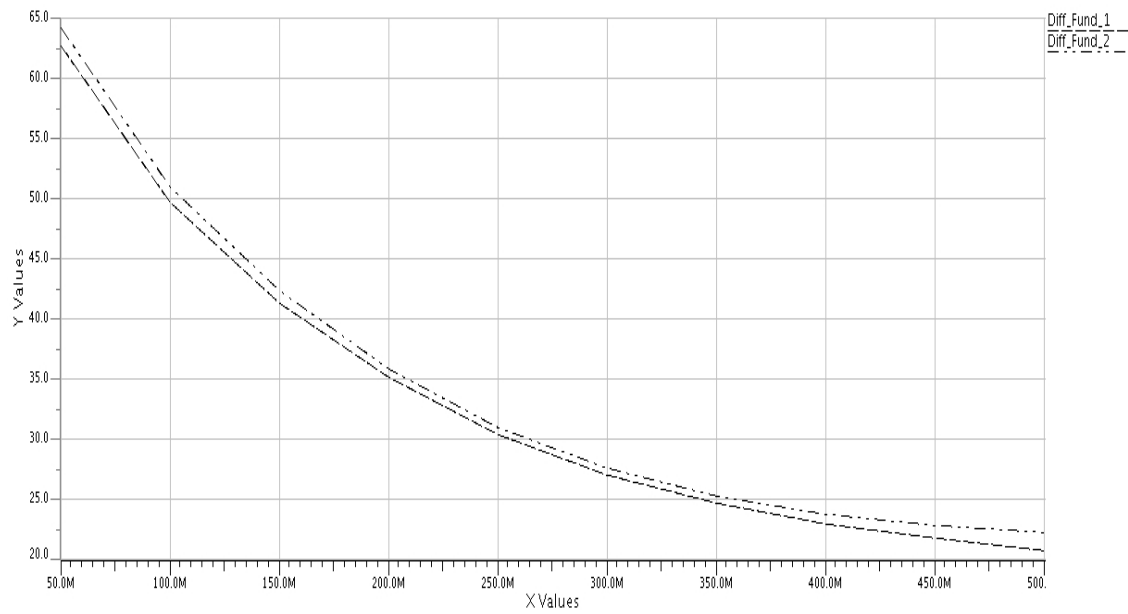


Figure 51: Difference between the fundamental frequency component and the third harmonic component. Super source follower version (—). Source follower version (-----).

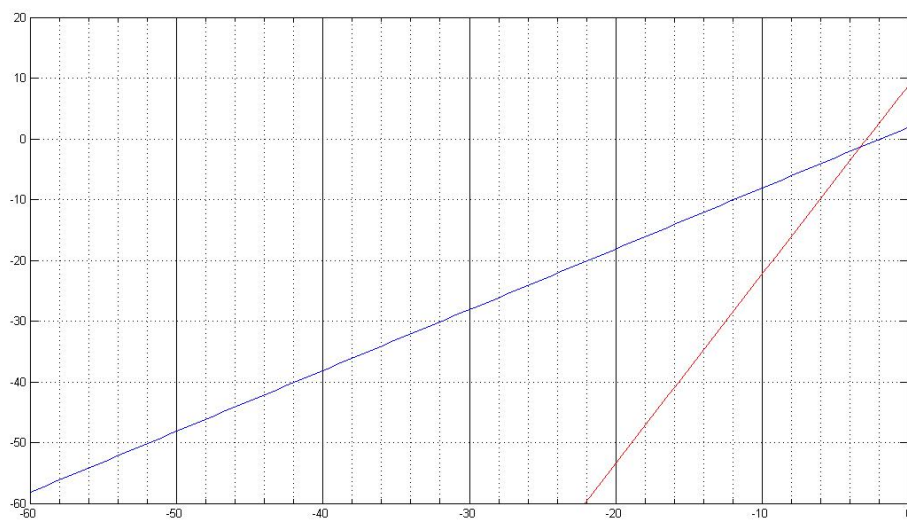


Figure 52: IIP3 graph. Super source follower filter.

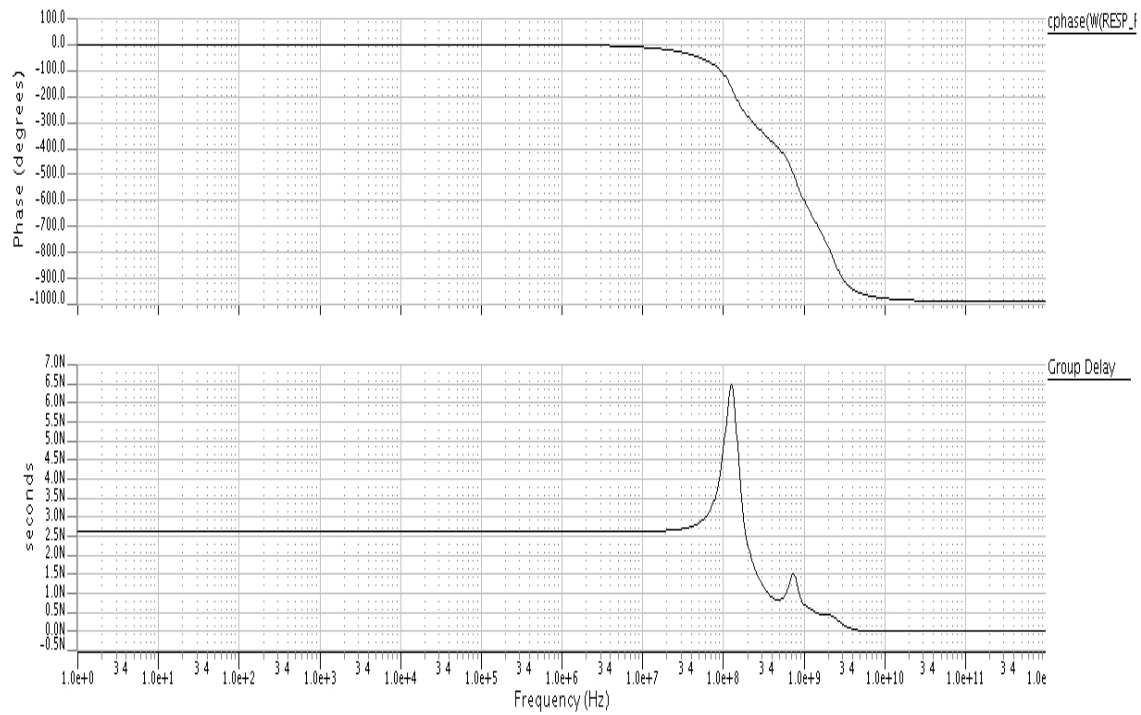


Figure 53: Phase and group delay. Super source follower filter.

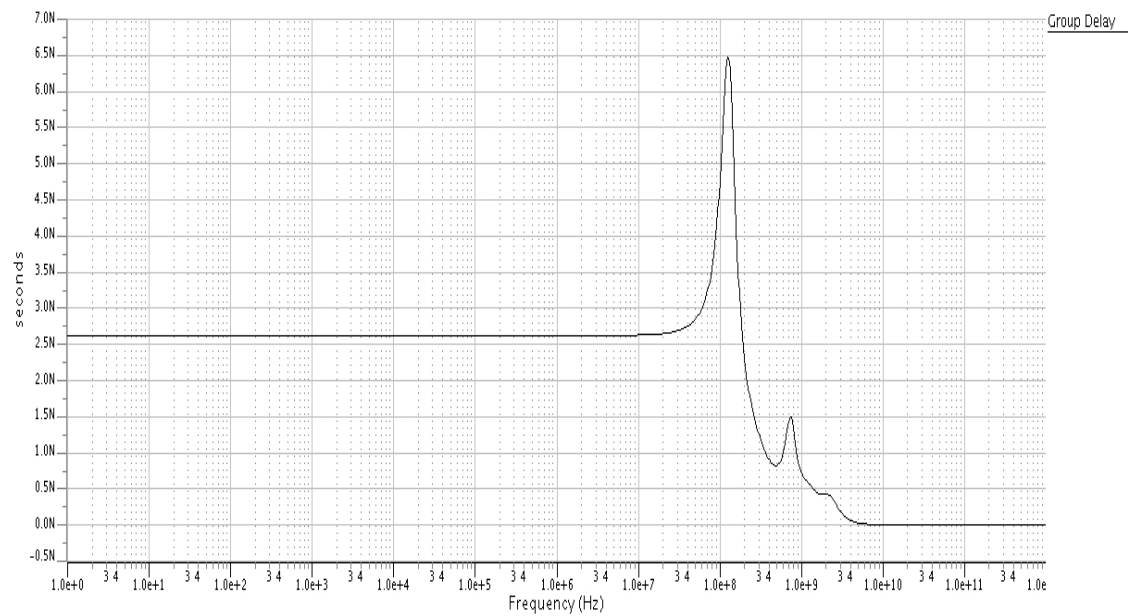


Figure 54: Detail of the group delay peak. Super source follower filter.

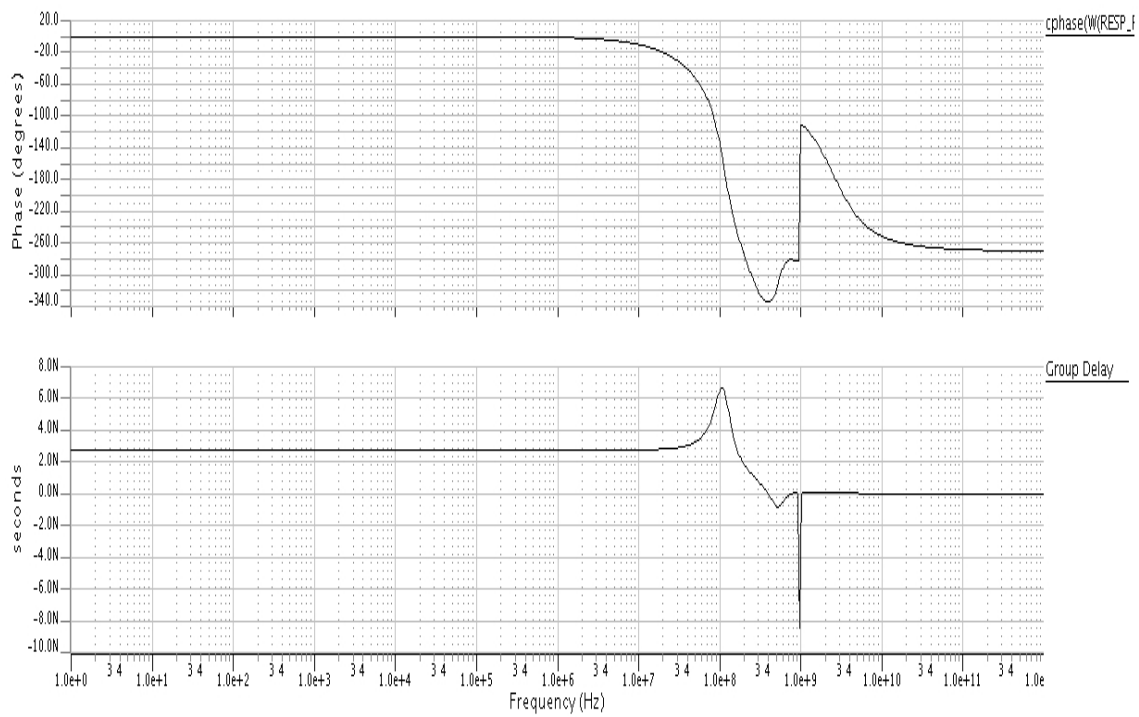


Figure 55: Phase and group delay. Source follower filter.

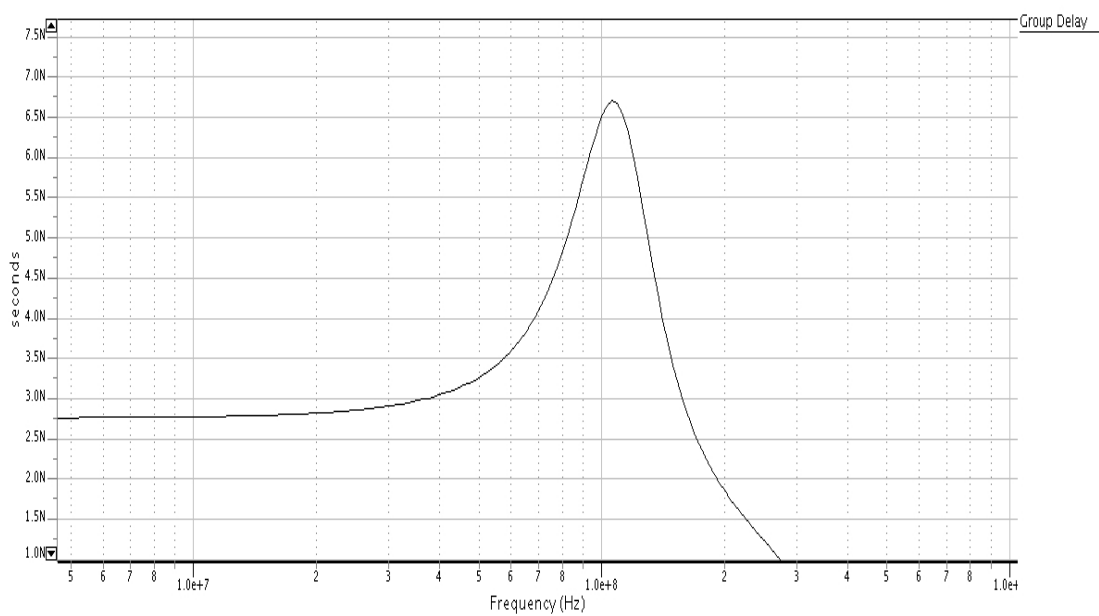


Figure 56: Detail of the group delay peak. Source follower filter.

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