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Continuous-time interface for a micromachined capacitive accelerometer with NEA of 4 μg and bandwidth of 300 Hz

Lasse Aaltonen*, Kari Halonen

SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, 02150 Espoo, Finland

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ABSTRACT

A continuous-time accelerometer interface is feasible when a high dynamic range together with a wide signal band is required. In this paper the implementation of a continuous-time force-feedback loop for a capacitive sensor element with a full-scale signal of $\pm 1.5\,g$ is presented. The interface is measured to attain a noise equivalent acceleration (NEA) density of $500\,\mathrm{ng}/\sqrt{\mathrm{Hz}}$ at 30 Hz for the on-chip digitized output and $300\,\mathrm{ng}/\sqrt{\mathrm{Hz}}$ at 30 Hz for the analog output using a capacitive half-bridge sensor element with a single pair of electrodes. The essential circuit structures of the closed-loop sensor will be presented and analyzed in detail.

1. Introduction

Typically, high-precision capacitive accelerometers operate in a closed loop, thus allowing us to reach for better linearity and resolution and a higher signal band compared to an open-loop sensor interface. Although this is achieved mainly at the expense of increased power consumption, complexity, or costs, the closed-loop operation provides features such as the damping of high-Q resonance modes, which cannot be achieved in an open-loop configuration [1].

Capacitive accelerometers, operating as electromechanical delta-sigma loops, have gained increasing popularity. Implementations of this type of sensor interfaces have been introduced in, for example, [2,3], whereas recent analysis concerning higher order noise shaping is presented in [4]. A common feature of most published delta-sigma interfaces is the use of a low-Q mechanical element. Incorporating a high-Q element in the electromechanical delta-sigma loop complicates the design, as the electronic interface is required to maintain stability, even under the presense of multiple high-Q resonance modes of the mechanical element [5]. An analysis of the use of a high-Q element for a delta-sigma interface is given in [6].

In applications where high resolution and linearity and a large signal band are the main requirements, an analog readout interface can provide an alternative way of implementing the accelerometer. The benefits of continuous-time readout are clear: the elimination of noise folding effects [7], any residual motion [8], and the requirements for very high clock frequencies, which are often needed to attain large bandwidth and resolution. One common reason for not using a continuous-time force-feedback loop for accelerometers is the potential threat of pull-in in the case of a shock condition [9]. This problem can be overcome to a large extent by preventing the short-circuit condition in the sensor element. This is commonly done by utilizing mechanical stoppers [10]. For the interface it is imperative to verify that the feedback signal is not capable of saturating the front-end, even during a momentary shock. If this is not prevented, the sign of the signal and the feedback can change because the active parts of the front-end are malfunctioning. The resulting positive feedback ties the feedback to either supply rail.

New implementations of continuous-time accelerometers, especially those utilizing a force-balancing feedback, are relatively scarce. Examples of earlier work are given in [11,10], where the force-feedback is active in the signal band, which, on the other hand, is lower than the resonance frequency of the sensor. Both sensors are monolithic, whereas the latter has separately optimized drive and sense electrodes, which enables higher detection voltage. In [12] the force-feedback is active below the signal band of interest, hence leaving the sensor to operate in an open-loop at the actual signal band. The work also reports the benefit of using a carrier frequency readout for reducing the effect of low-frequency noise.

* Corresponding author. Tel.: +358 9 4512278; fax: +358 9 4512269.
E-mail addresses: ljaalton@ecdl.tkk.fi (L. Aaltonen), karih@ecdl.tkk.fi (K. Halonen).

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The force-balanced accelerometer of [13] detects the signal a by converting the capacitive signal to phase difference. After transforming the phase to voltage, an integrator is used to balance the sensor element and two zeros to ensure the stability of the loop. The high performance sensors of [14,15] clearly benefit from the closed-loop operation. A sensitive sensor with a low resonance frequency in comparison to the frequency range of interest is used and the feedback increases the signal bandwidth up to the required value. However, very few details of the interface are presented. Compared to other published works, this paper presents a detailed description of the interface electronics, which allows the signal bandwidth to be increased up to or even above the resonance frequency of the high-Q sensor element. The linearity of the implemented sensor is characterized over the temperature range of interest and it is shown that the sensor dc non-linearity can be removed using dc calibration.

In this paper, the structure of the high-resolution continuous-time interface is presented first, in Section 2. The system description is followed by a detailed analysis of the noise sources within the interface. In Section 4 the design of the interface building block is introduced and, finally, in Section 5, the measured results of the closed-loop sensor are provided.

2. Structure and operation of the closed-loop accelerometer

The block diagram of the accelerometer is shown in Fig. 1. The bulk micromachined sensor consists of a single seismic mass between two fixed electrodes. For the continuous-time system, the feedback and the readout are separated in the frequency domain. A differential carrier, fed to the fixed electrodes of the sensor, is used for the readout. Any mismatch between the capacitors of the sensor causes charge to flow to the feedback capacitor of the charge-sensitive amplifier (CSA). The carrier frequency signal is amplified using a chain of high-pass filters (HPF), which also prevent the feedback signal from saturating the readout. The carrier frequency signal is demodulated coherently using an in-phase sample of the original carrier. The downconverted signal, fed through a low-pass filter (LPF) and a controller, is used to balance the forces acting on the sensor seismic mass. The feedback, the controller output, is connected to the non-inverting input of the operational amplifier in the CSA. The feedback voltage biases the middle-electrode of the sensor in such a way that the electrostatic forces balance the sensor element. The feedback voltage is directly proportional to the external acceleration and functions as the analog output of the servo loop. The digital output is created by digitizing the feedback signal.

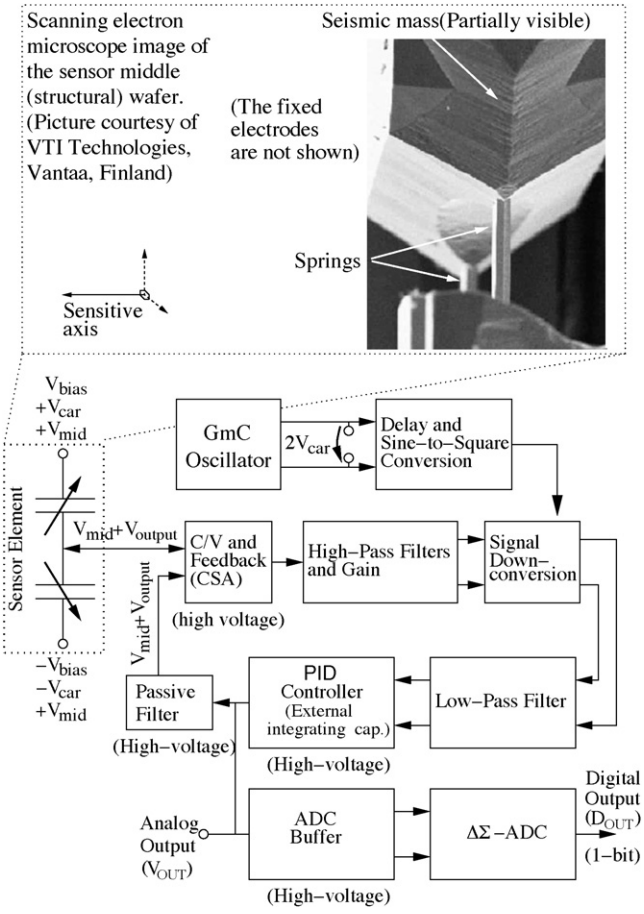

Fig. 1. A block diagram of the accelerometer interface and the electrical model of the sensor. A picture of the middle-electrode of the sensor is also included. The blocks denoted using solid lines are on the ASIC.

The technology used for the design of the interface is a 0.7-μm HV CMOS technology with high-ohmic polysilicon resistors, analog capacitors, and a 5-V nominal supply. The technology also offers parasitic bipolar transistors, vertical NPNs with a cut-off frequency (f_t) of roughly 1 GHz, and lateral PNPs. Because of the wide base and the resulting very low f_t, the use of PNPs is limited to dc sources. The sensor element used for the measurements has its fundamental resonance at 450 Hz and a Q-value of roughly 30, which results in a Brownian equivalent acceleration noise of 60 ng/$\sqrt{\text{Hz}}$.

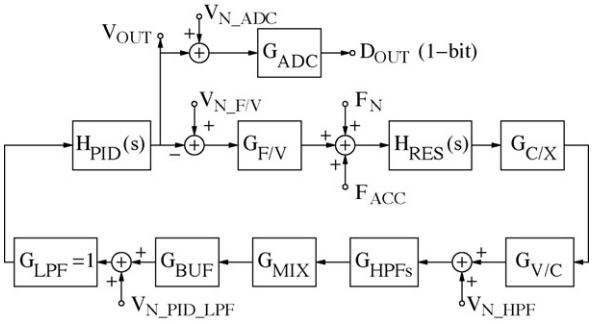

Fig. 2. Linear model of the system that includes different noise sources.

3. Linear model and noise sources of the sensor

In order to evaluate the noise performance of the sensor, the transfer functions (TF) of various noise sources to the sensor output must be derived. The noise sources are shown in the linear model of the system, in Fig. 2.

The element is modeled as a second-order resonator, the TF of which, $H_{RES}(s)$, is given as

$$H_{RES}(s) = \frac{1}{s^2M + s\gamma + K}, \tag{1}$$

where M, γ, and K determine the sensor mass, damping coefficient, and spring constant, respectively. The effective spring constant K is defined as the difference between the mechanical and the electrostatic spring constants, K_{mech} and K_e,

$$K = K_{mech} - K_e = K_{mech} - \frac{2\epsilon_0 A_s (V_{bias}^2 + V_{car}^2/2)}{x_0^3}, \tag{2}$$

where ϵ_0 is the permittivity of the vacuum, A_s the area of the plate capacitors that are used for actuation and signal detection, x_0 the spacing between the capacitor plates, V_{bias} the single-ended dc bias voltage, and V_{car} the single-ended carrier amplitude (see Fig. 1). The resonator transforms the input force to displacement, which is further converted to capacitance with a transducer $G_{C/X} = 2\epsilon_0 A_s / x_0^2$.

The CSA detects the capacitance and transforms it to voltage. The CSA gain $G_{V/C}$ equals V_{car}/C_{fb}, where C_{fb} is the CSA feedback capacitor (see Fig. 7). The voltage mode signal is amplified so that G_{HPF} is the gain of the HPFs at the carrier frequency, G_{MIX} the demodulator conversion gain, and G_{BUF} the mixer buffer dc gain. The amplified and demodulated signal is fed to the PID controller, which creates the feedback that also represents the sensor analog output V_{OUT}. The controller TF is

$$H_{PID}(s) = \frac{K_i}{s} + K_0 + \frac{sK_d}{s/\beta + 1}, \tag{3}$$

where K_i, K_0, and K_d are the gains of the integrator, the proportional controller, and the differentiator, which together form the PID controller. The integrator provides infinite loop gain and allows to improve the linearity, while the parameters K_0, and K_d are required for control over the sensor bandwidth and stability. Further improved controllability of the sensor parameters would require more complex controller, which however is not feasible in a continuous-time analog system. The feedback voltage is converted to force, which compensates for any external acceleration applied. The transducer gain $G_{F/V}$ equals $G_{C/X}V_{bias}$.

In order to simplify the closed-loop TF, two new terms are introduced,

$$G_{FILT} = G_{BUF}G_{MIX}G_{HPF} \tag{4}$$

and

$$H_{RESx}(s) = H_{RES}(s)G_{C/X}G_{V/C}. \tag{5}$$

Now, the TF from input acceleration A_g [g] (1 g = 9.8 m/s^2) to the sensor output voltage V_{OUT} is

$$\frac{V_{OUT}}{A_g}(s) = \frac{H_{PID}(s)G_{FILT}H_{RESx}(s)M9.8}{1 + H_{PID}(s)G_{FILT}H_{RESx}(s)G_{F/V}}, \tag{6}$$

where $A_g = F_{ACC}/9.8/M$ (see Fig. 2). This TF determines both the dynamic properties of the sensor and the sensitivity to mechanical thermal noise F_N [16]. For the implemented and simulated sensor the four poles of (6) are set to the same frequency according to a Butterworth polynomial [17].

The theoretical TFs from the voltage-to-force transducer input noise ($V_{N\_F/V}$), from the input noise of the HPFs (V_{N_HPF}), and from the input noise of the LPF and the controller ($V_{N\_PID\_LPF}$) to V_{OUT} are plotted in Fig. 3 together with the signal transfer function (6). Clearly, the sensor is very insensitive to $V_{N\_PID\_LPF}$ because of the high gain of the preceding blocks. However, the sensitivity to both $V_{N\_PID\_LPF}$ and V_{N_HPF} increases rapidly above the sensor open-loop resonance frequency. The resonance can be seen as a noise minimum in two of the TFs in the figure. The noise $V_{N\_F/V}$ has the same dependency of frequency as the acceleration and the sensitivity to this noise source stays high over the whole frequency range. The parameters used for calculating the TFs are shown in Table 1 and the open-loop properties of the modeled sensor element are shown in Table 2. Table 3 demonstrates the noise densities of the sources in Fig. 2 that correspond to the same noise equivalent acceleration (NEA) of 30 ng/$\sqrt{\text{Hz}}$. The noise densities are valid only in the flat low-frequency region of the noise TFs (see Fig. 3).

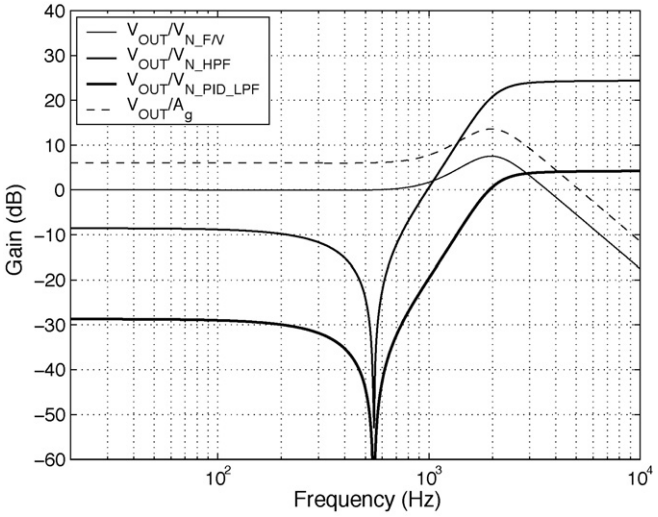

Fig. 3. The curves represent the theoretical noise TFs, where the noise sources correspond to Fig. 2, and the signal TF (6). The selected pole frequency for the sensor is 2 kHz.

Table 1
Parameters of the simulated system.

$H_{RESx}(s)$	$\frac{6.5\times10^6}{4.8\times10^{-6}s^2+3\times10^{-6}s+60}$ $\frac{\text{V}}{\text{N}}$
G_{FILT}	10 $\frac{\text{V}}{\text{V}}$
$H_{PID}(s)$	$\frac{5.0\times10^{-5}s^2+0.45s+2400}{3.0\times10^{-5}s^2+s}$ $\frac{\text{V}}{\text{V}}$
$G_{F/V}$	2.4×10^{-5} $\frac{\text{N}}{\text{V}}$
V_{bias}	3.6 V
$G_{V/C}$	10^{12} $\frac{\text{V}}{\text{F}}$

In order to provide a better understanding of the influence of the noise sources, in the following subsections the design of the interface is commented on from the noise point of view.

3.1. Noise of the carrier and readout (V_{N_HPF})

The demodulator, designed as a full-wave rectifier, downconverts the signal and noise effectively by multiplying them by a square wave that has unity amplitude. Hence, the noise gain for a white noise floor at the rectifier input can be calculated as a sum of squared Fourier series terms of the square wave:

$$G_{N\_DEM} = \frac{4}{\pi}\frac{1}{2}\sqrt{2}\sqrt{\sum_{i=1}^{\infty}\frac{1}{(2i-1)^2}} = 1. \tag{7}$$

The $\sqrt{2}$-term accounts for noise folding from both the positive and negative offset frequencies of each harmonic component and the 1/2-term for the splitting of power when multiplying the noise by each sine component. On the other hand, the signal conversion gain G_{MIX} is defined as the ratio between the output dc and input ac amplitude, $G_{MIX} = V_{dca}/V_a$. The dc of the output waveform, depicted in Fig. 4 as a function of input amplitude V_a and phase errors ϕ_e and

Table 2
Properties of the bulk micromachined sensor element used in simulations.

Resonance frequency	650 Hz
Sensitivity (dc)	3.8 pF/g
Q-value	> 500
Seismic mass, M	4.8 mg

Table 3
Noise densities of sources in Fig. 2 that correspond to the same noise NEA density of 30 ng/$\sqrt{\text{Hz}}$ at frequencies below the resonance frequency of the open-loop sensor. The term G_{MIX} represents both the gain of the demodulator and the decrease in SNR after demodulation because of noise folding (see Section 3.1).

$V_{N\_F/V}$, V_{N_ADC}	60 nV/$\sqrt{\text{Hz}}$
F_N	1.4 pN/$\sqrt{\text{Hz}}$
V_{N_HPF}	160 · G_{MIX} nV/$\sqrt{\text{Hz}}$
$V_{N\_PID\_LPF}$	1.6 μV/$\sqrt{\text{Hz}}$

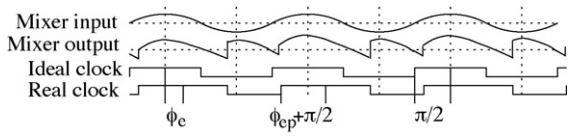

Fig. 4. Example waveforms of the mixer.

ϕ_{ep}, can be expressed as

$$V_{dca} = V_a \frac{2}{\pi} \cos(\phi_e) \cos(\phi_{ep}). \quad (8)$$

The phase error terms represent both the delay mismatch between the clock and the input signal ϕ_e and the pulse width error ϕ_{ep}. Hence, the input-referred noise is increased by a factor of $1/G_{MIX}$. In addition to reducing the gain G_{MIX}, a non-zero ϕ_{ep} will cause dc to leak to the demodulator output. The gain of the leakage is $2\phi_{ep}/\pi$. The leakage compromises the stability of the sensor [17] and can degrade the noise performance as a result of the high low-frequency noise content at the demodulator input (HPF output).

The amount of noise folded during multiplication by a square wave does not essentially depend on the phase errors ϕ_e and ϕ_{ep}; however, the effective signal at the demodulator output does, according to (8). The noise penalty is given by G_{MIX} (see Table 3), which is, in an ideal case, $2/\pi$ when it is assumed that the noise source V_{N_HPF} has a flat noise density at and above the carrier frequency. If the noise bandwidth is limited so as to include only the region around the carrier frequency, the SNR drop decreases to $\sqrt{2}$ as (7) is less than unity. The improvement resulting from the limited noise bandwidth is fairly small compared to the case with a white noise floor ranging up to infinity and, in fact, it is more important to maintain minimal phase errors in order to maximize the conversion gain.

Another noise source of the demodulator is the phase noise of the demodulator clock, which causes input signal-dependent noise. The oscillator phase noise is canceled in all cases as both the signal and the clock use the same oscillator as a signal source. The effective phase noise stems from both the delay tuning, used to equalize the signal and clock path delays, and the sine-to-square conversion, required to transform the sinusoidal carrier to the demodulator clock. When the delay tuning circuit has a gain of $G_{\phi/V}$, $\phi_e = \phi_{edc} + \phi_{n\_rms}$, and $\phi_{ep} = 0$ the mixer output noise resulting from the phase noise can be approximated, by linearizing (8), as

$$V_{N\_DEM} \approx \frac{2V_a}{\pi} \phi_{n\_rms} \sin(\phi_{edc}) \approx \frac{2V_a}{\pi} G_{\phi/V} V_{d\_delay} \sin(\phi_{edc}). \quad (9)$$

The terms ϕ_{n_rms} and ϕ_{edc} represent the phase noise caused by low-frequency noise in V_{d_delay}, and the dc phase error. Now, the sensitivity to noise in the delay control signal V_{d_delay} is at its minimum when ϕ_{edc} is zero. Although the delay control signal can be low-pass filtered, the noise can also fold, for example during the sine-to-square conversion [18].

An additional noise source contributing to V_{N_HPF} is the carrier (see Fig. 1) that is used to detect the difference in the signal capacitances. Although the differential component of the carrier is the only beneficial one, the common-mode (CM) signal also has an effect on the CSA output. The coupling of the CM carrier signal is depicted in Fig. 5, which can be used to calculate the amount of CM carrier noise that can be tolerated. The parameters in Table 1 correspond to C_{fb} of 2 pF and $C_{s1} + C_{s2}$ of 24 pF. The resulting gain of 12 allows a maximum V_{N_CM} of $13 \cdot G_{MIX}$ nV/$\sqrt{\text{Hz}}$ when the V_{N_HPF} is $160 \cdot G_{MIX}$ nV/$\sqrt{\text{Hz}}$ (Table 3). It is assumed that V_{N_HPF} has no other noise contributors. Hence, this noise source, dominated by the CM noise of the differential buffer for the carrier (see Section 4.1), is one of the most significant ones. Similarly, other noise sources with a very high gain are the high-frequency noise of the bias voltage V_{bias} and the feedback voltage. Both of the sources can be filtered. The differential noise of the carrier has an effect only when there is an imbalance between the sensor capacitors and the effect is considerably smaller than that of CM noise.

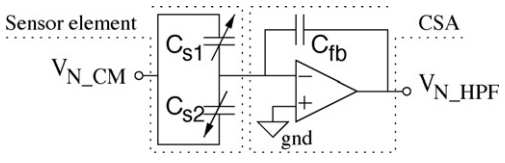

Fig. 5. A simplified circuit diagram of the readout front-end to model the effect of the high-frequency CM noise of the carrier.

The noise of the CSA itself is also an important parameter. However, several publications exist, for example [19], about the noise optimization of the CSA.

The HPFs of the readout serve three purposes: they amplify the carrier frequency signal, attenuate the feedback signals, and remove the offsets of previous stages and in this way prevent the readout from saturating. The noise specifications are simple to meet, especially when the CSA gain is fairly high, as in the example case (Table 1).

The gain of the HPFs should be designed to be high enough to allow the use of the more compact but high-flicker-noise MOSFET operational amplifiers in the LPF.

3.2. Noise of the controller and LPF ($V_{N\_PID\_LPF}$), $V_{N\_F/V}$ and V_{N_ADC}

As the NEA densities shown in Table 3 indicate, the high gain of the readout enables loose noise requirements to be set for the controller. With complete integration as a typical goal, the area optimum is reached when the resistors and capacitors are equally large in area. The gain of the controller must be high enough to allow easier integration. High gain also increases the sensor pole frequency, which further improves the force balance at ac accelerations. The sensor bandwidth, however, can be severely limited by the parasitic modes of the sensor element (see Section 5), which must not be excited. Another limiting factor is the separation of the feedback and detection, which may require an unacceptable amount of chip area and power. The noise of the digitizer V_{N_ADC} and the noise in the feedback path after the controller have a unity gain to output at low frequencies. Hence the number of circuits after the controller should be kept to a minimum.

4. Design of the interface

The sensor poles can be designed at a higher frequency than the actual signal band of interest in order to reduce, for example, the temperature effects. In this design, where the element was fixed, the system pole frequency was designed to be variable in order to avoid instability resulting from a critical parasitic resonance mode [17]. The signal bandwidth of 300 Hz was selected for the system, while the pole frequency was designed to be tunable from roughly 1 to 2 kHz. The option to set the poles at 1 kHz also necessitated the use of an external integrator capacitor as the controller components were otherwise impractical for integration. To provide information about the building blocks of the interface, the relevant circuit structures will be presented in the following subsections.

4.1. Carrier generation

The carrier frequency is determined on one hand by the complexity of the filters and the pole frequency of the sensor and, on

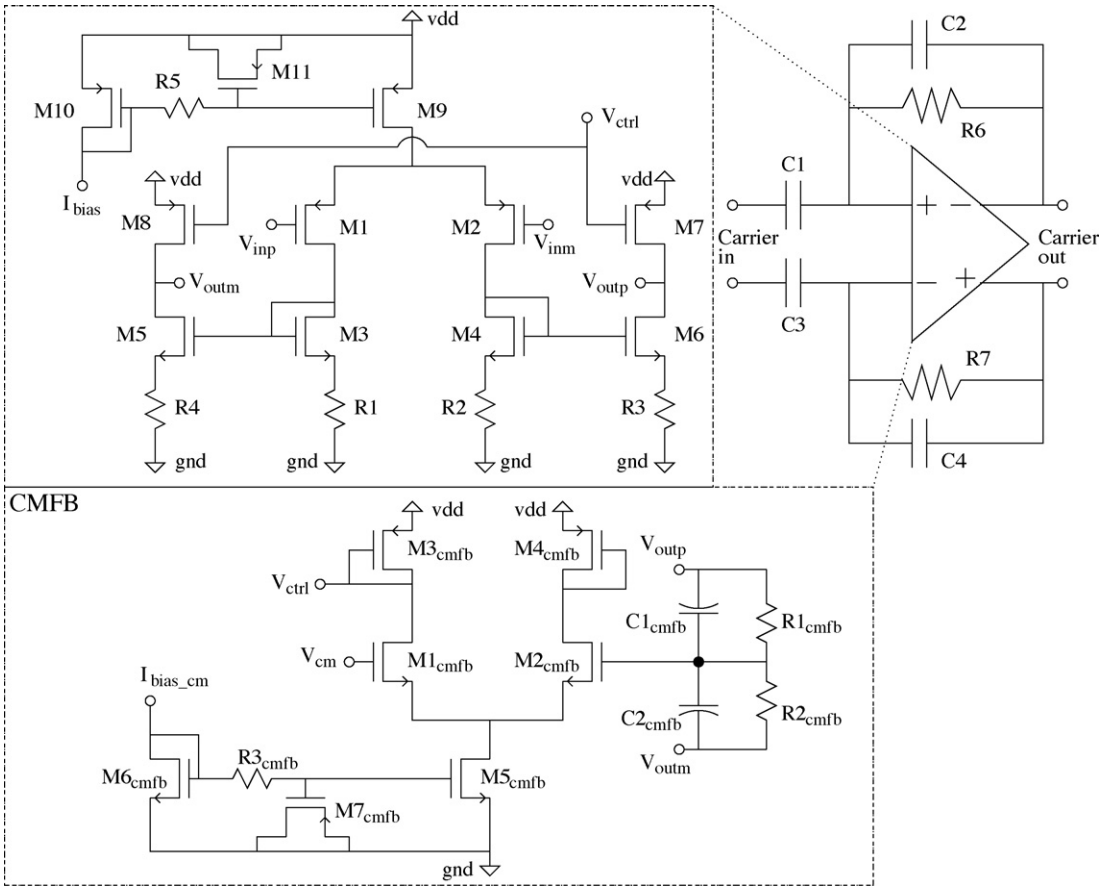

Fig. 6. The carrier buffer and the operational amplifier with the CMFB used.

the other hand, by the power consumption specifications and technology. The selected frequency ω_c of the sinusoidal carrier is 3 MHz and it is generated using a GmC-oscillator, which is described in detail in [20].

As described earlier, the CM properties of the carrier signal are of the utmost importance. The HPF that buffers the carrier uses a current mirror operational amplifier, the schematic of which is shown in Fig. 6 that includes also the schematic of the common-mode feedback (CMFB) of the amplifier. The CM loop is designed to have a bandwidth of 70 MHz (20 pF single-ended load) and an output noise density of 6.5 nV/$\sqrt{\text{Hz}}$. In order to attain a CM noise this low, all the biasing paths must be filtered. The light degeneration of the NMOS transistors also lowers the CM noise. The high bandwidth and transconductance of the CMFB reduces both the noise and the CM signal. The CM signal exists as a result of second-order distortion of the differential path and the full-scale differential signal. The CMFB can attenuate this 6-MHz component by a factor of 7, compared to a mere dc CM control.

The differential path has a nominal gain of 9.6 dB with a −3 dB frequency of 11 MHz and an output noise density of 45 nV/$\sqrt{\text{Hz}}$. The current consumption, 3.6 mA, of the buffer is determined by the capacitive load set by the sensor element; a single-ended signal amplitude up to 2 V can be delivered to the element without increasing the distortion.

4.2. Charge-sensitive amplifier

As the CSA closes the loop, the feedback path requires low noise properties at low frequencies, implying very low flicker noise content. Low-noise operation is also required at the carrier frequency, where the signal is read from the sensor. The schematic of the folded cascode operational amplifier (OPAMP) which fulfills these requirements is shown in Fig. 7. One problem with using BJT input devices in the CSA is the base current, which can be as high as a few microamperes when the current gain is small (∼50). Normally, the input bias current can only be supplied through the feedback resistor R_{fb}, which should thus be minimized. A similar requirement is also imposed by the feedback, which should be maximally attenuated at the CSA output. The noise minimization, however, requires the feedback resistors to be maximized. The gain, defined by C_{fb}, should also be maximized in order to reduce the power and area of the readout chain that follows the CSA. A small C_{fb}, on the other hand, makes the CSA more susceptible to rapid transients of the feedback signal. The selected R_{fb} of 700 kΩ and C_{fb} of 2 pF offer a corner frequency of 120 kHz. The additional branch connected to the CSA input is used to copy the base current of Q_5, which is fed to the inverted input of the amplifier in order to compensate for the Q_1 base current. This configuration reduces the CSA output dc level, ideally to the same level as the input.

From the system stability point of view it is crucial that the CSA gain remains inverting in every condition. If not, the feedback sign changes and the loop finds a stable operation point where the feedback is stuck at either supply rail. For the current design the feedback signal is limited externally, which does not prevent the CSA from saturating as a result of a fast feedback transient. This kind of ac instability complicates the system behavior under some circumstances, for example, where the potential parasitic mode is excited because of an external impulse.

The HV supply (V_{ddhv}) of 12 V is used, as the electrostatic feedback requires voltages close to ±3.4 V for ±1.5 g acceleration when V_{bias} is 3.6 V. The diodes D_{1-4} protect the low-voltage transistors M_1 and M_2 from excess drain-source voltage during power-up. BJT

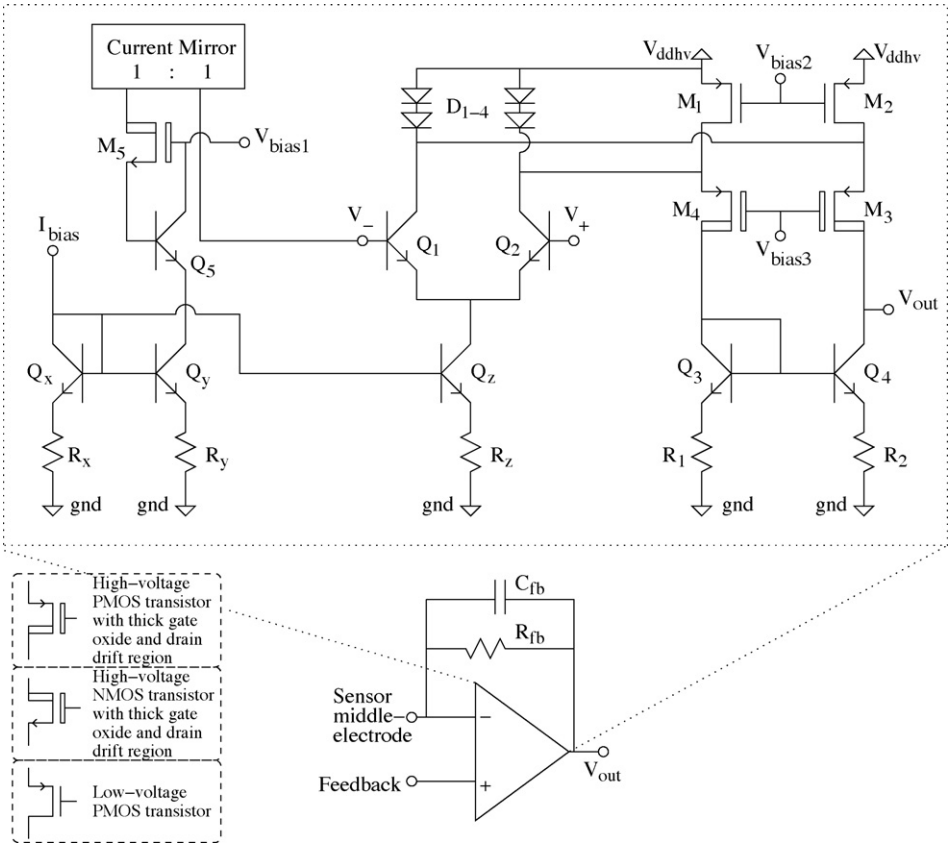

Fig. 7. Operational amplifier of the HV CSA.

transistors Q_{1-4} are used to reduce flicker noise. For the same reason the use of NMOS transistors is totally avoided in the differential signal path, as their flicker noise is considerably higher than that of PMOS transistors. The base current compensation roughly doubles the base current noise and hence increases the total output noise, 53 nV/$\sqrt{\text{Hz}}$ (input capacitance 20 pF), by less than 10%. The transistors M_1 and M_2 both supply 160 μA, while 80 μA of this is consumed by each transistor of the input pair.

4.3. HPFs, demodulator and LPF

The high-pass filters in Fig. 8 provide the necessary gain for the readout, while attenuating low-frequency components as much as possible. In addition, they convert the signal to differential form, hence enhancing power supply insensitivity and relaxing the linearity requirements. The operational amplifiers are designed as basic low-voltage folded cascode CMOS operational amplifiers. The HPFs and the CSA result in a CSA output-referred noise of 56 nV/$\sqrt{\text{Hz}}$.

The first HPF in the figure is of the first order and has a nominal gain of 3 and a high-pass corner frequency of 310 kHz. The second, second-order multiple feedback (MFB) HPF has a gain of 2 and a corner frequency of 750 kHz and the third, first-order variable gain HPF has a gain and a corner frequency of 0.8–2 and 670 kHz.

To minimize the effect of coherent amplitude detection on both noise performance and system dynamics, the delay between the signal and the clock is set to zero by using a delay control circuit. The phase shift of the readout is a function of process variations, temperature, and gain, which means that some tunability is required in the delay control. However, the delay temperature sensitivities of both the signal and the clock paths should match, so that no active delay compensation is needed. The implemented delay control of Fig. 9 has two band-pass filters, in which the upper limiting frequency, and hence the phase, is controlled by changing the gate bias of the MOSFET resistors. The coarse tuning is implemented as 2-bit matrices of input capacitors and resistors, in order to compensate for the gain change resulting from the corner frequency control. The phase noise is reduced by making the gate control independent

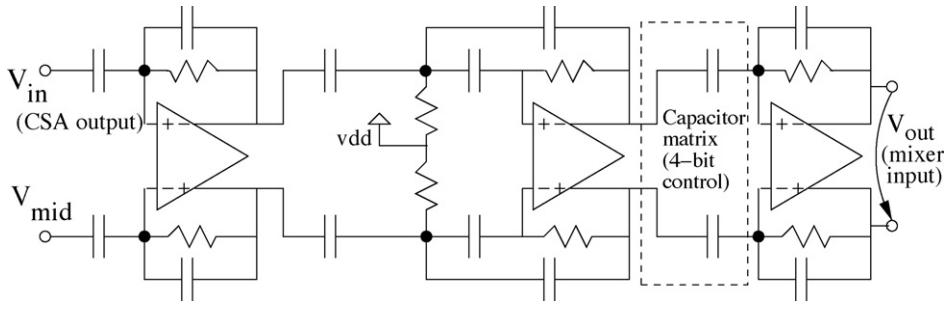

Fig. 8. The chain of HPFs used for the readout of the sensor.

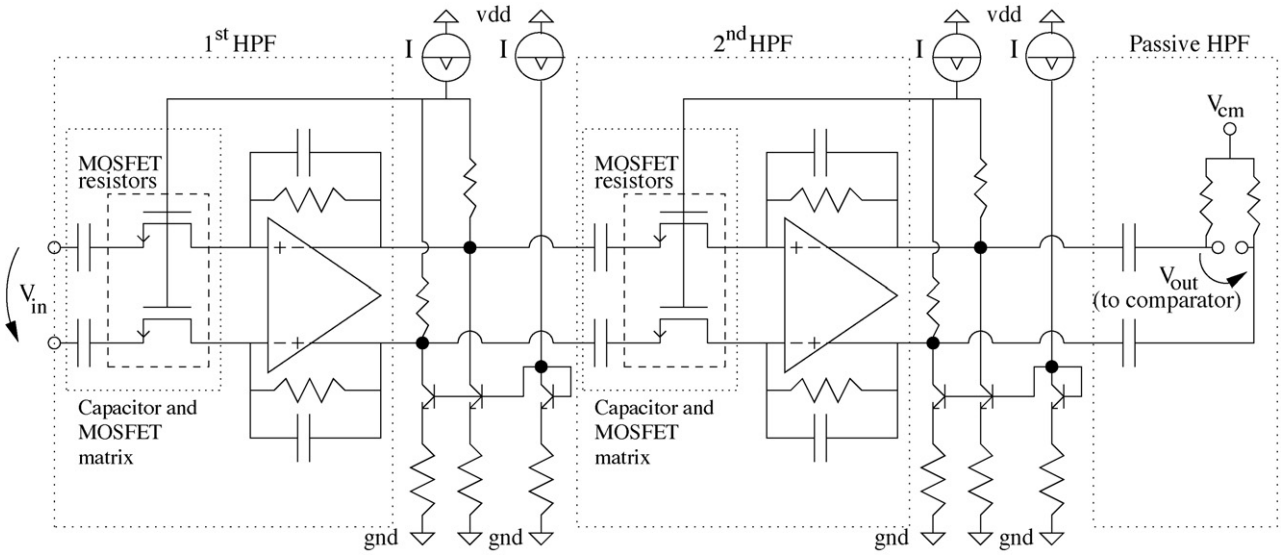

Fig. 9. The schematic of the controllable delay that is used to minimize the phase error between the signal and the clock before the amplitude extraction.

of the amplifier CM noise and by reducing the flicker noise in the delay control path with source-degenerated bipolar current mirrors. The last stage before the comparator, a passive HPF, removes the low-frequency noise from the HPF output.

The coherent detection of the envelope is done using a full-wave rectifier, which is implemented as a switching demodulator (chopper) shown in Fig. 10. The switches, transmission gates, allow high signal levels to be passed through the demodulator without increasing the level of leakage. The capacitor C_{lp} creates a pole at roughly 1 MHz to prevent the amplifier from slewing, while C_1 compensates for the pole created by the buffer feedback resistors and the amplifier input parasitic capacitors. The buffer noise, referred to its input, is typically 500 nV/$\sqrt{\text{Hz}}$ at 1 Hz and 40 nV/$\sqrt{\text{Hz}}$ at 300 Hz. The supply current of the buffer amplifier is 770 μA. The operational amplifier used is a two-stage Miller-compensated differential difference amplifier, similar to that in Fig. 11 with an additional input pair. The demodulator includes also a duty ratio balancing circuit [17].

In order to remove the high-frequency components after the demodulation without inflicting much delay, a sixth-order LPF is used. An optimal design would be likely to allow a lower order filter to be used, but in order to avoid instability under all system settings, due to either excessive phase shift or insufficient attenuation [17], the sixth-order Butterworth-type LPF is selected. The LPF is designed using three MFB sections of Fig. 11. The two-stage Miller-compensated operational amplifier has a PMOS input pair and degenerated NPNs as the load for the first stage. The use of NMOS transistors is avoided in the first stage because of their high flicker noise content. The source-followers between the first and second gain stages are required for level shifting. Only a single CM feedback is used for the amplifier and hence there is a potential stable operation point where both the inputs and outputs are tied to the *vdd* rail. Simulations are run to verify that this operation point does not occur. The amplifier gain-bandwidth product can be as low as 5 MHz in the worst case, which means that it has a considerable effect on the filter pass-band edge gain characteristics. On the system level these changes have a small effect, but they can increase sensitivity to mixer leakage by increasing the maximum loop gain between the stop-bands of the HPFs and LPF. To compensate for process variations, the −3 dB frequency of the filter can be controlled externally (2-bit control) from 200 to 500 kHz by changing the capacitor values. The LPF (unity gain) noise is typically 1300 nV/$\sqrt{\text{Hz}}$ at 1 Hz and 400 nV/$\sqrt{\text{Hz}}$ at 300 Hz. The dotted box (Fig. 11) shows the differentially connected capacitor, which is split into two and connected to V_{cm} so as also to allow effective attenuation for CM signals.

4.4. Controller and digitizer

As the single-ended CSA output is converted to differential, the signal must be converted back to single-ended to drive the element. The instrumentation amplifier is placed before the controller, because of its reduced sensitivity to noise (see Table 3). Because of the large time constants, the use of a single-ended controller topology offers considerable savings in area. The TF of the controller corresponds to (3) and can be found in [21], together with more information about the implementation.

To achieve a digitized signal of sufficient accuracy is a challenging task. The low-frequency noise in the ADC (analog-to-digital converter) reference voltages, in the potential ADC buffering circuits, and in the ADC itself should be minimal. On the other hand, the controller output fed to the digitizer is very sensitive to

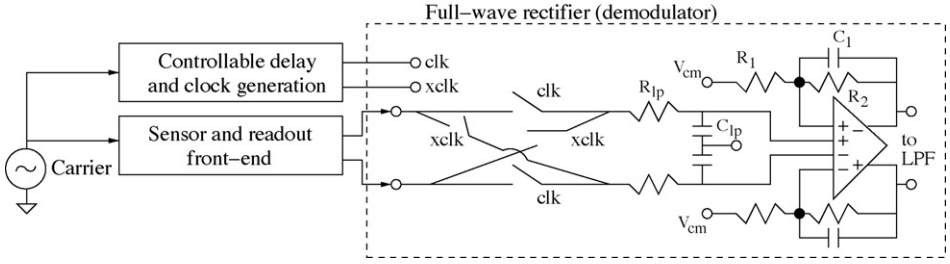

Fig. 10. The demodulator with a differential buffer (gain of $G_{BUF} = 4$), which prevents the resistive loading of the switches.

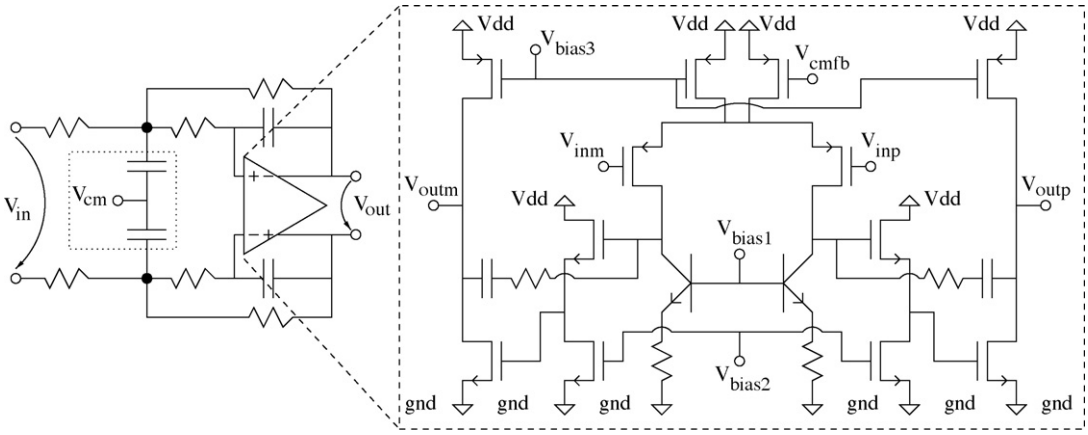

Fig. 11. One of the three MFB cells in the LPF and the operational amplifier used.

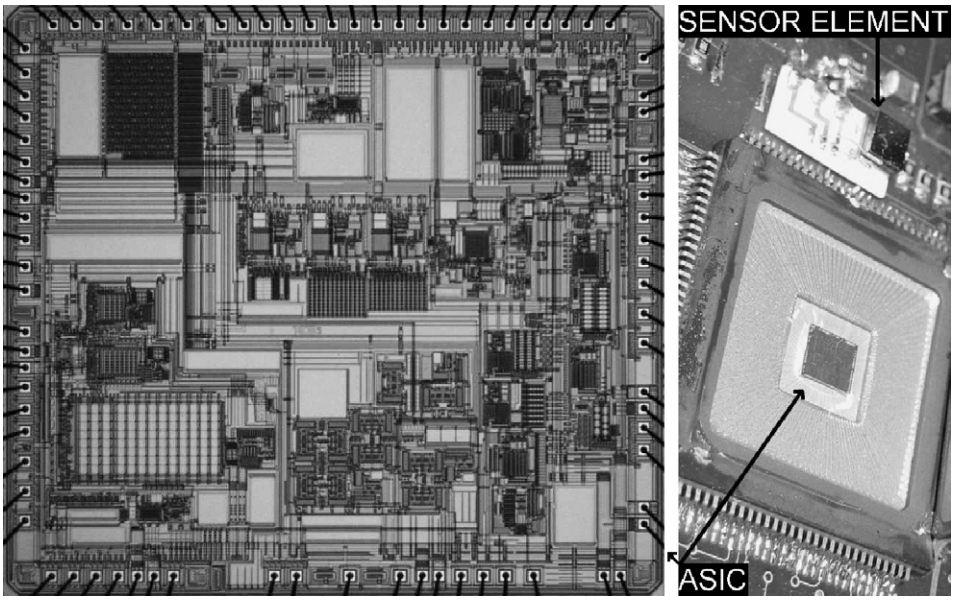

Fig. 12. The microphotograph of the implemented chip, and the photograph of the combined chip in a quad flat package and the sensor element.

high-frequency interference as it will be heavily amplified in the CSA. In addition, the controller has a HV single-ended output. For these reasons, finding the optimal digitizer topology is challenging.

The implemented circuitry, reported in [22], includes a differential HV buffer that converts the signal to differential with an amplitude smaller than the nominal supply. The buffer is followed by a differential $\Delta\Sigma$-ADC (see Fig. 1).

5. Measured results

The chip was combined with a bulk micromachined element on a printed circuit board (PCB), as shown together with chip microphotograph in Fig. 12. The references for the interface and the ADC clock were generated externally. The carrier (V_{car} in Fig. 1) is fed to the sensor through 100-pF capacitors and the external bias voltages (V_{bias}, V_{mid} in Fig. 1) through 5-kΩ resistors. The total and block-

Table 4
Chip area and current consumption of the interface building blocks.

	Supply current (mA)	Area (mm^2)
GmC-oscillator	0.3	0.5
GmC-oscillator buffer	3.6	0.4
Controllable delay	2.0	0.8
CSA (HV supply)	0.3	0.2
HPFs	2.8	0.7
Mixer (including buffer)	1.0	0.6
LPF	1.3	1.2
Controller (HV supply)	0.6	1.8
ADC & buffer	3.5	3.4
Complete chip	15.4	22

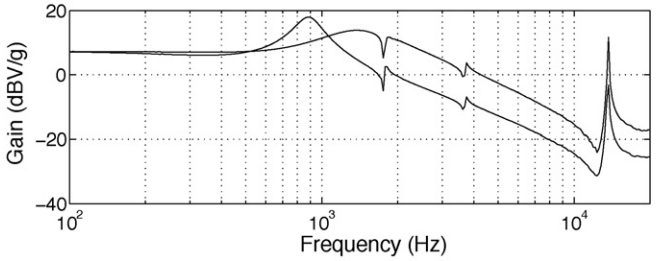

Fig. 13. The transfer function with higher bandwidth, gain maximum at 1.4 kHz, is roughly the maximum bandwidth obtainable. The second curve corresponds to the system gain characteristics when the loop gain is halved.

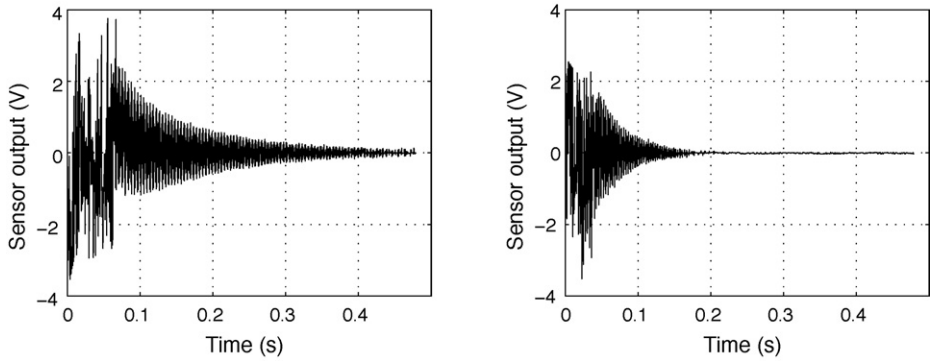

Fig. 14. Time domain settling after high-magnitude impulse which awakens the mode at 11 kHz. The figure on the left corresponds to the higher bandwidth of Fig. 13 and the figure on the right to the lower bandwidth of Fig. 13.

level chip area and the current consumption are summarized in Table 4.

The closed-loop TFs were measured using a signal analyzer (Agilent 4395A) and electrostatic excitation [17]. The maximum system pole frequency is shown in Fig. 13. The pole frequency is roughly equal to the position of the gain maximum. The bandwidth of the system is limited by the resonance mode at 11 kHz. With high signal bandwidth the loop gain at the parasitic resonance frequency is also increased, which results in an increased Q-value and potential instability. When the loop gain is lowered, also shown in Fig. 13, the Q-value is reduced. The same effect can be seen in the time domain, in Fig. 14, where the two impulse responses correspond to the TFs of Fig. 13. The excitation is applied as a sharp knock on the PCB, which causes the system to saturate and parasitic resonance to awaken. The system returns to the linear operation region after the initial ac instability. The settling speed is considerably lower (Q-value higher) in the left-hand subfigure of Fig. 14, which corresponds to the higher loop gain.

The TFs are also measured at the extreme values of the specified temperature range. The results for a single gain configuration are shown in Fig. 15 at three temperatures. The three TFs indicate the same dc gain, as expected in closed-loop configuration. The inset figure shows the theoretical TFs where the resistivity is assumed to vary ±10%. This variation is approximately the same as the temperature causes in integrated resistors, which predominantly affect the PID controller properties. The temperature effects are mostly visible at the gain peak, where the gain variation of both the theoretical and the measured TFs is alike. Any major gain change as a function

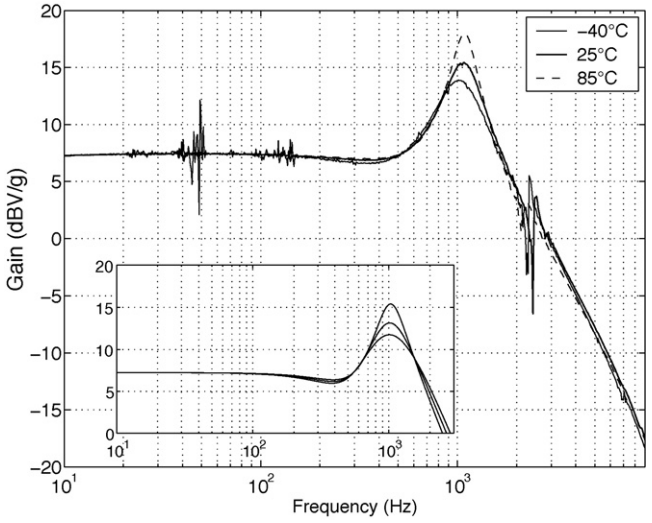

Fig. 15. The measured transfer functions at three different temperatures. The inset shows three theoretical transfer functions, which assume ±10% variation in the resistor values.

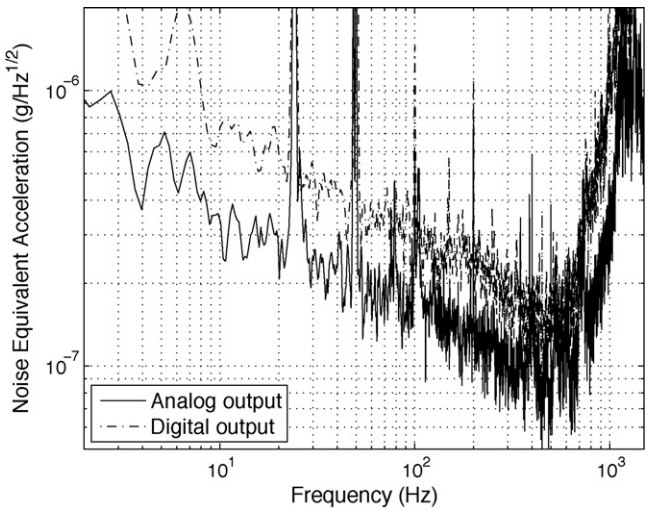

Fig. 16. The sensor noise density of both the digital and analog outputs.

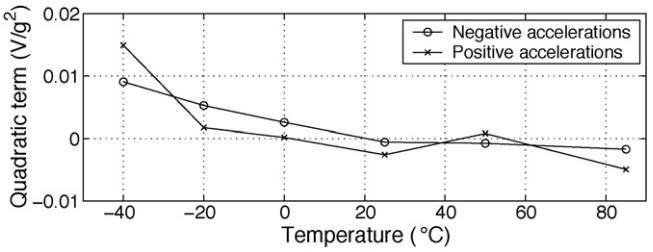

Fig. 17. The quadratic term as a function of temperature.

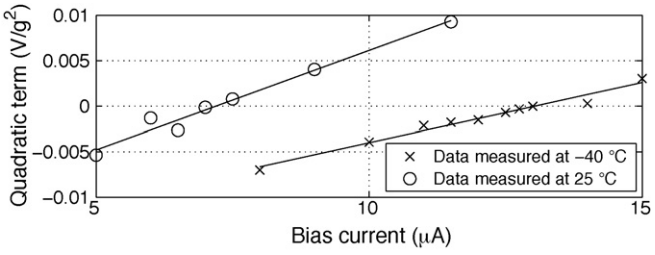

Fig. 18. The quadratic term as a function of dc compensation current at two temperatures.

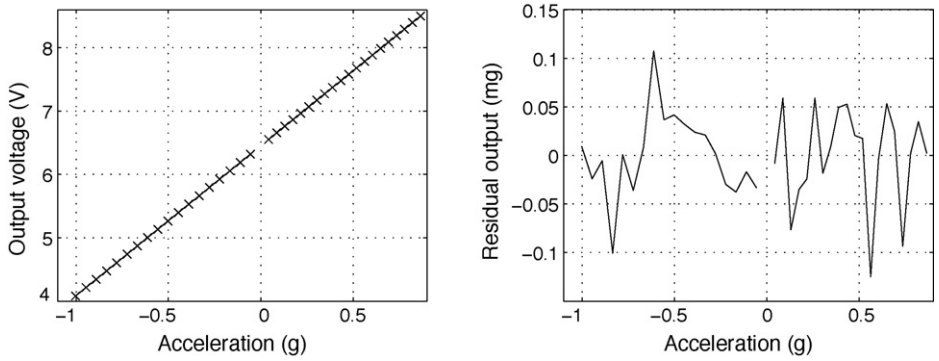

Fig. 19. The dc transfer function from acceleration to output voltage (left) and the residual error after linear fit (right).

of temperature, for example as a result of drifting phase error in demodulator clocking, would also be visible in this figure, if such gain errors were present. The test chamber fan introduces the signal to the sensor output, which inflicts error on the TF at roughly the harmonics of the line frequency. The dc block that is used to isolate the sensor output dc from the analyzer input attenuates the signal by about 1 dB at 10 Hz.

The noise equivalent acceleration density is shown in Fig. 16. The noise floors of both the digital output and the analog output are shown in the figure. The measurement PCB is isolated from the vibrations of the environment through a mass-spring system and a battery is used as a power source, and yet some line-frequency harmonics still exist in the noise spectrum. The noise in both spectra of Fig. 16 shows a rapid increase after the sensor open-loop resonance frequency. This corresponds to Fig. 3 when the dominant noise source is located in the high-frequency readout. The noise level of the analog output, 150 ng/$\sqrt{\text{Hz}}$ at 100 Hz, is roughly 3 dB higher than that expected from the theoretical calculations. The additional noise at least partly originates from the flicker noise in the base current of the CSA input transistors, which is transformed to voltage in the passive filter that precedes the CSA (see Fig. 1). This noise source was not included in the transistor models. Additionally, digitizing the output was measured to increase the noise floor by 6 dB. The figure indicates that the sensor attains a noise equivalent acceleration density of 500 ng/$\sqrt{\text{Hz}}$ for the digitized output and 300 ng/$\sqrt{\text{Hz}}$ for the analog output at 30 Hz. The noise floor can be modeled to be composed of purely flicker noise with a density of 1.7 μg/$\sqrt{\text{Hz}}$ at 1 Hz, which gives an rms NEA of 4 μg over the 300-Hz bandwidth. The resulting SNR, when referred to 1.5-*g* dc acceleration, is 111 dB.

The system linearity is measured using a rate table to provide a centrifugal force. In order to get the dc response with both positive and negative signs, the measurement system needs to be flipped around and any resulting alignment errors will cause the gain to vary. For this reason the input-output characteristics for negative and positive accelerations are plotted separately. The rate table inflicted strong AC vibration, which made it necessary to use a lower measurement range than the one specified, ±1.5 *g*. All the dc transfer functions from acceleration to output voltage are measured using the analog output, which is more tolerant of the ac vibration of the rate table, which can exceed the nominal output range. The digitizer [22] was measured to achieve a linearity of more than 90 dB and thus would not limit the system linearity.

Because of the continuous-time closed-loop system, the nonlinearity is dominated by any existing asymmetry between the capacitors of the half-bridge sensor [17]. The sensor output, with the resulting second-order distortion, can be expressed as

$$V_{OUT} = A \cdot ACC_{in} + B \cdot ACC_{in}^2, \quad (10)$$

where A is the linear term, the gain, B the quadratic term, and ACC_{in} the input acceleration. The measured quadratic term over the temperature is shown in Fig. 17, where the measurement inaccuracy causes some discrepancy between the two curves. The best linearity is achieved at room temperature. The total gain and offset variation over the temperature range are 1.3% and 0.022 *g*, respectively.

The element asymmetry can be compensated by balancing the system with either dc fed to the controller input or by using very small variable capacitors at the CSA input [17]. The quadratic term in Fig. 17 is compensated at room temperature, but the linearity clearly changes with the temperature. This means that the parasitic capacitors that cause imbalance in the voltage-to-force transducer have a non-zero temperature dependency. However, the compensation can be redone at different temperatures, as shown in Fig. 18. Here the dc current is fed to the controller integrator virtual ground and the quadratic term is plotted as a function of the bias at two temperatures. The optimum can be found at both temperatures.

With a compensated second-order term the linearity is limited by the uncertainty during the measurement, as shown in Fig. 19. The maximum residual error after linear fit is 0.11 mg or 0.014%. The linear fit is done separately for both negative and positive accelerations and is, hence, referred to half of the full-scale input, 0.75 *g*.

A summary of the essential properties of the implemented sensor is given in Table 5.

Table 5
Summary of the sensor properties.

Interface implemented in	0.7 μm HV CMOS
Chip area (mm^2)	22
Supply current (mA)	15 (5 V) and 0.9 (12 V)
Bandwidth (Hz)	300
SNR, analog output (dB)	111 (@ full-scale dc of 1.5 *g*)
Maximum dc non-linearity (%)	0.014

6. Conclusions

Several aspects of the design of an analog closed-loop accelerometer with a digital output were presented. The blocks required for the implementation of the interface are suitable for integration within a reasonable chip area. The important noise sources, especially the carrier CM noise, low-frequency noise of the feedback, and references, are identified. The linearity was shown to improve when dc compensation was used for linearizing the voltage-to-force transducer. The closed-loop operation eases the gain temperature stability requirements, which, for example, allows the carrier amplitude to change with temperature considerably more than in the case of an open-loop interface. A stable sensor requires careful recognition of sources of instability, some of which are the leakage in the demodulator and insufficient attenuation in

filters and, especially, the parasitic vibrational modes of the sensor element.

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Biographies

Lasse Aaltonen received the MSc and LicSc degrees in Electrical Engineering from Helsinki University of Technology (TKK), Espoo, Finland, in 2004 and 2006, respectively. Currently he is working towards doctoral degree, in the Electronic Circuit Design Laboratory, TKK. His main research interest is design of electronics for micro-electromechanical sensors.

Kari A.I. Halonen received the MSc degree in Electrical Engineering from the Helsinki University of Technology, Finland, in 1982, and the PhD degree in Electrical Engineering from the Katholieke Universiteit Leuven, Belgium, in 1987.

Since 1988 he has been with the Electronic Circuit Design Laboratory, Helsinki University of Technology. From 1993 he has been an Associate Professor, and since 1997 a Full Professor at the Faculty of Electrical Engineering and Telecommunications. He became the Head of Electronic Circuit Design Laboratory in 1998. He specializes in CMOS and BiCMOS analog integrated circuits, particularly for telecommunication applications. He is the author or co-author of over 200 international and national conference and journal publications on analog integrated circuits.

Prof. Halonen has been an Associate Editor of *IEEE Transactions on Circuits and Systems I*, a Guest Editor for *IEEE Journal of Solid-State Circuits* and the Technical Program Committee Chairman for European Solid-State Circuits Conference year 2000. He has been awarded the Beatrice Winner Award in ISSCC'02 Conference in 2002. He is a TPC member of ESSCIRC and ISSCC.